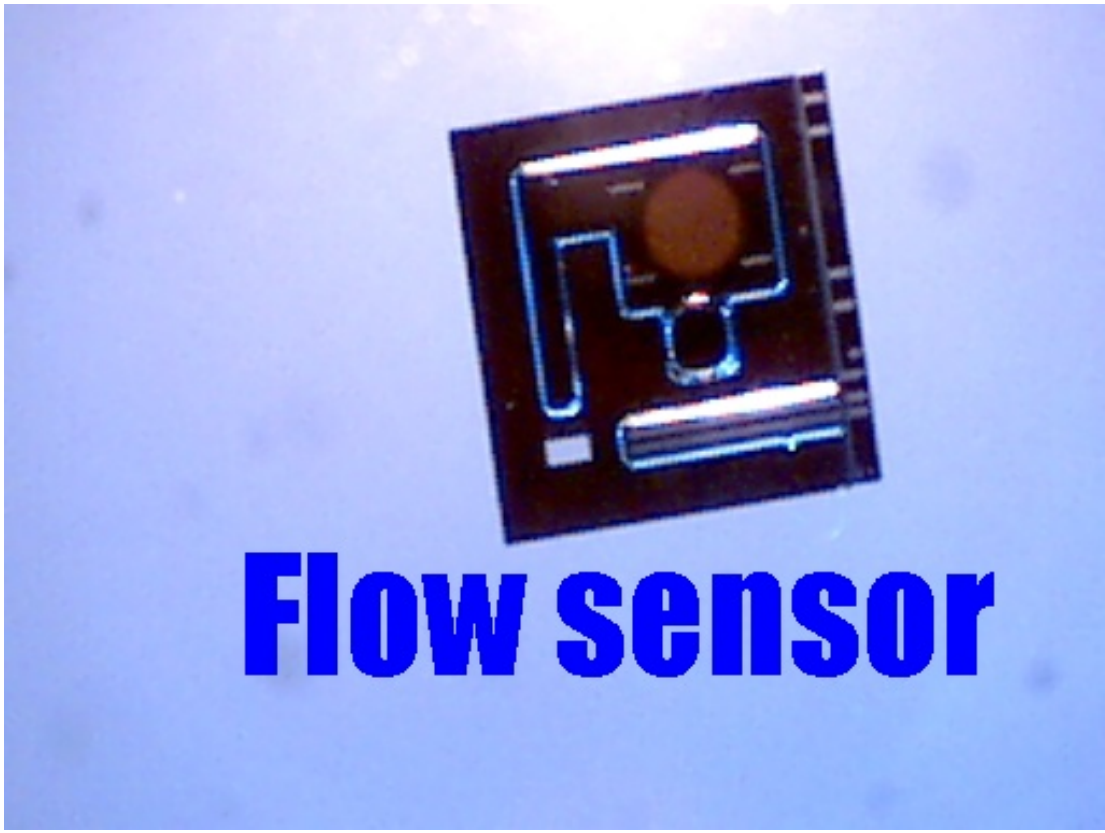
Microfabrication

Example: Manufacturing of flow sensor

Design and manufacturing of a flow rate sensor step-by-step SensoNor Multi-Project-Wafer MPW process

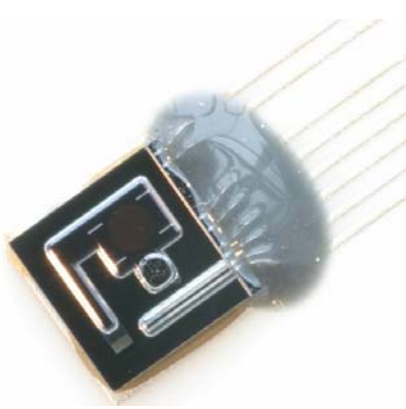
- Principle of flow sensor

- Step-by-step:
- Lithographic mask layout
- Manufacturing processes associated with mask layers



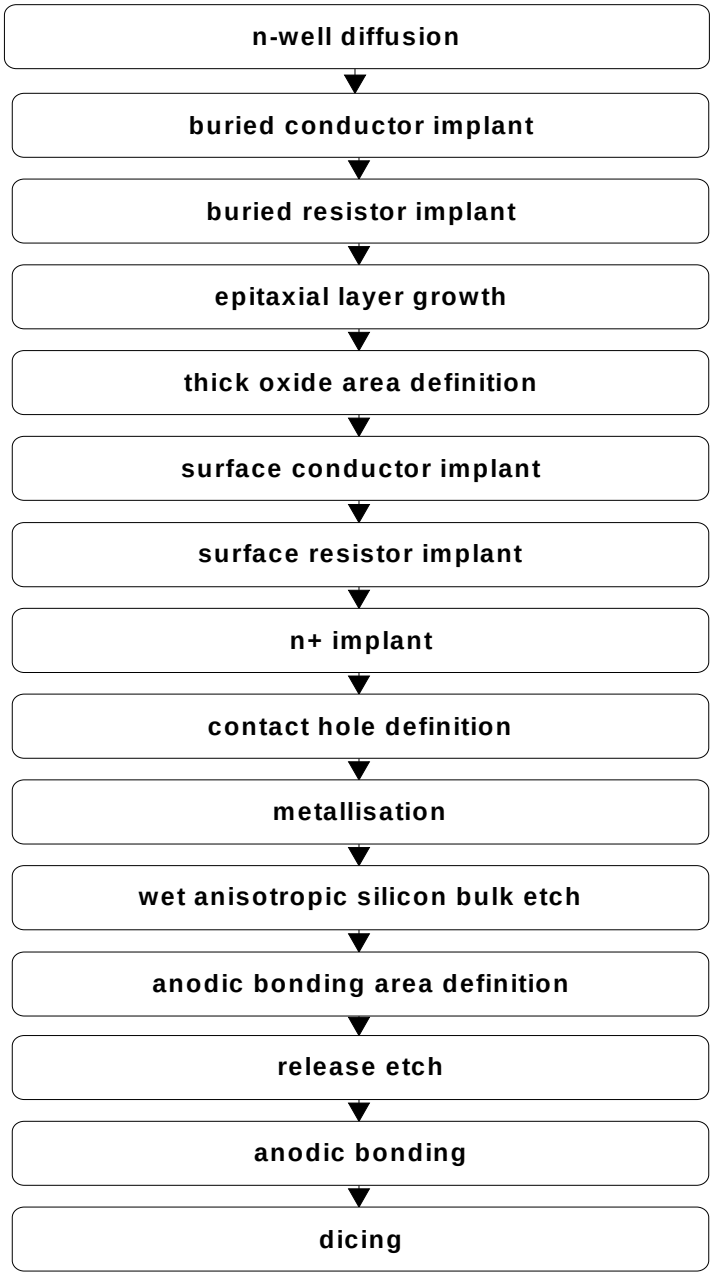
Flow sensor is made from silicon and pyrex glass

The world's leading manufacturing line for tire sensors is used for production of the flow sensor



The SensoNor An Infineon Technologies Company foundry produces a micro-fluidic element for the first time

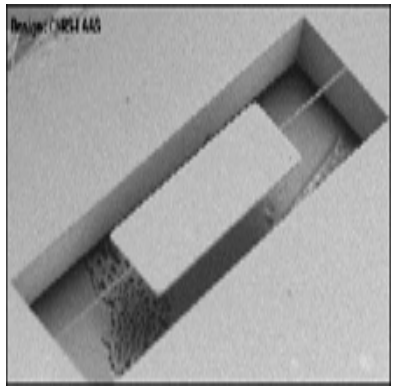
Overview of SensoNor MPW process

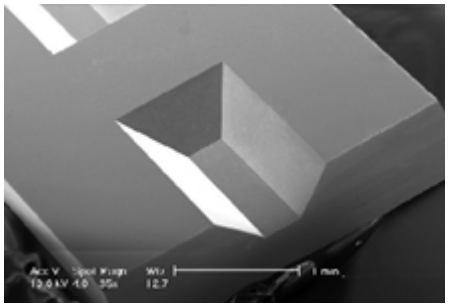


From idea to chip

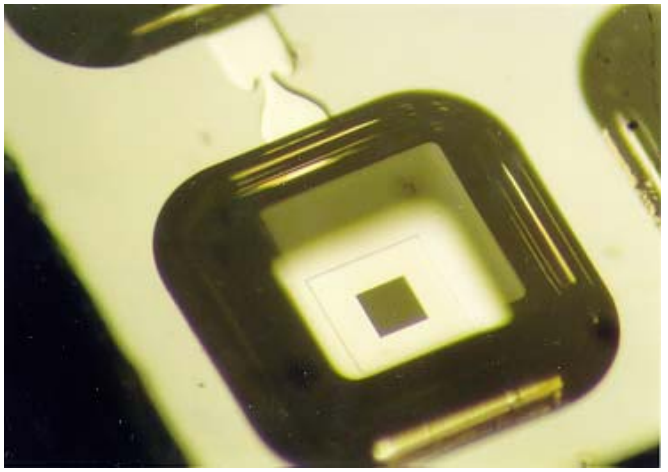
- Design – the concept
- Design of lithographic masks
- Manufacture quartz / chromium lithographic masks
- Perform all manufacturing steps in clean room
- Saw into dices
- Package

Bulk Silicon Micro machining

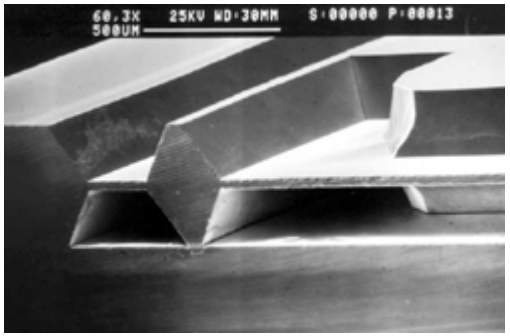


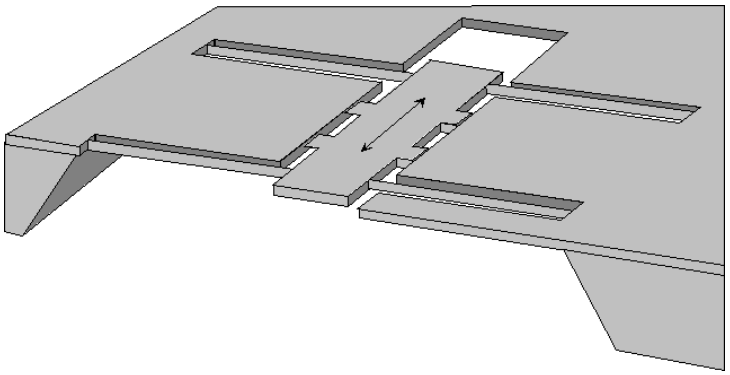


TRONIC'S

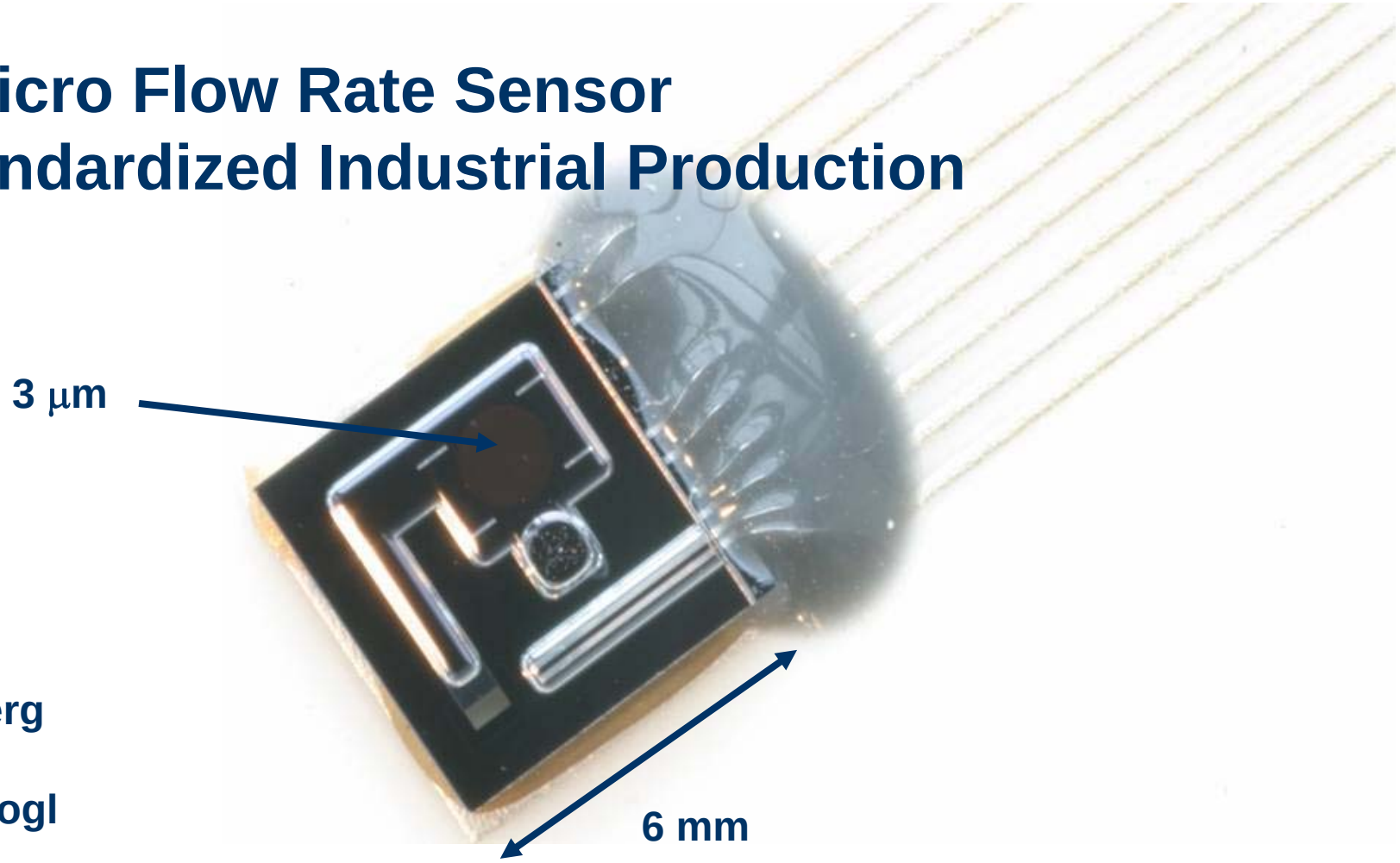


SensoNor





New Micro Flow Rate Sensor for Standardized Industrial Production

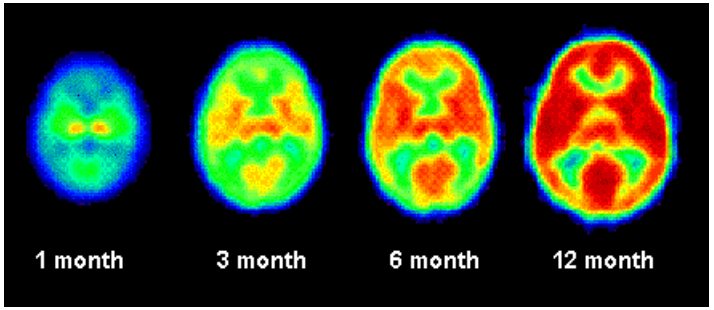


Liv Furuberg
Dag Wang
Andreas Vogl

Microsystems and Nanotechnology
SINTEF Information and Communication Technology

The miniature flow rate sensor can be used in diverse applications

Safety check of implanted medicine pumps



Reagent flow rates in micro reactor for PET radioactive isotopes

Measuring flow rates of enzymes into bacteria analysis chip

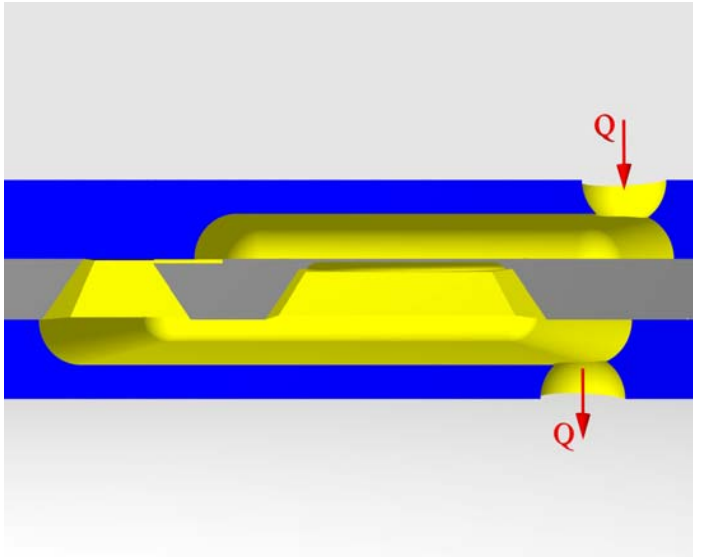
Monitoring the dosing of medicine

Design of sensor

- Inlet/Outlet:
  through etch top/bottom glass

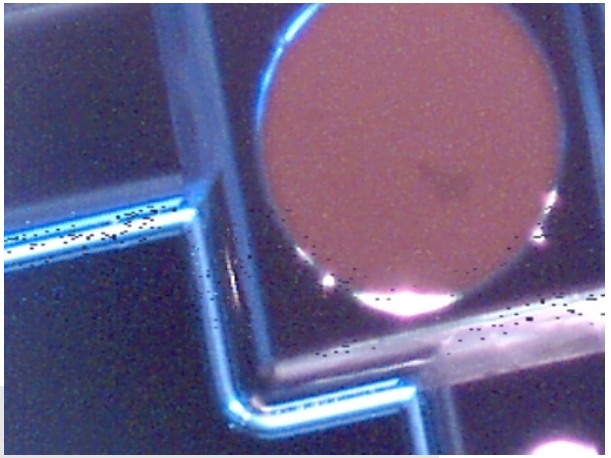
- Flow channels:
  etch in glass, RIE-etch in silicon

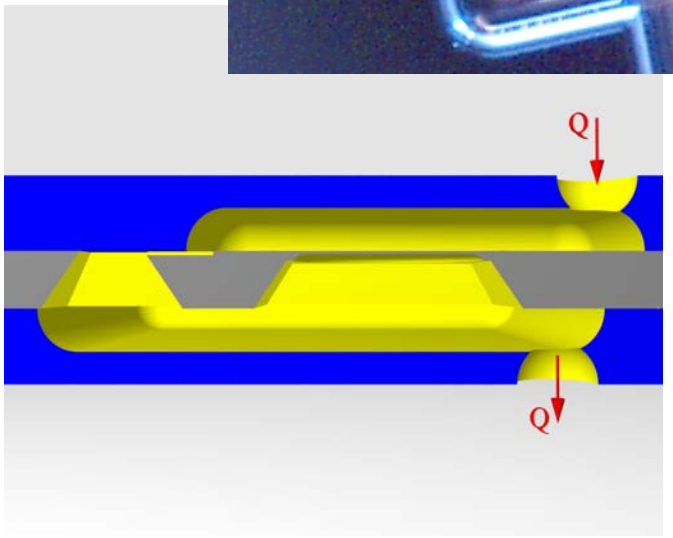
- Pressure sensor:
  anisotropic etched membrane with piezoresistive Wheatstone bridge



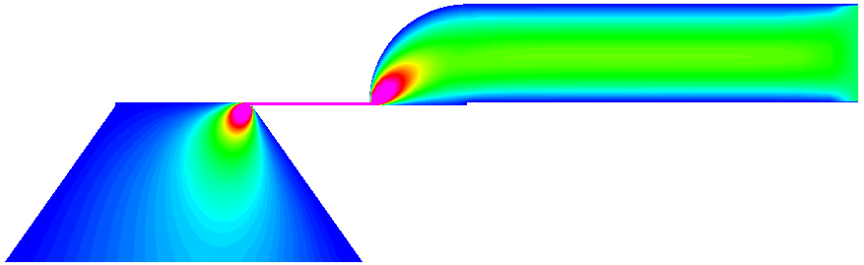
Volum-strømningsmåler

- Applikasjoner: Dosering, tilføring av reagenter, måle flow gjennom analysesystem
- Væskestrøm gjennom brikken
- Glass-silisium-glass brikke
- Laminær strøm, lave Re tall
- Differensiell trykksensor (membran + piezomotstander)
- Trang kanal med trykkfall, Pouseille strøm
- Trykkfall ~ 100 -200 Pa
- Integrert temperaturmåler



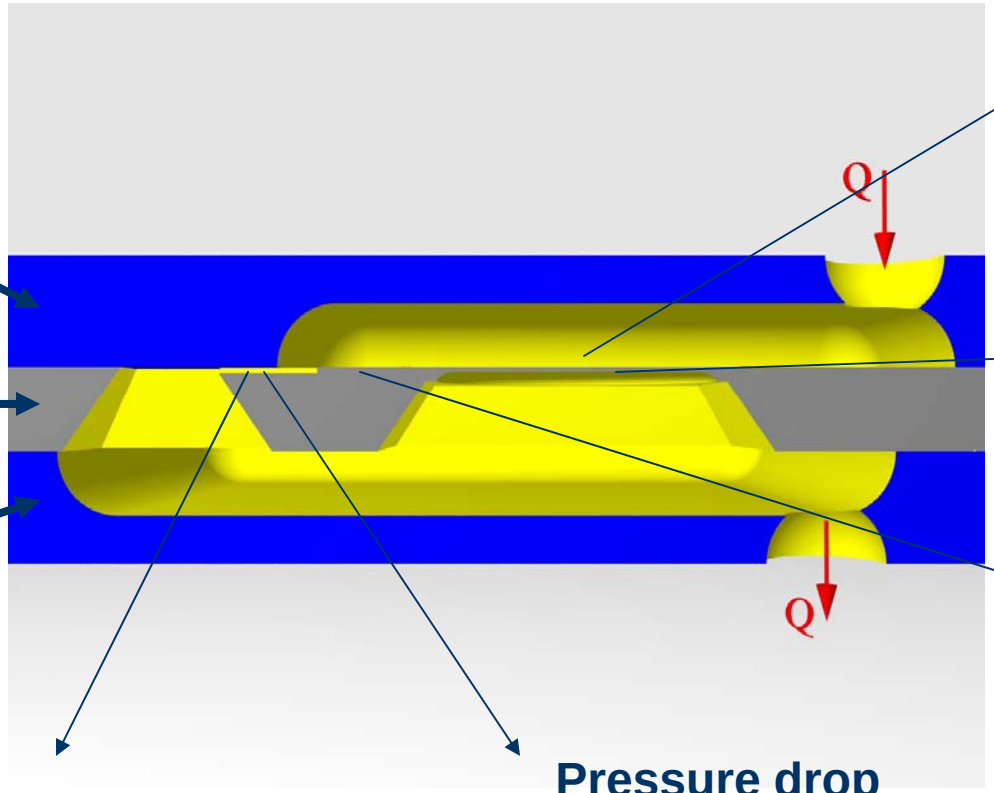


- Kanal: 800x1500x10 μm
- Flow rate 2 μl/min



$$\Delta p = \frac{12 \cdot \eta \cdot l \cdot Q}{w \cdot h^3}$$

The new design suggests a low-noise, mechanically robust flow sensor



Sensitive and strong membrane

Pyrex

Silicon

Pyrex

Protected piezoresistors for stress measurements

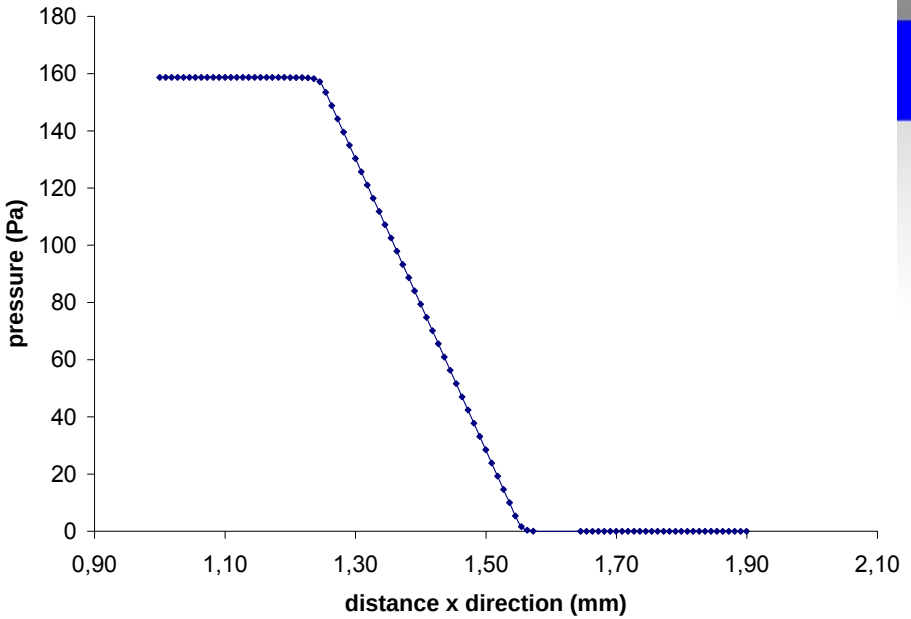
Temperature sensing diode

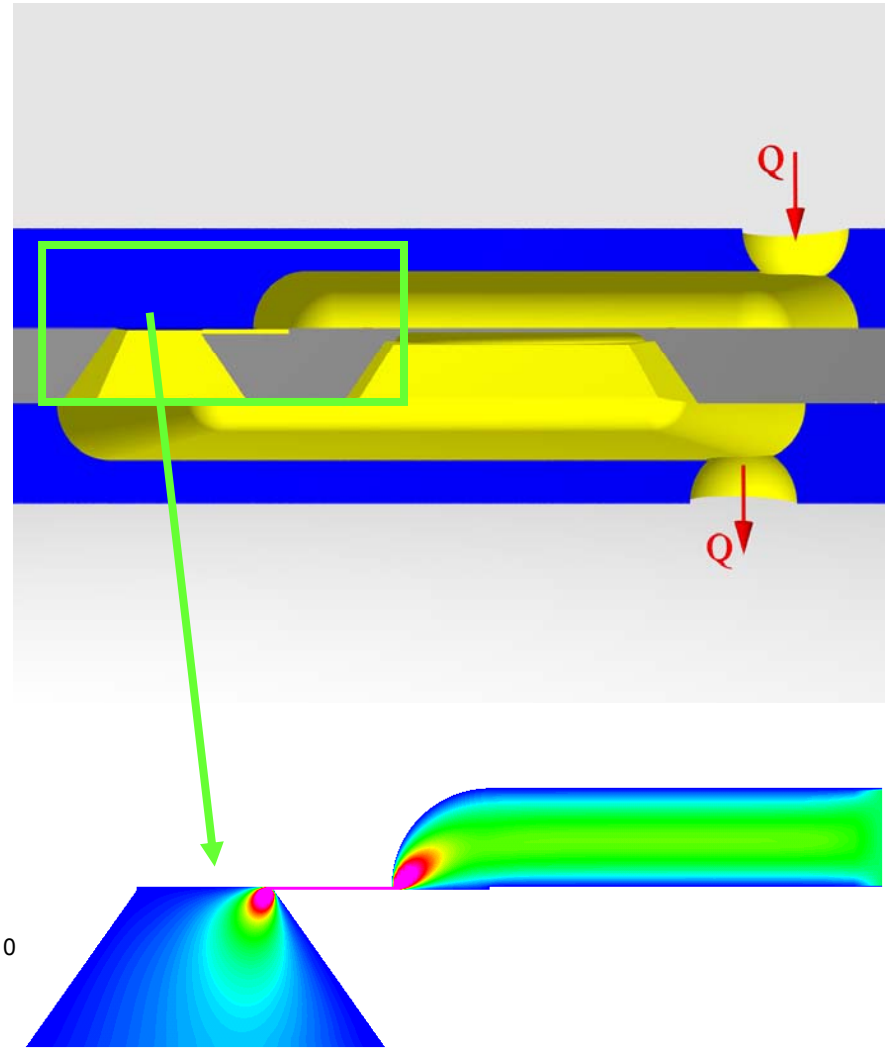
Channel depth 11 μm

Pressure drop proportional to the flow rate

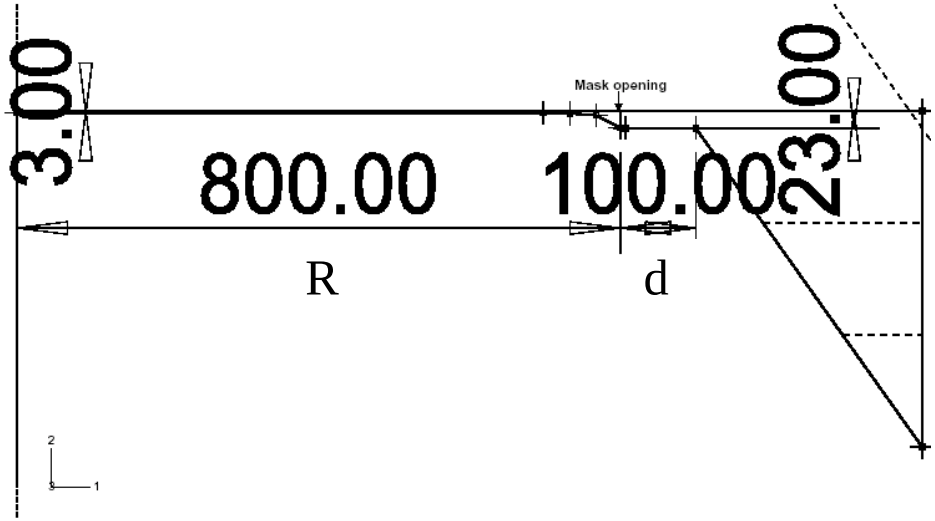
Determine dimensions: Flow simulations

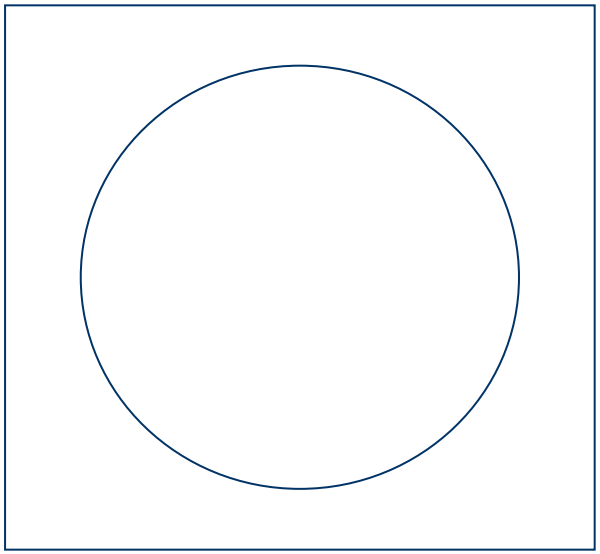
- Finite volume simulations of flow field (CFDRC)



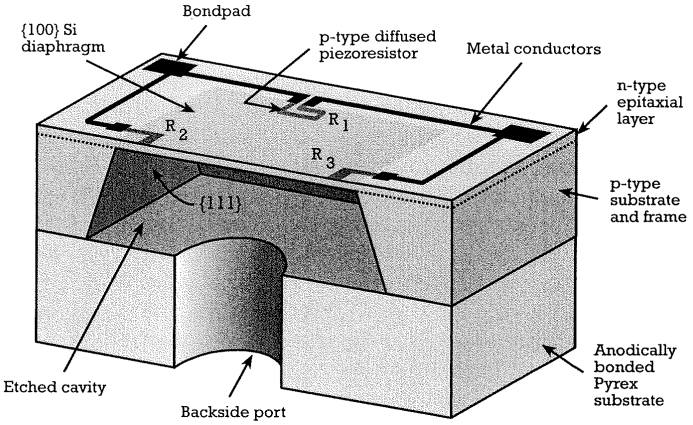


Pressure sensor: Thin circular membrane embedded in a thicker square membrane

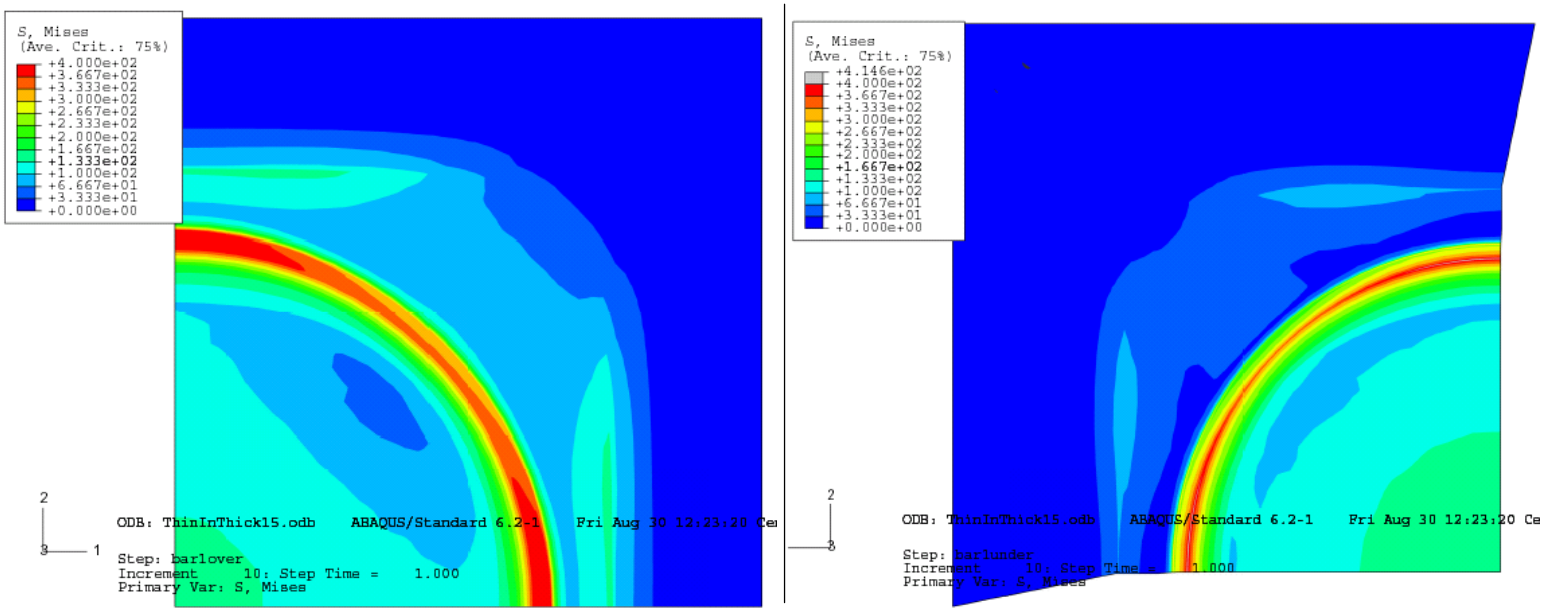




From Maluf



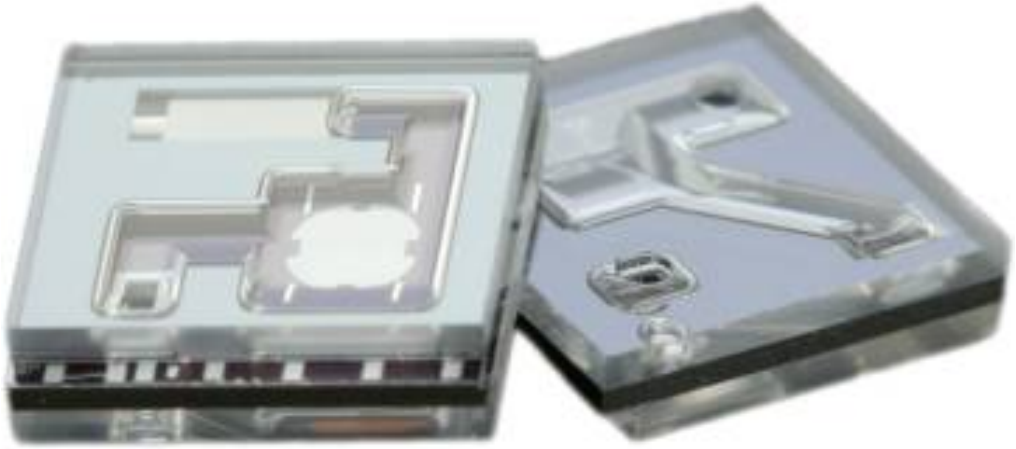
Determine dimensions: elastic/mechanical simulations using CoventorWare

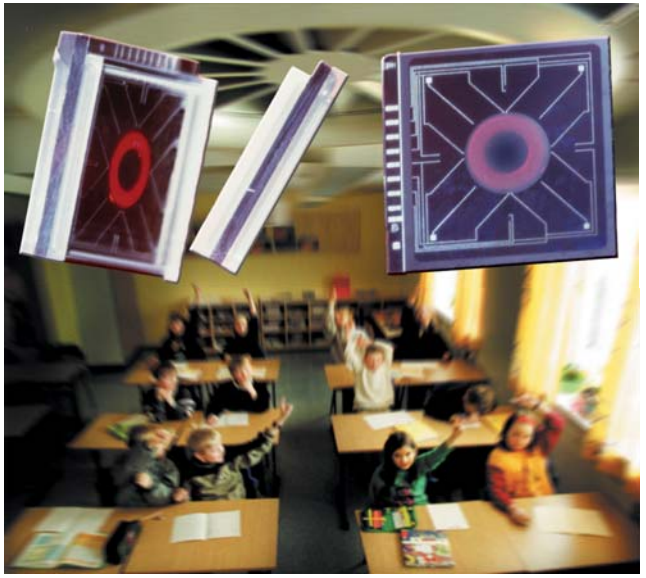


Stress distribution caused by: Left 1 bar pressure from the top, top view. Right 1 bar pressure from the bottom, bottom view. Only ¼ of the membrane is simulated. The stress shown is the von Mises stress in MPa.

Production processes for bulk micromechanical devices

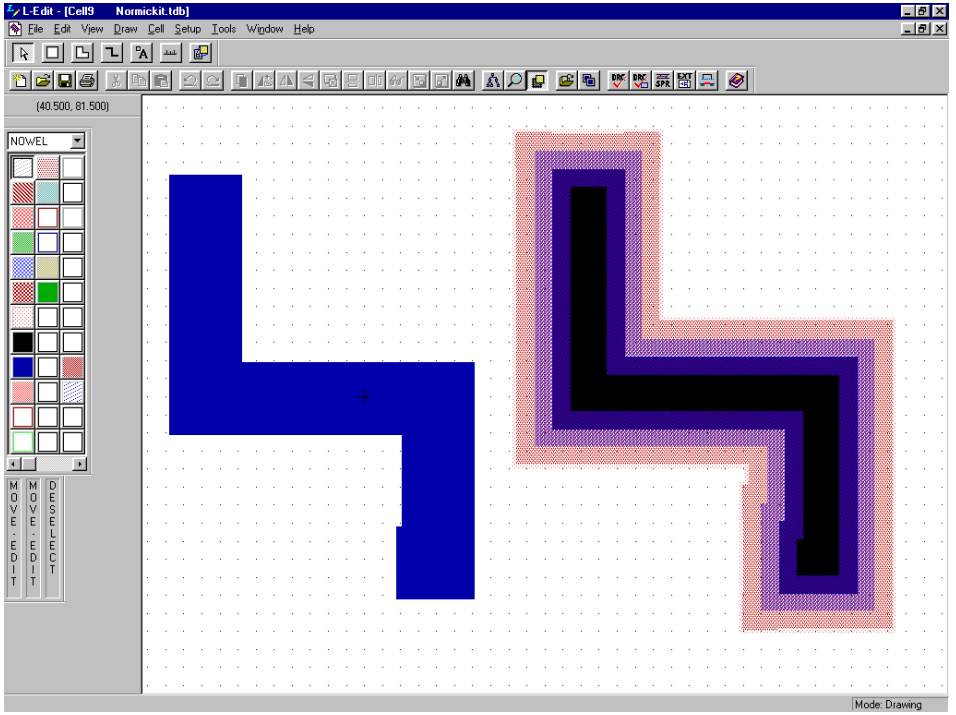
- Semiconductor integrated circuits processes
  oxidation
  implantation
  metal deposition
- Silicon 3D etching:
  Anisotropic wet
  Dry RIE
- Glass etch:
  Isotropic wet etch
- Wafer bonding
  Glass wafer + silicon wafer
  (anodic bonding)





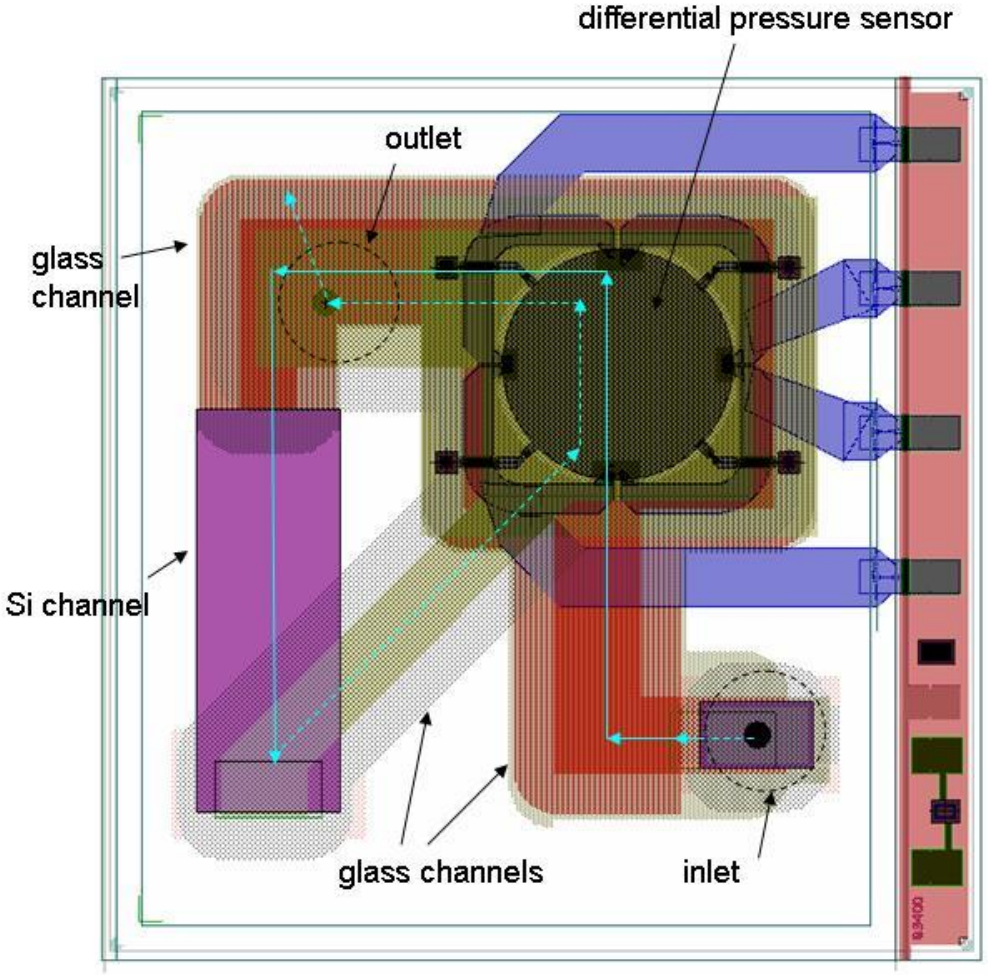
Mask drawing and production

- Draw mask layers
- Some process steps need masks, some do not
- Send design to mask manufacturer
- Get back fused silica (amorphous quartz) plates
- Pattern is in chromium layer



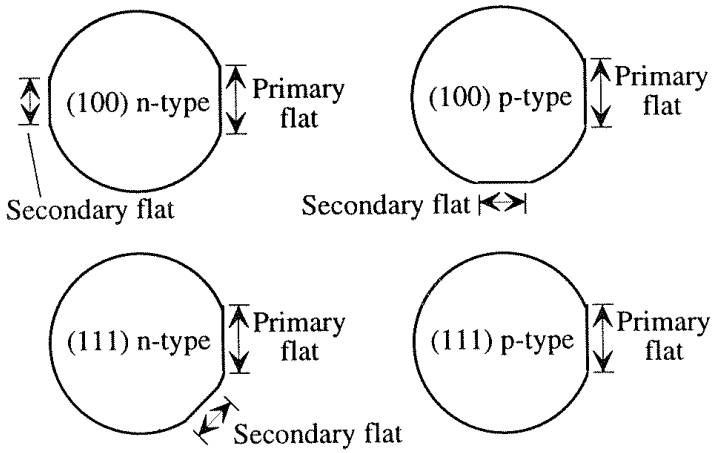
Design of mask layers

(here are all mask layers on top of each other)



Start with silicon wafer: made of single crystal (cubic crystal)

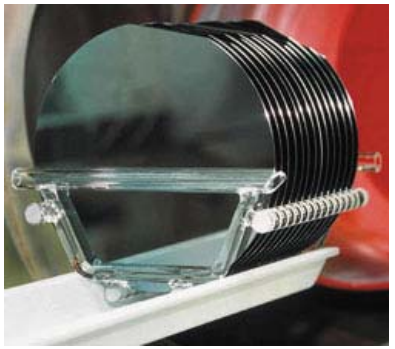
- Flats define crystal orientation and doping



. Primary and secondary wafer flats are used to identify orientation and type.

Crystal orientation is important in micromachining because of :

- Wet silicon etch
- Piezoresistors



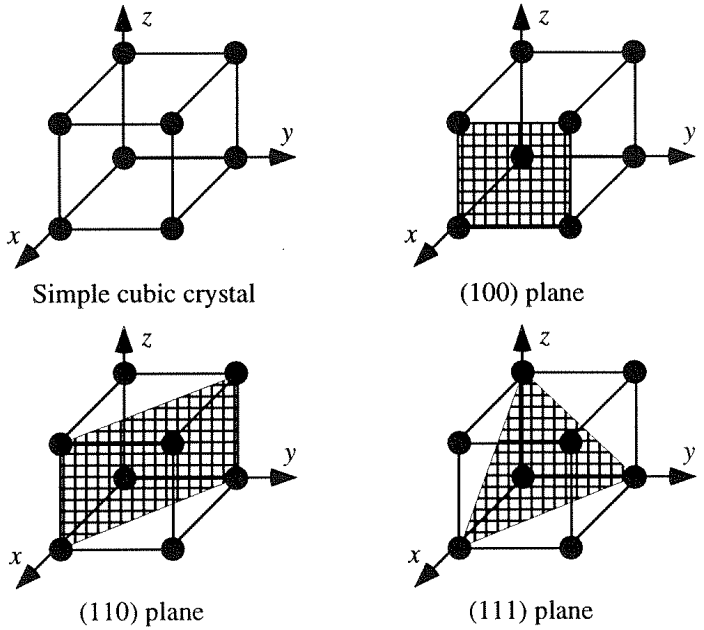
TRONIC'S

Start with silicon wafer: made of single crystal cubic crystal

- Definition of directions and planes in crystals

Miller indices

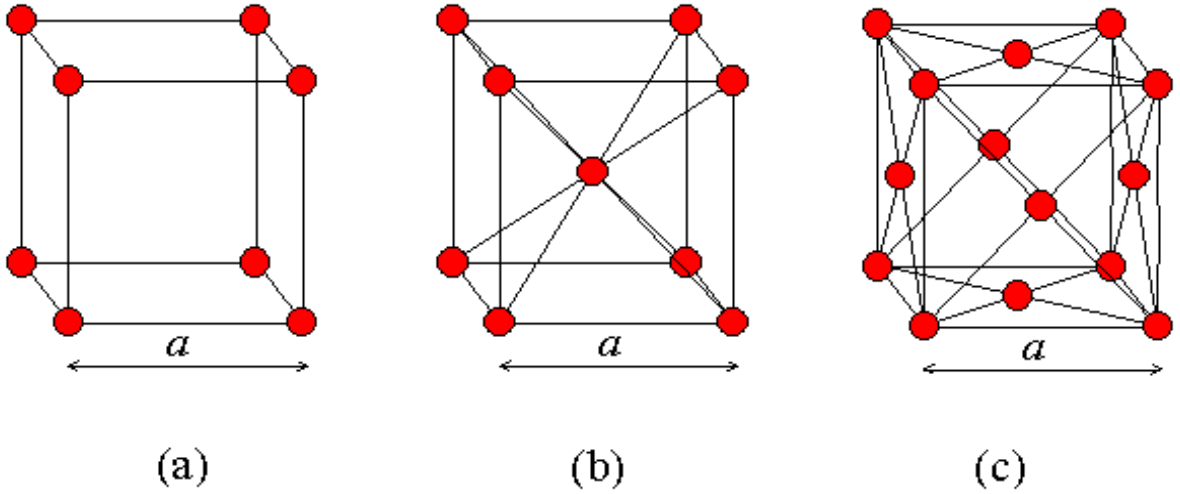
- Direction [100]
- Plane perpendicular to this direction (100)
- Equivalent directions <100>
- Equivalent planes {100}



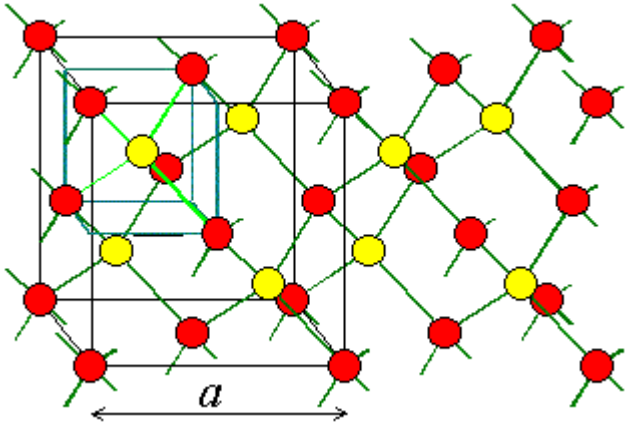
re 3.1. Illustrating the different major crystal planes for a simple cubic lattice of atoms.

Cubic Lattices

- Face centred cubic lattice



- Silicon: Two face centred cubic lattices. Two atoms per basis



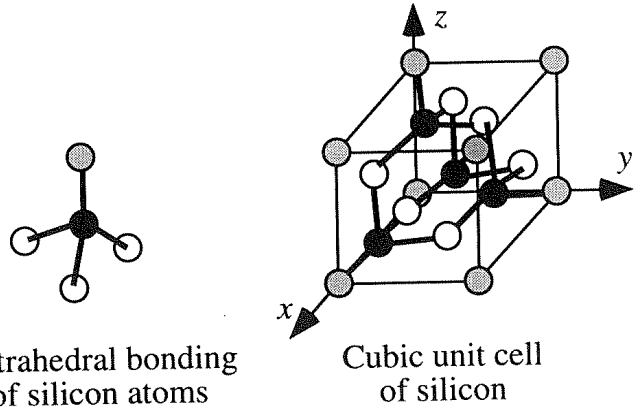
Colorado University

Silicon crystal structure

- Silicon: Face centred cubic

+ second shifted lattice The second lattice is displaced one quarter along the body diagonal

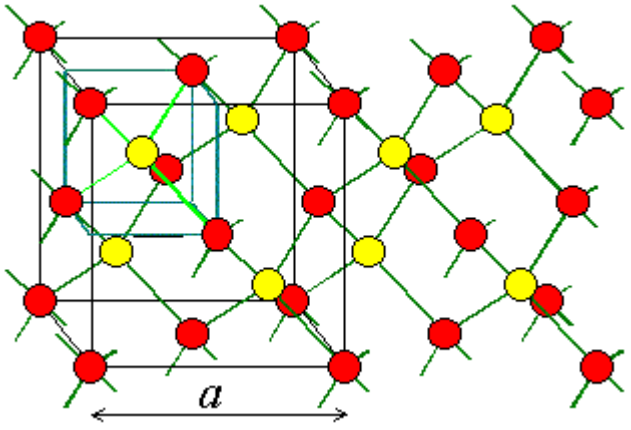
(silicon has diamond structure)



Tetrahedral bonding of silicon atoms

Cubic unit cell of silicon

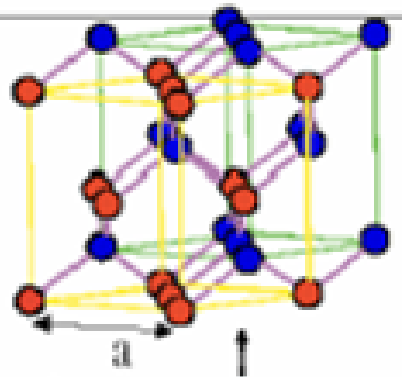
- Covalent bonds
- (111) planes highest atom density
- silicon atoms in (111) plane bonded to three atoms under plane, one over plane
- silicon atoms in (100) and (110) planes bonded to two atoms below and two atoms over plane

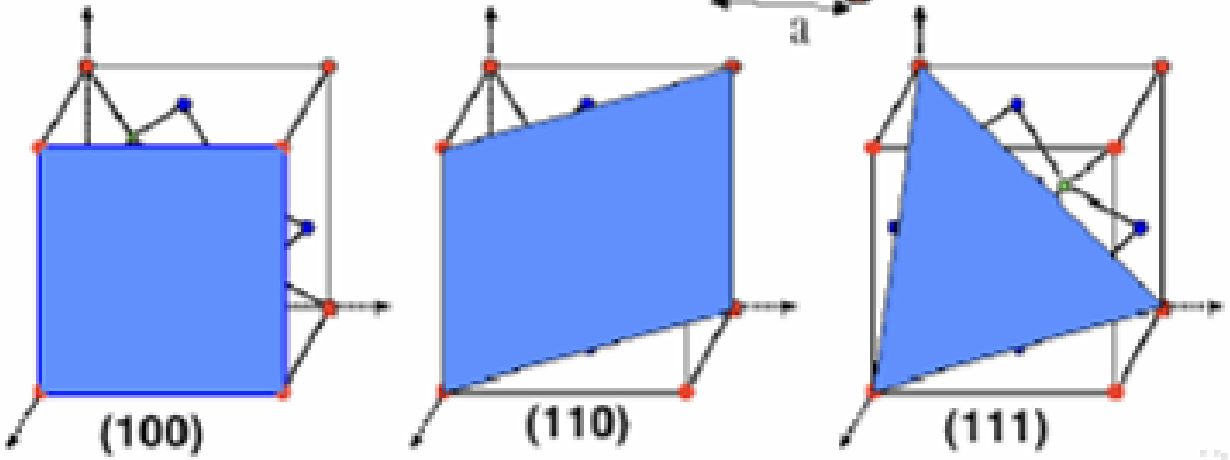


Silicon Etching

Crystallographic etching

- recall crystal lattice is face centered cubic (FCC), with two atom basis [at (0,0,0) and (1/4, 1/4, 1/4)]
  - two "interpenetrating" FCC lattices





1st process step: Oxidation

- Start with p-type 100, 400 μm thick wafers
- Create “Glass” layer covering silicon wafer
- Silicon dioxide SiO_2
- **Protection** - or dielectric - or spacer

- Tube furnaces: 850-1200 °C
- Dry oxidation: Pure O_2
- Wet oxidation: Water vapour

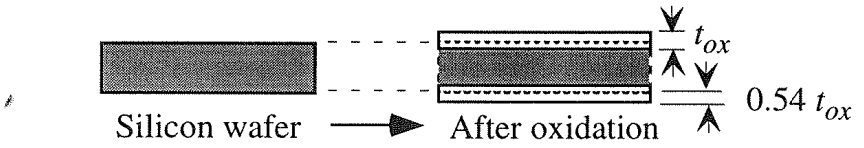


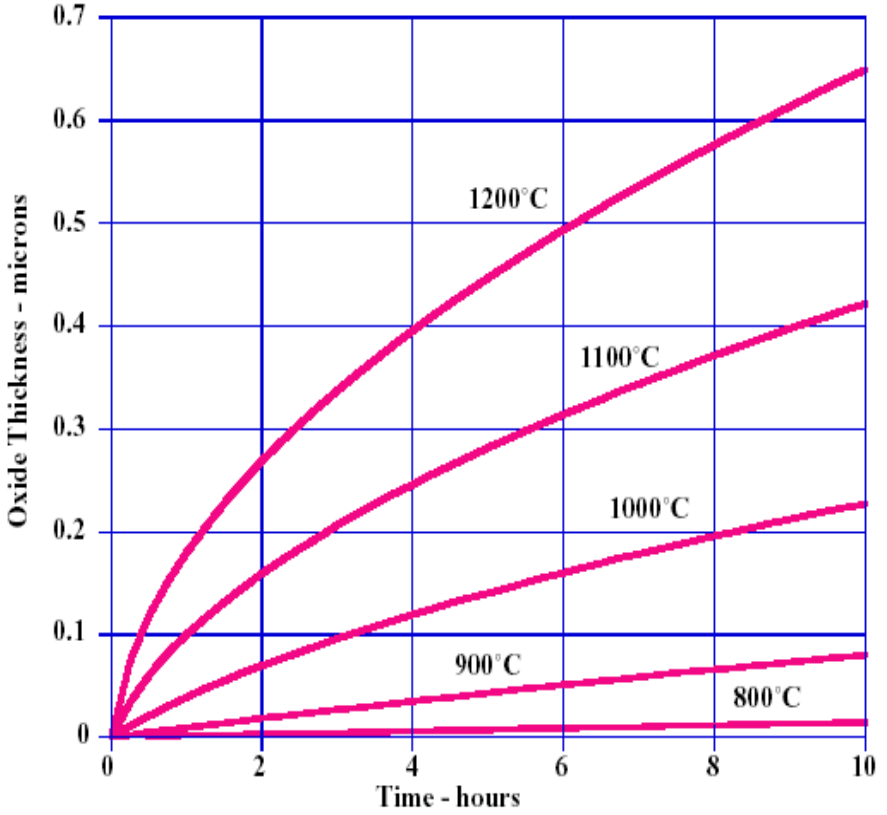
Figure 3.4. Thermal oxidation consumes some of the wafer thickness. Only 54% of the final oxide thickness appears as a net increase in wafer thickness. The remaining 46% appears as a conversion of silicon to oxide within the original wafer.

Oxidation, Deal-Grove model

- Deal-Grove model of layer thickness/time:

$$x_f = 0.5\left[A_{DG}\sqrt{1+\frac{4B_{DG}}{A^2{}_{DG}}(t+\tau_{DG})} - 1 \right]$$

Reaction limited at thin oxide layers
Diffusion limited at thicker oxide layers, oxygen diffuses through oxide

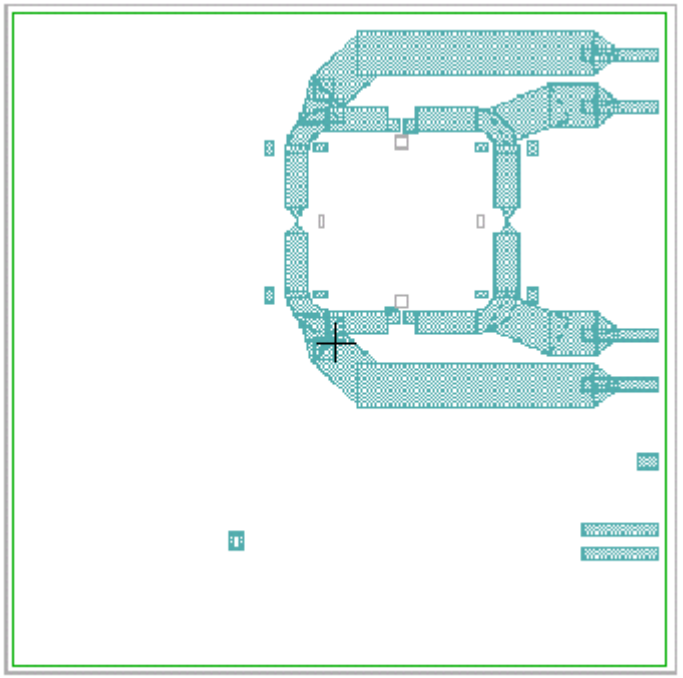


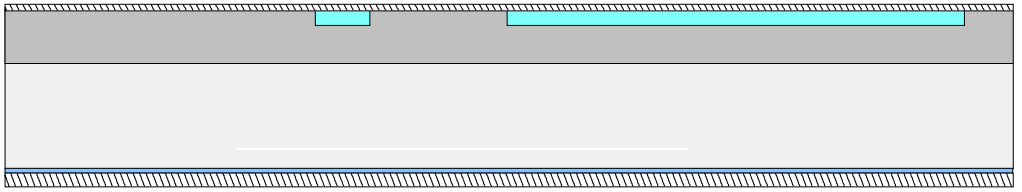
• Calculated dry O_2 oxidation rates using Deal Grove.

BUCON mask (boron doped buried conductors)

Used for conductors into hermetically sealed cavities, conductors, connection

- **Drawn areas define pattern of buried conductors (reverse polarity)**





Optical lithography

Transfers pattern from mask to resist-covered silicon wafer

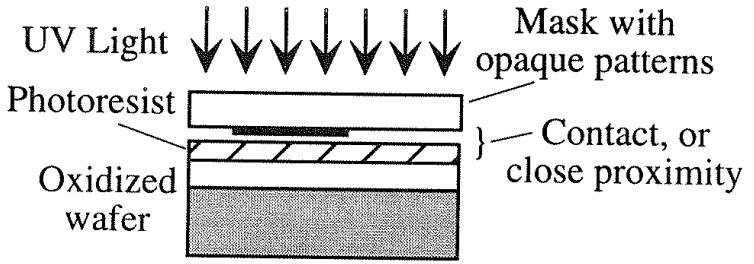
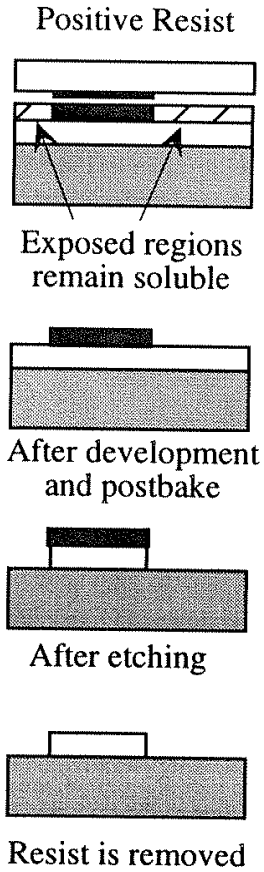
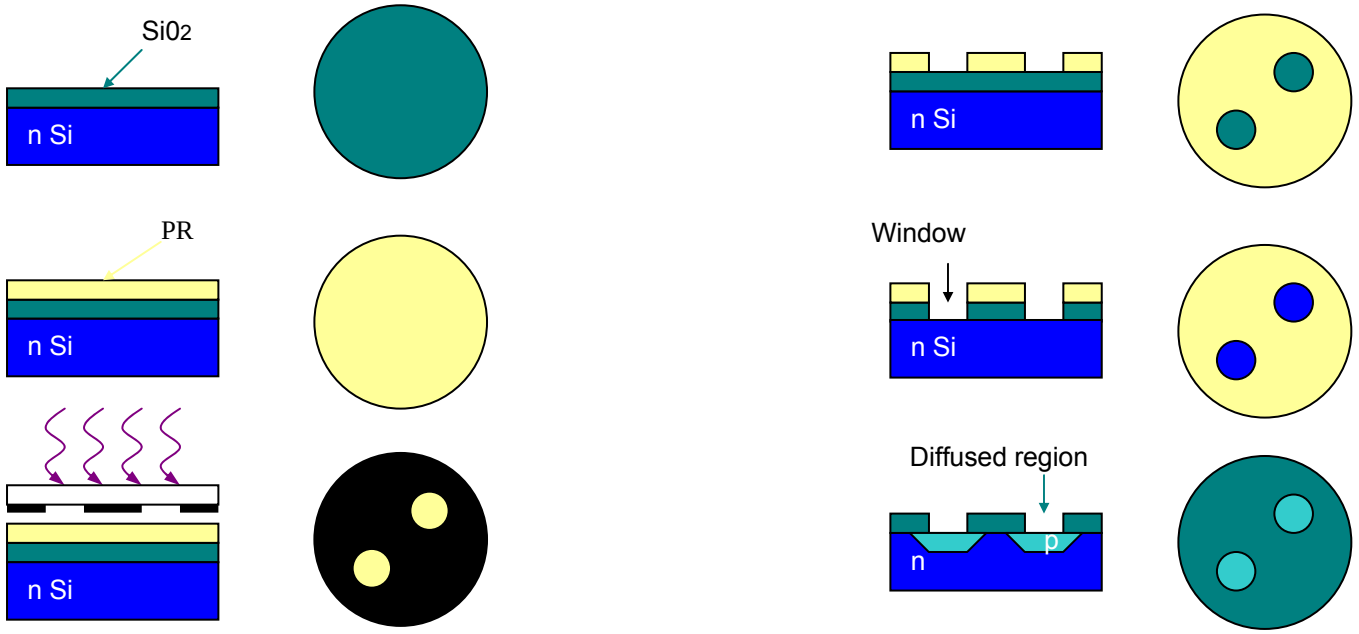


Figure 3.13. Illustrating contact or proximity photolithography.



Photolithography (positive resist)



Doping (Chapter 3.2.5)

- Boron doping of silicon:
  charge carriers “HOLES”, p-type

- Phosphorous/Arsenic doping of silicon:
  charge carriers conductor “ELECTRONS”, n-type

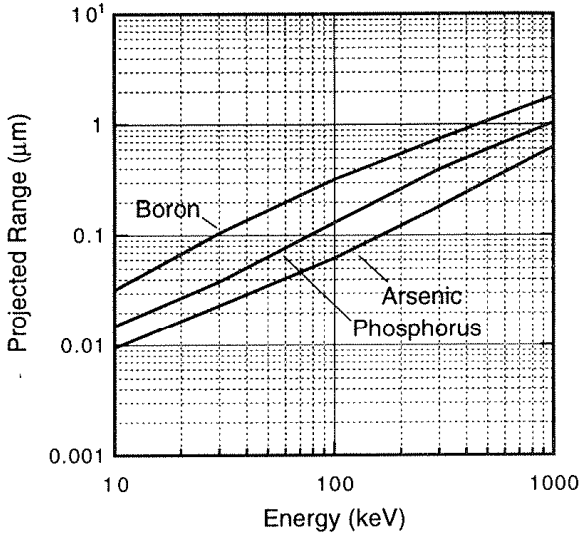
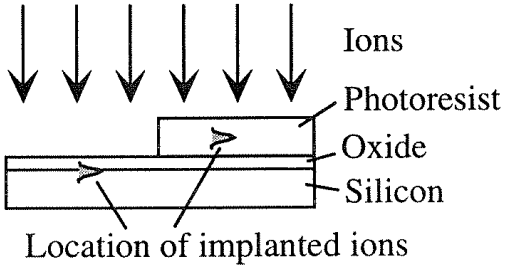


Figure 3.6. Projected ranges of ions implanted into silicon (redrawn from [7]).

Ion implantation

- Particle accelerator shoots a beam of dopant atoms directly into the wafer
  - Calculate energy/depth of dopant atoms in advance

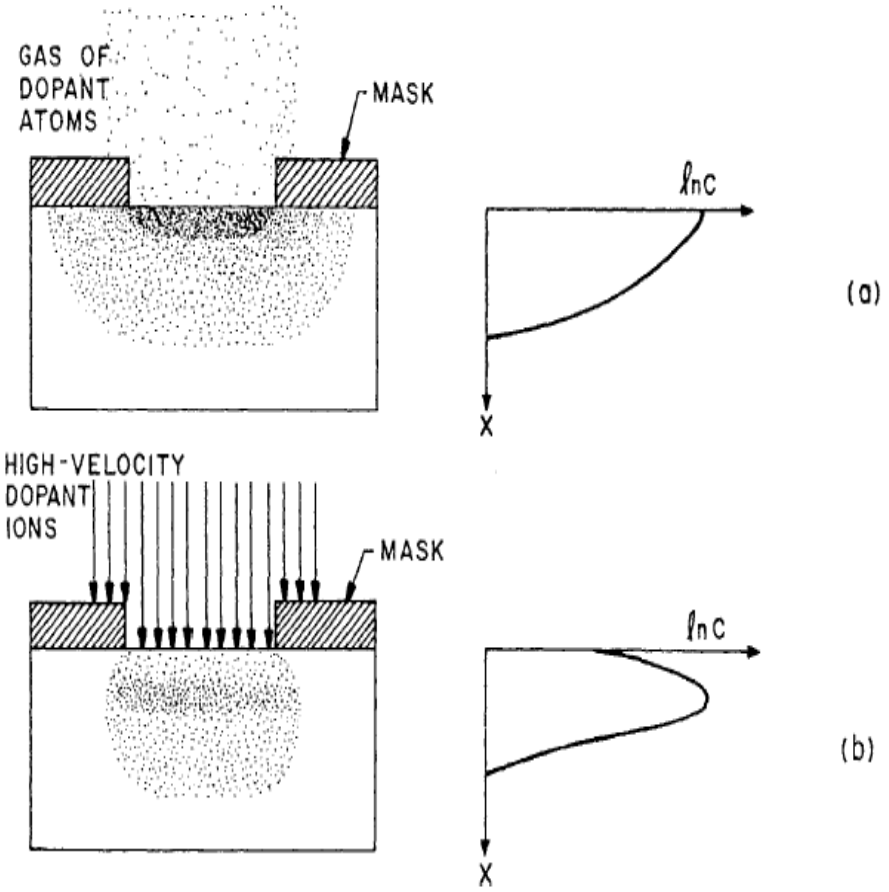


igure 3.7. Illustrating the use of a photoresist mask to keep the implant from reaching the ilicon in selected regions.

Implantation or gas doping + diffusion

- Deposition
- Dose [atoms/cm^2]

- Annealing or
- Drive-in



Drive-in diffusion of implanted atoms

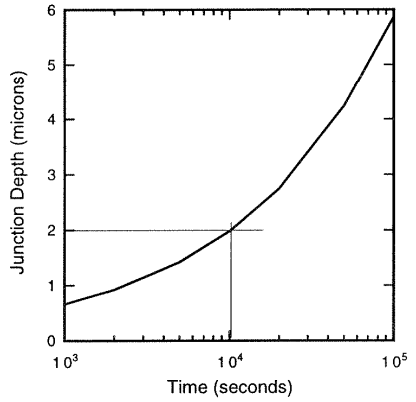
- High temperature (1000-1150°C)
- Flux of dopants from regions of high concentration to regions of lower concentration
- Sharp dopant profile at time t=0, gaussian profile after time t:

$$N(x,t)=\frac{Q}{\sqrt{\pi Dt}}e^{-\left[\frac{x^2}{4Dt}\right]}$$

Junction depth:
Depth at which the concentration of doped atoms equals the background concentration of the wafer

Example 2.2

An n-type substrate with a background doping $N_D = 10^{15}$ cm^{-3} is doped by ion implantation with a dose of boron atoms Q of 10^{15} cm^{-2}, located very close to the surface of the silicon. The wafer is then annealed at 1100°C. How long should the drive-in anneal be to achieve a junction depth of 2 μm? What is the surface concentration that results?

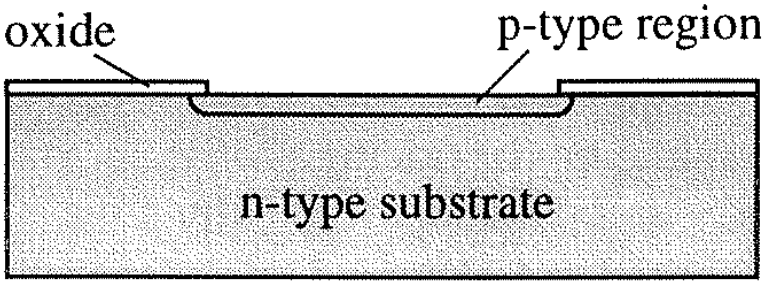


Example 2.2

Solution: Since the equation relating junction depth to diffusion time is transcendental and cannot be algebraically inverted, one can either plot x_j *vs.* t and read off the required time, or use an iterative numerical solution of the transcendental equation. The graph is shown above, with the result that the anneal time is 10^4 seconds, or 2.8 hours. The surface concentration is found by substituting this value for t into Eq. 3.8, and evaluating $N(0, 2.8\text{ hr})$. The result is 1.8×10^{19} cm^{-3}.

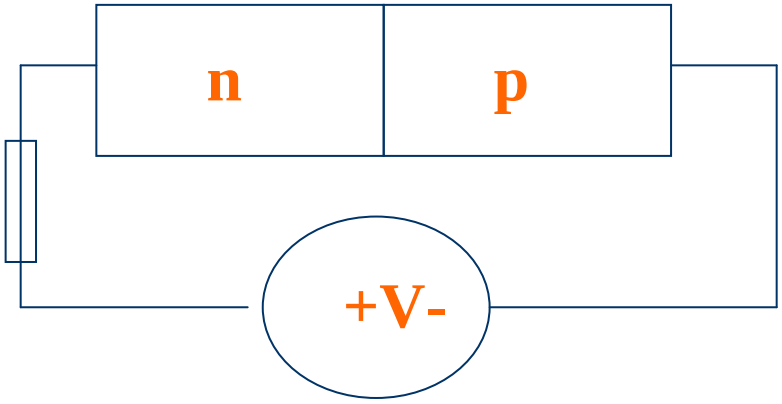
Electronics (Chapter 14.1 - 14.4)
Doped resistors

Define a p-type circuit
in a n-type wafer



n-type wafer must be at positive potential relative to the p-type circuit

Reverse biased diode → no current between circuit and wafer/substrate



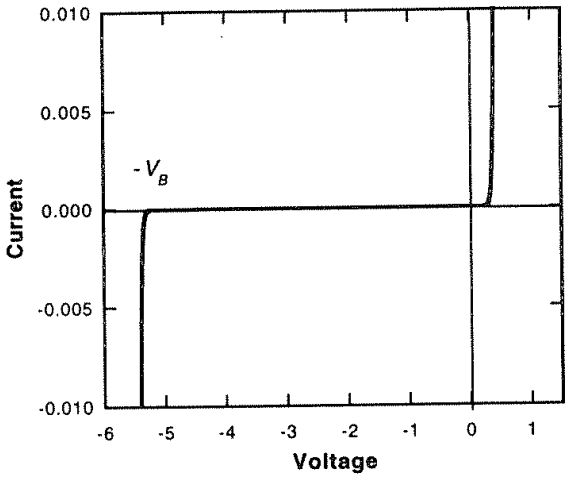
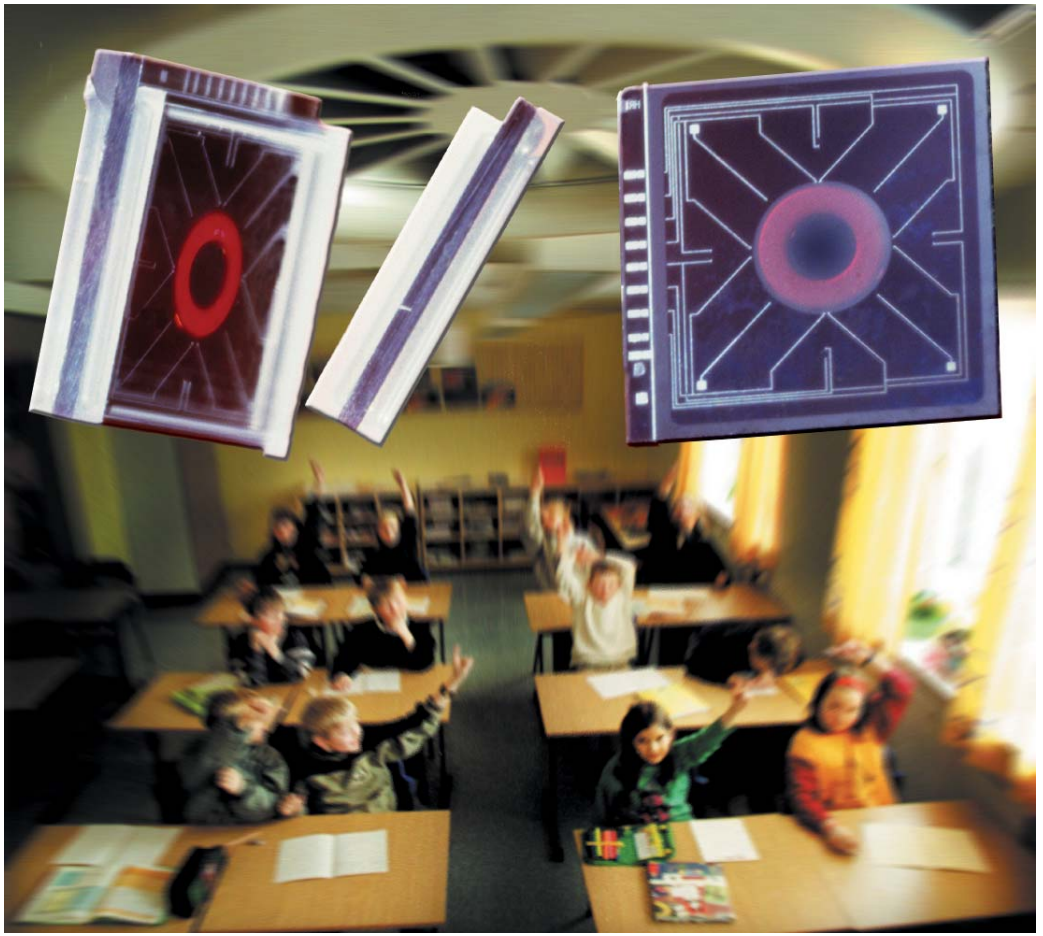


Figure 14.3. A typical diode current-voltage characteristic.

P-type electric circuit patterned in surface of n-type silicon wafer



Metal lines on top of p-type doping are visible

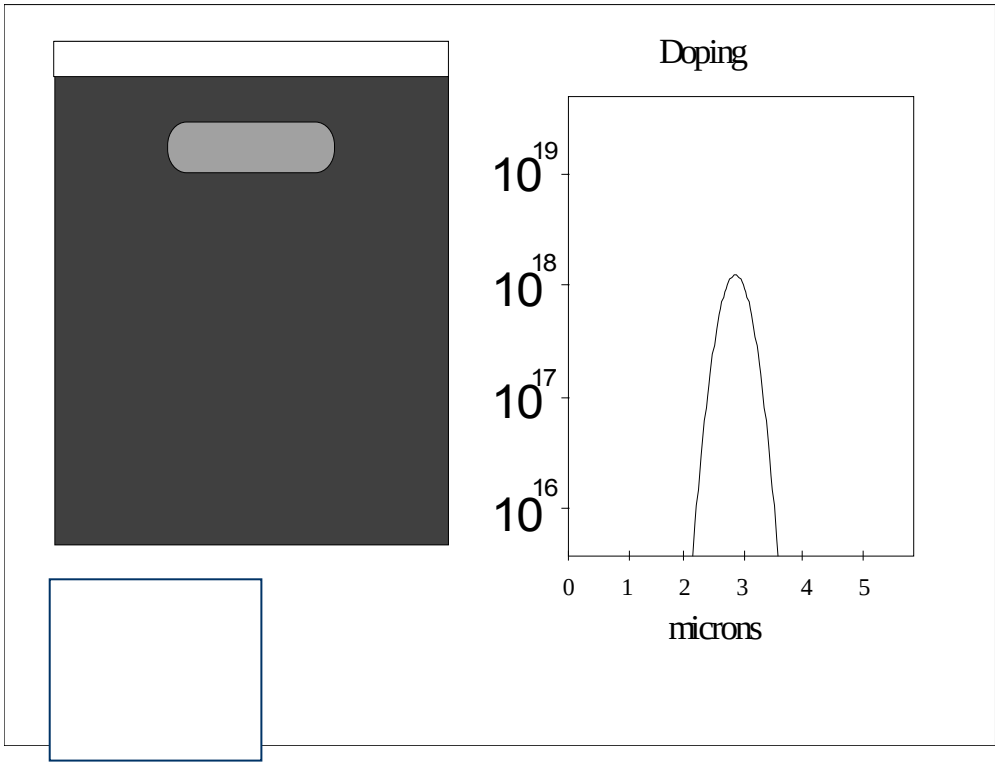
Epitaxial silicon layer (2µm thick)

- Single crystalline silicon grown on top of silicon (with doped patterns)
- Silane (SiH_4)
- The underlying silicon serve as template for the deposited material to develop an extension of the single crystal

- Chemical vapor deposition CVD
- Precursor material in heated furnace/plasma
- Chemical reaction on surface of silicon wafer: Deposition
- LPCVD : Low Pressure CVD
- PECVD: Plasma Enhanced CVD, deposition in a glow-discharge plasma (lower temperatures < 400 C)

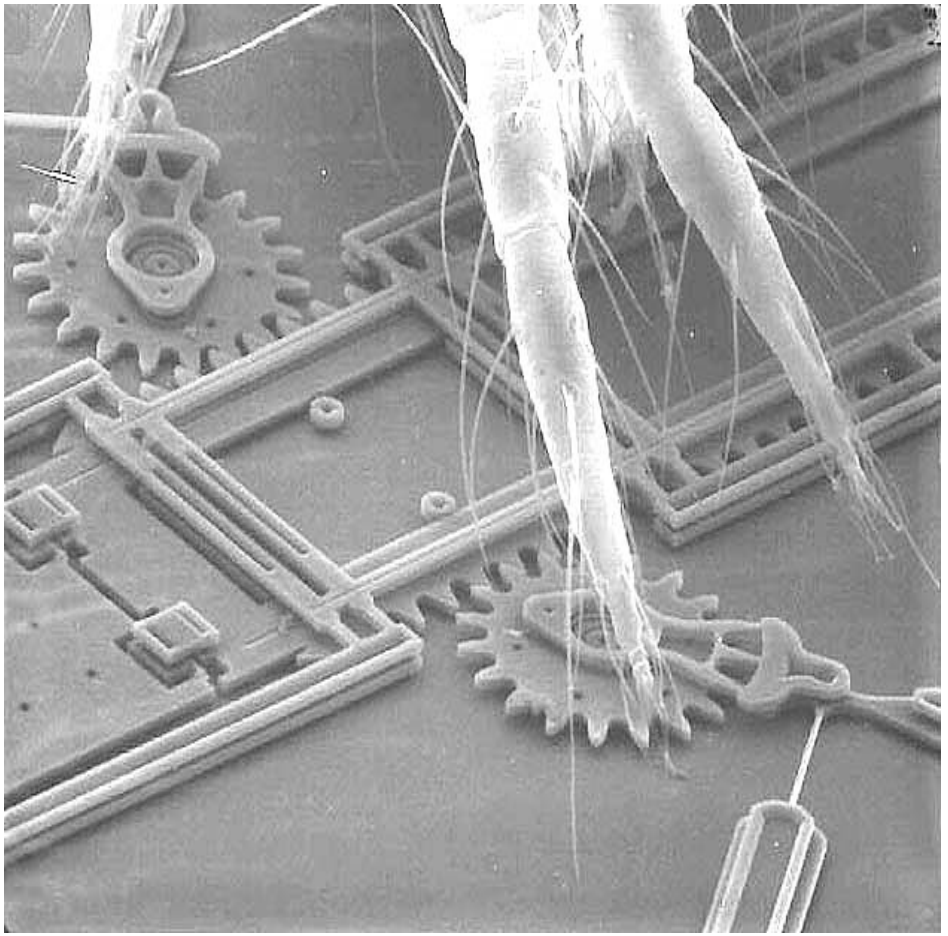
Buried conductors

- Buried under epitaxial silicon layer
- Used for long-term stability
- Sheet resistivity ca. 500 Ω/□



Thin film deposition

- Chemical Vapor Deposition
- LPCVD (low pressure CVD) temperatures in range 500-850 C
- PECVD (plasma enhanced CVD) temperatures below 400 C
- POLYSILICON
- Epitaxial silicon (slow deposition rate)



Chemical vapor deposition CVD

- Silicon films : Silane (SiH_4)
- Nitride films: Diclorosilane + ammonia

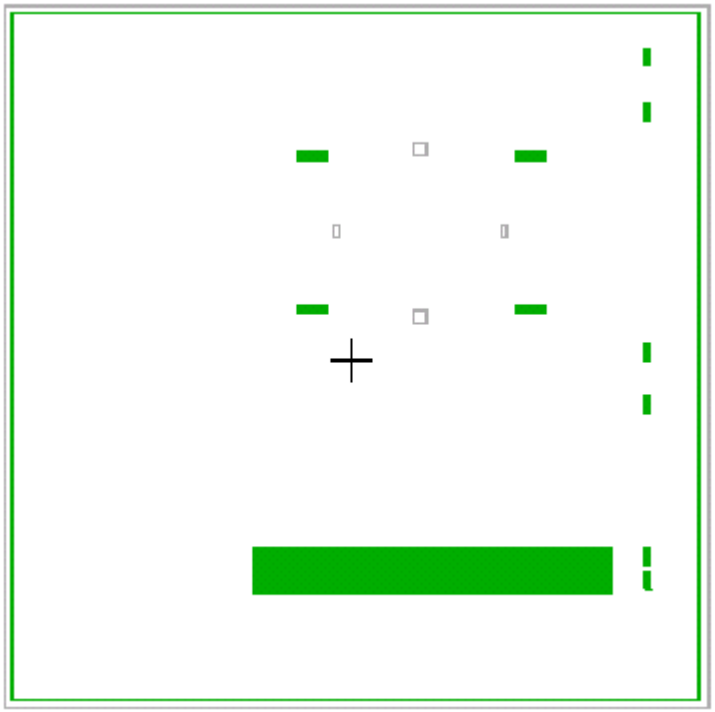
- LPCVD
  - Low pressure chemical vapor deposition
  - High temperatures (500-850 C)

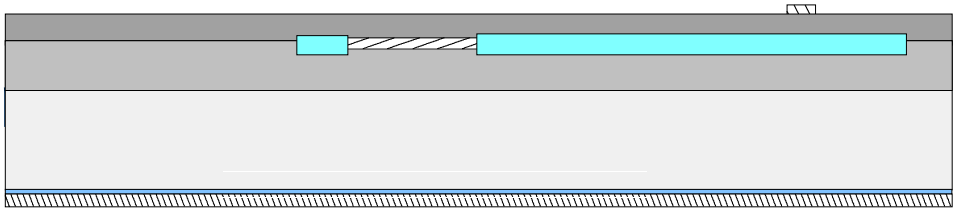
- PECVD
  - Plasma enhanced chamical vapor deposition
  - Low temperatures (to 40 C)

TIKOX mask (thick oxide)

- **Drawn areas define pattern of thick 4000 Å passi-vation oxide**
- **Used to isolate buried conductors and crossing metal lines, reduces spiking**

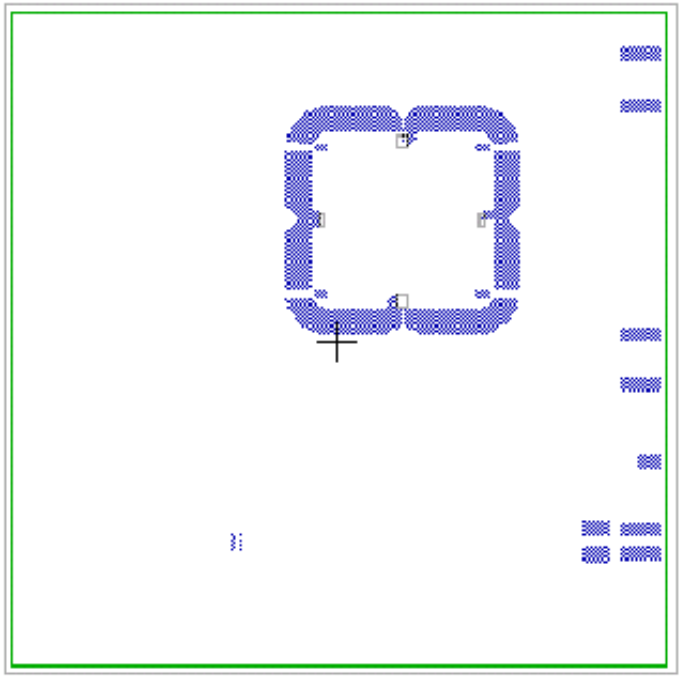
Grow thin oxide 1000 Å afte

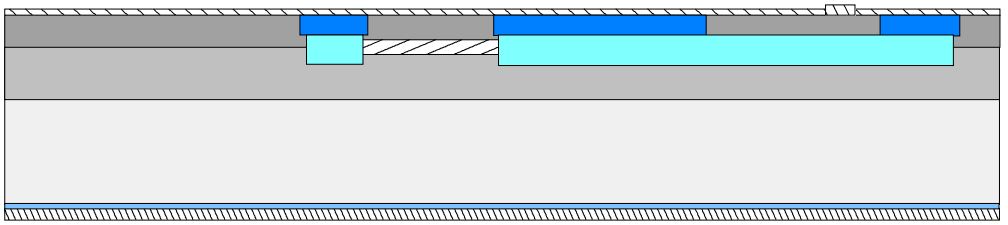




SUCON mask
(boron doped surface conductor)

- **Drawn areas define pattern of the surface conductors**
- **Used as vertical connection to BUCON and conductors to surface resistors**

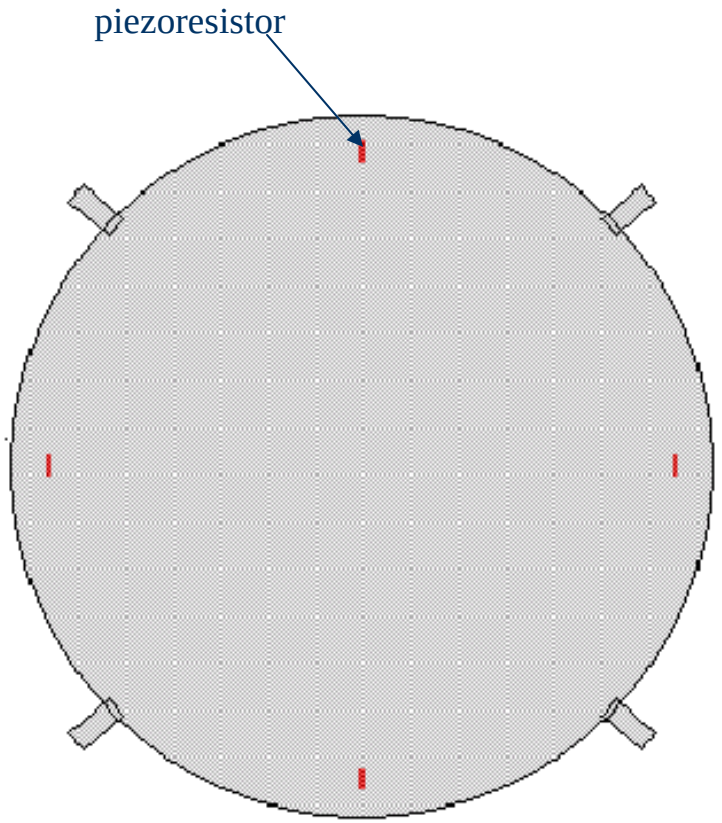




SURES-mask (boron doped surface resistors)

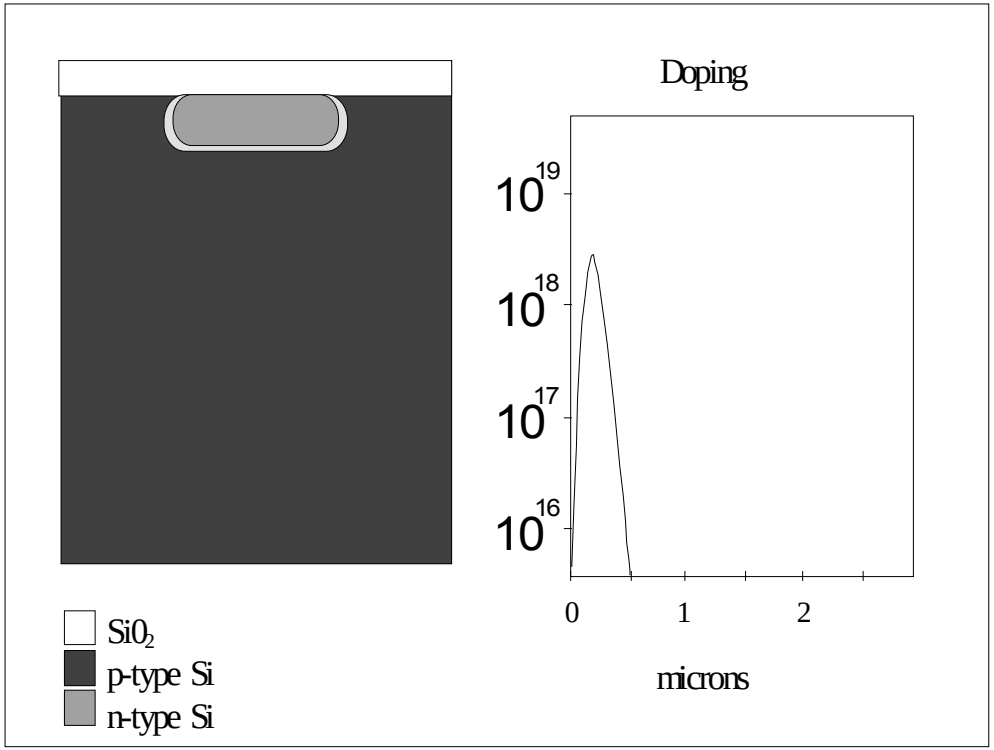
- **Drawn areas define pattern of the surface resistors**
- **Used as piezo-resistors for stress detection in thin membrane**

Lower p-doping concentration than conductors



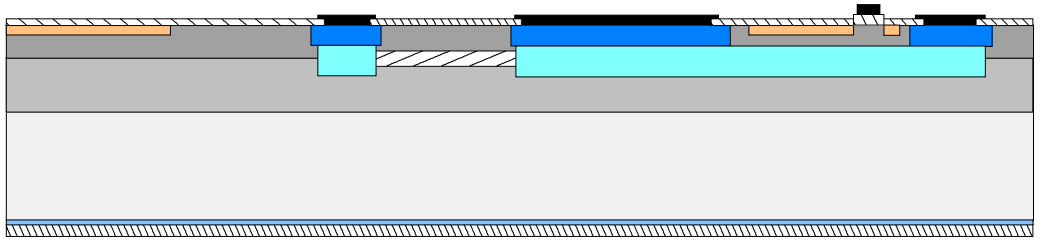
Surface Piezo-resistors

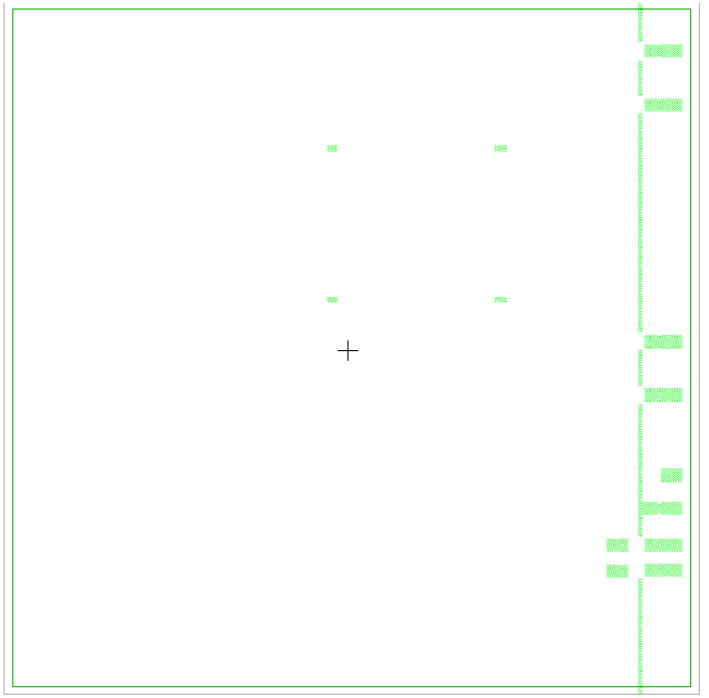
- Diffused into epi-layer surface
- Offers highest sensitivity
- Sheet resistivity ca. 800 Ω/□
- Particularly suited on thin springs



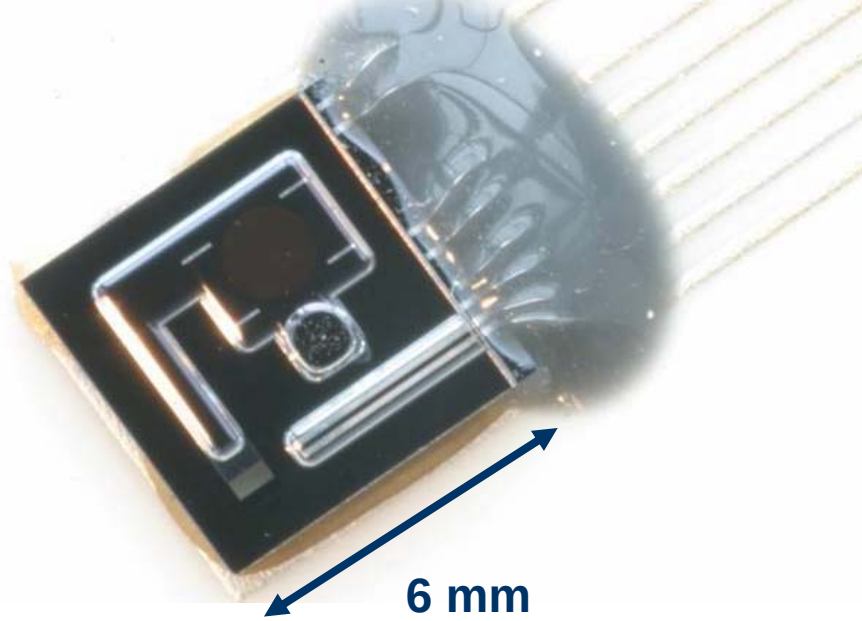
COHOL mask (oxide etch)

- **Drawn areas define the contact holes**
- **Used for electrical connection between metal and SUCON**

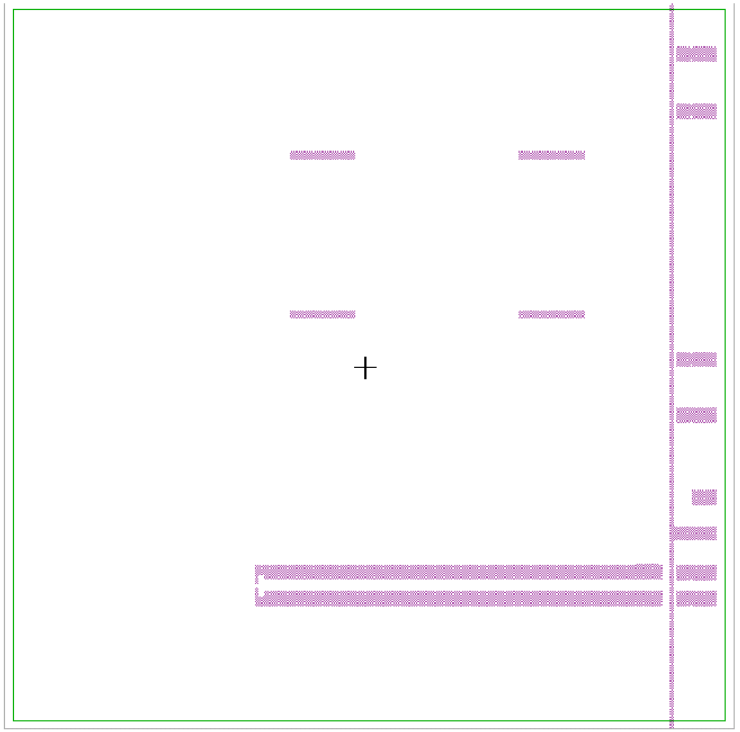




MCOND-mask

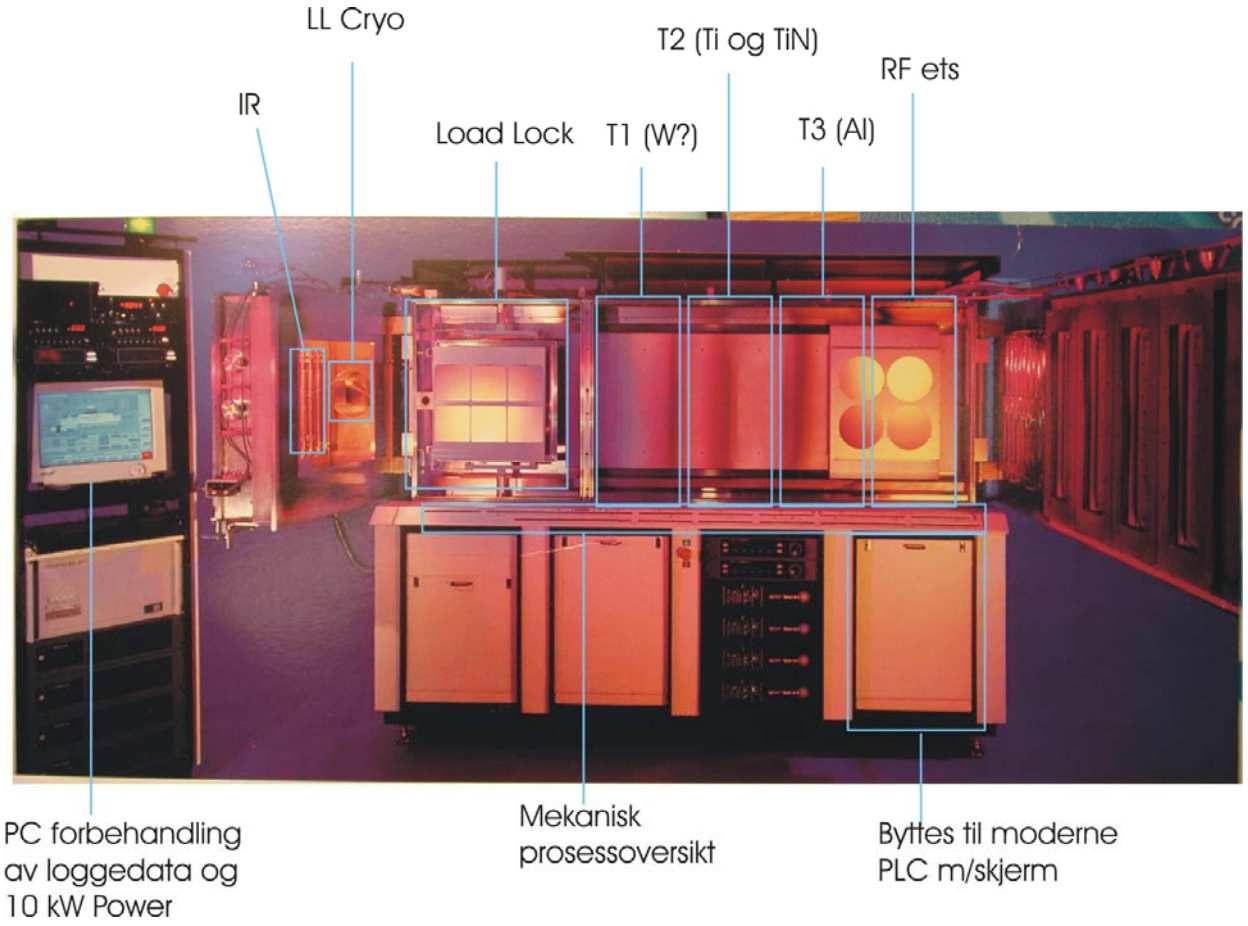


- **Drawn areas define the pattern of Aluminium wiring and bond pads**
- **Used for conductors in glass cavities and bond pads; in combi-nation with BUCON and SUCON**



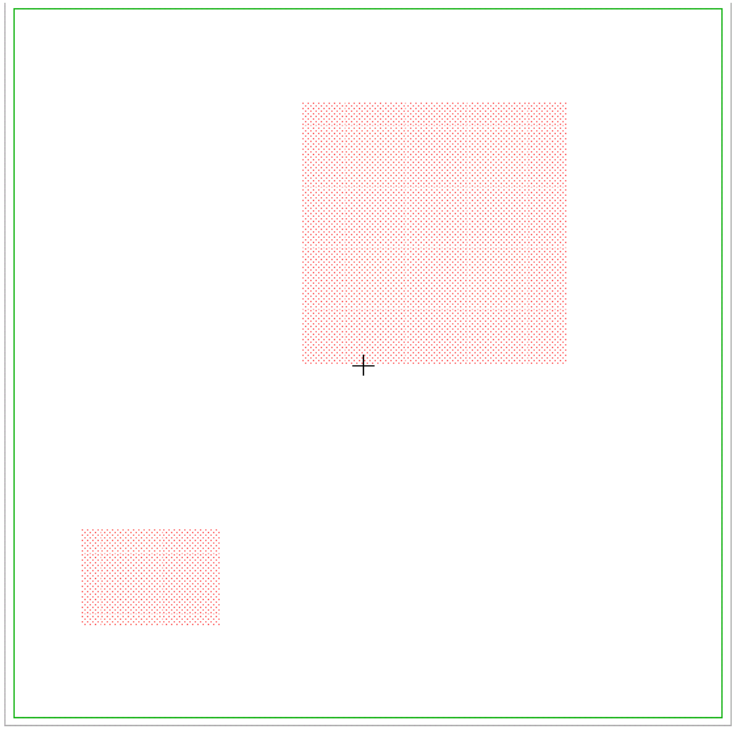
Physical vapor deposition PVD

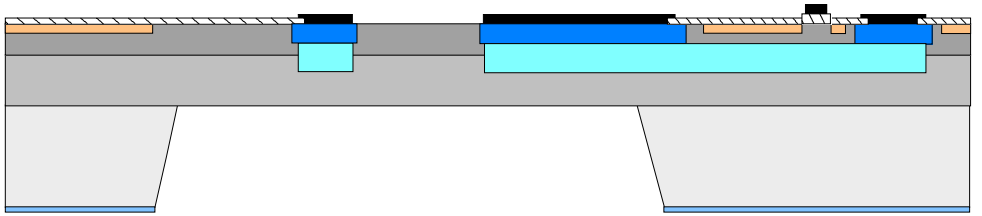
- Sputtering
  - Plasma (argon ionized in glow discharge)
  - Ions accelerated by electric field
  - Atoms from target knocked out
  - Deposit of target material on substrate
- High deposition rates
- Metallisation



BETCH mask

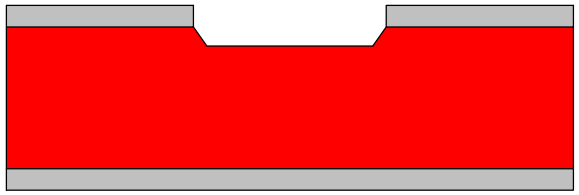
- **Drawn areas define the mask opening for the anisotropic backside etch**
- **Used for membrane, and through etch**



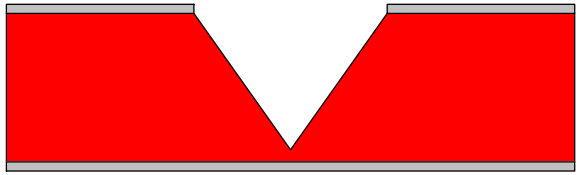


Wet anisotropic etch

SiO2 opened by photolithographic process

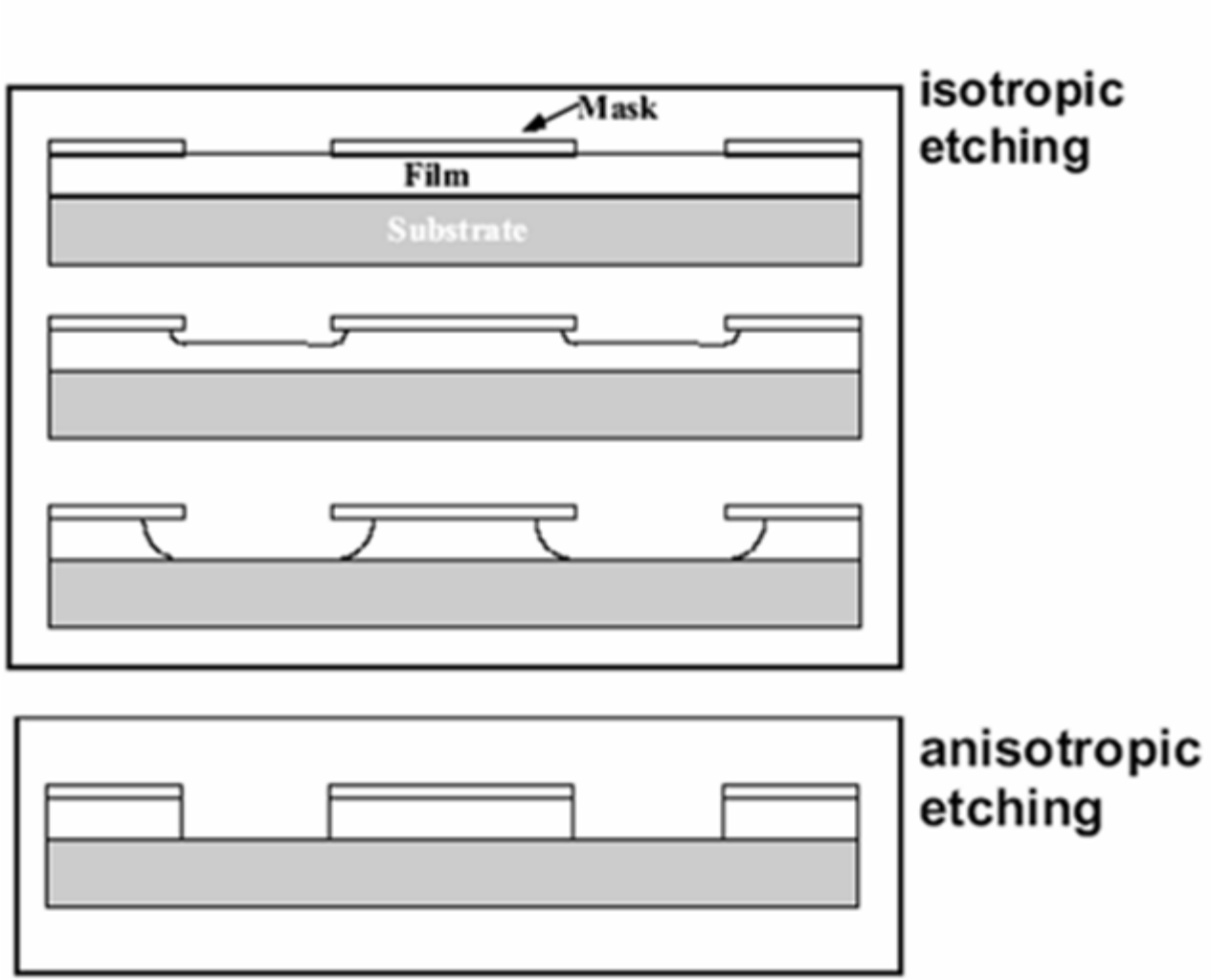


Short time in TMAH



Long time in TMAH

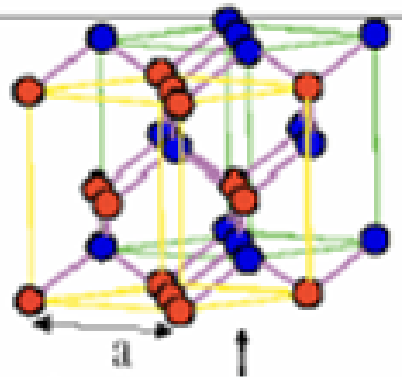
Isotropic vs anisotropic etch

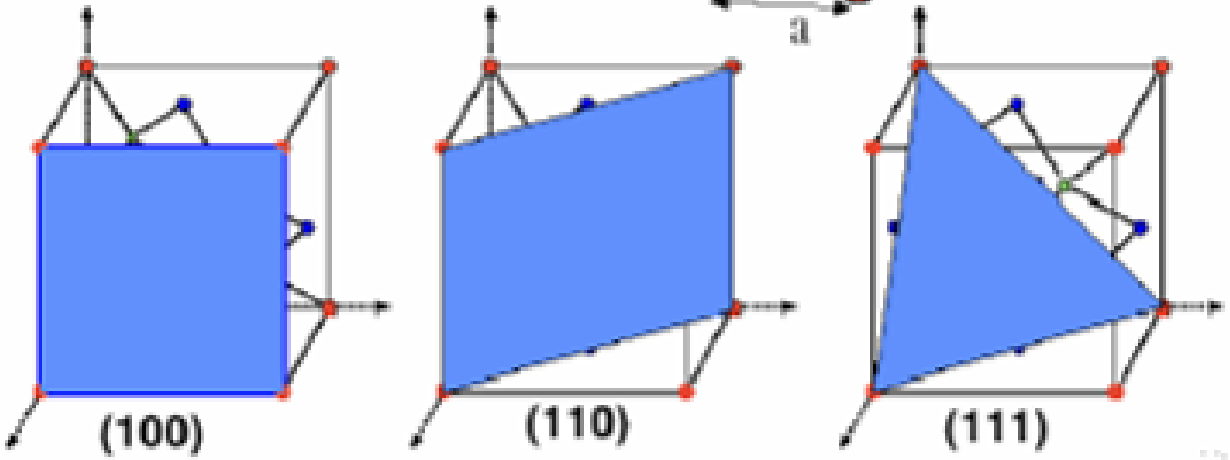


Silicon Etching

Crystallographic etching

- recall crystal lattice is face centered cubic (FCC), with two atom basis [at (0,0,0) and (1/4, 1/4, 1/4)]
  - two "interpenetrating" FCC lattices

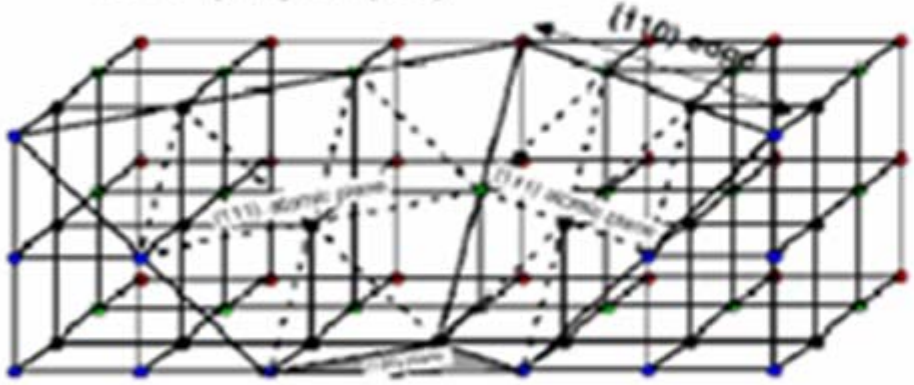




Silicon Etching

(111) planes

- (111) planes etch the slowest, tend to be cleavage planes
- 54.74° (1 1 1) wrt (100)

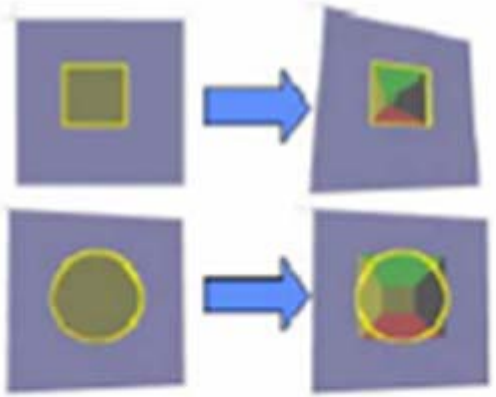


- edge of "pit" lines up with (110)

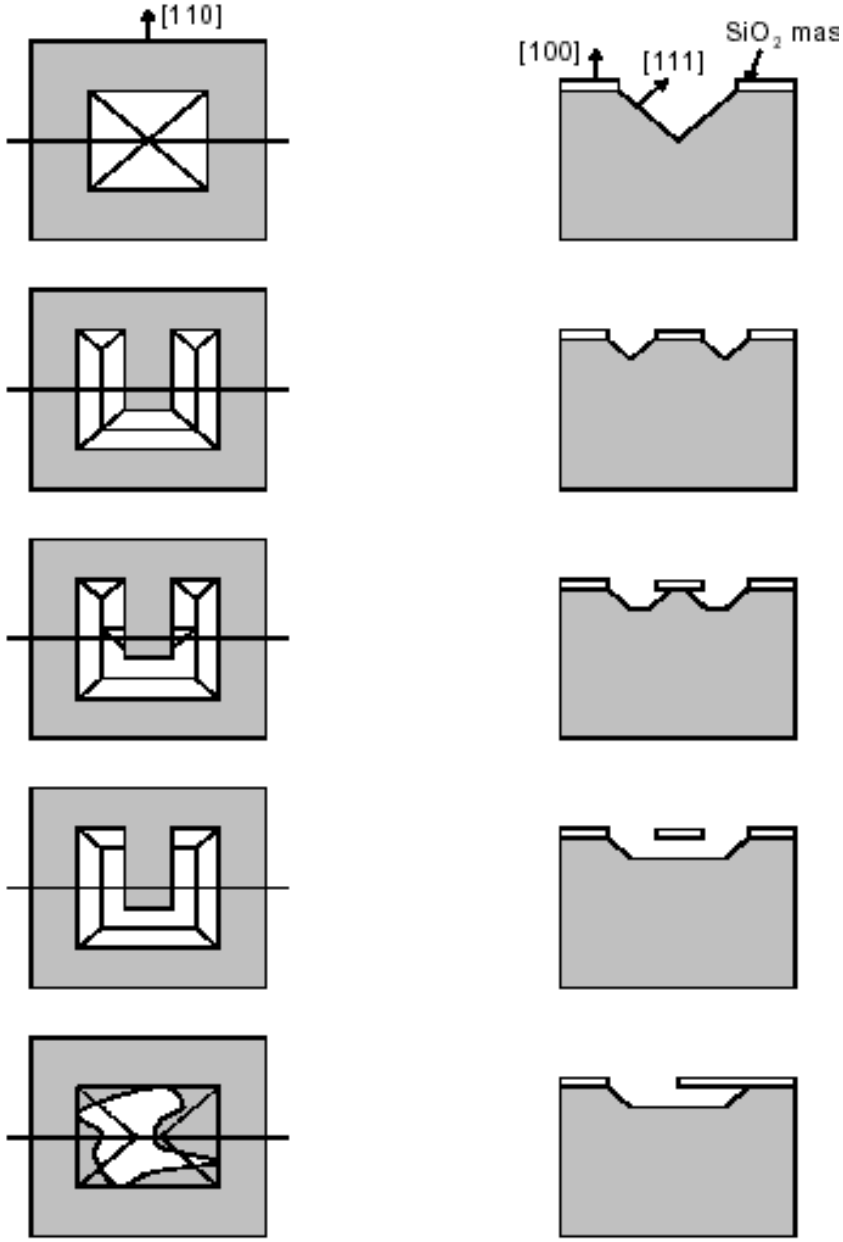
Silicon Etching

Masking

- assume bulk crystalline (100) silicon substrate combined with anisotropic etch
  - results in pyramidal shape
- bounding (111) planes can be reached using a variety of mask shapes
  - square mask opening, (100) wafer orientation, side of square is aligned to the (110) flat
  - what happens if you use a circular mask opening?
    - undercutting of the mask occurs until the (111) planes are reached
    - still forms a pyramidal pit!



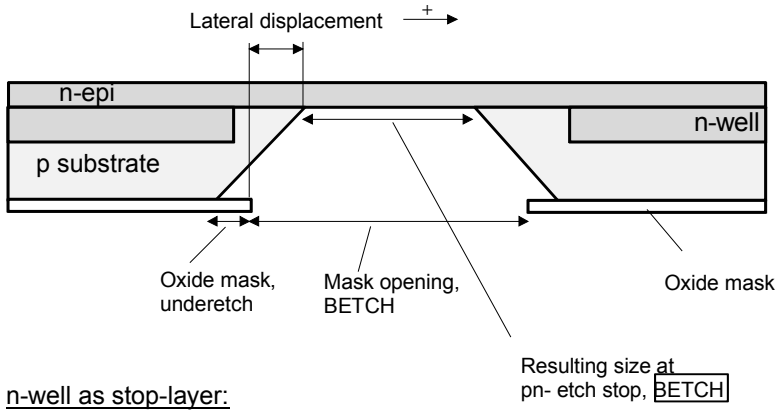
TMAH etch of silicon (100)



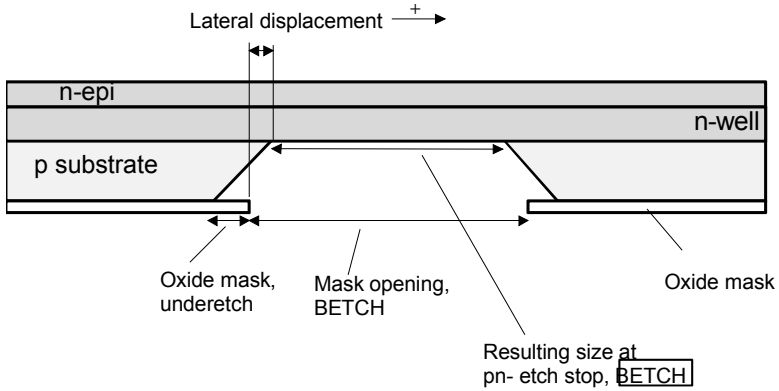
BETCH mask electrochemical etch stop

- **Layer BETCH: Seen in the cross section view: The size of the back-side etched mem-branes has to be calculated with the etch calculator**

Epi-layer as stop-layer:

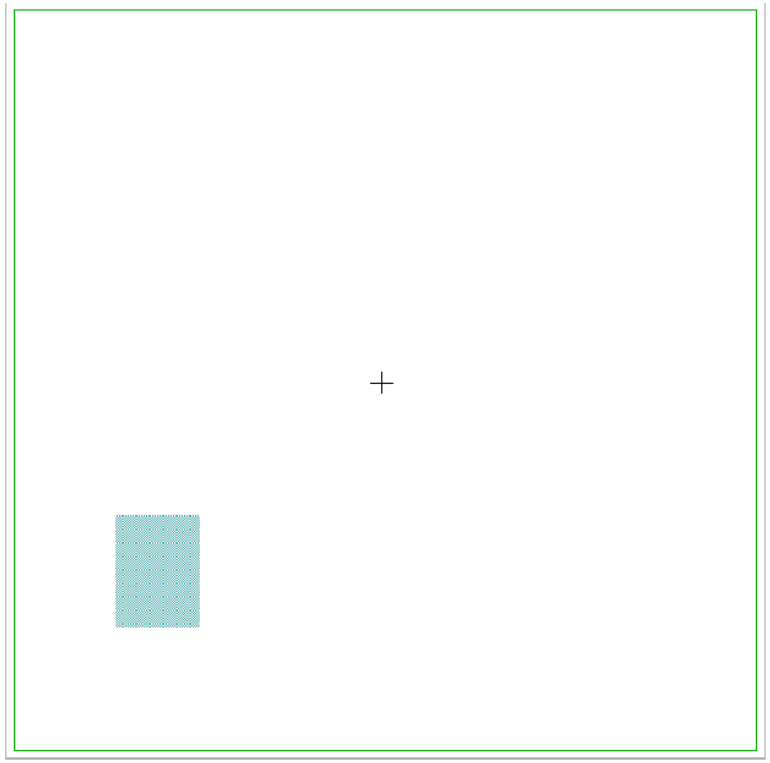


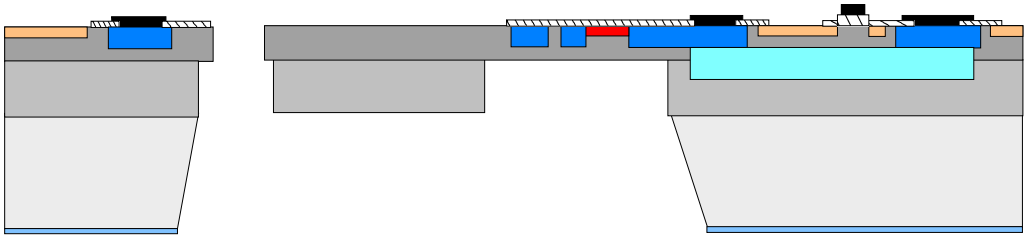
n-well as stop-layer:



RETCH mask

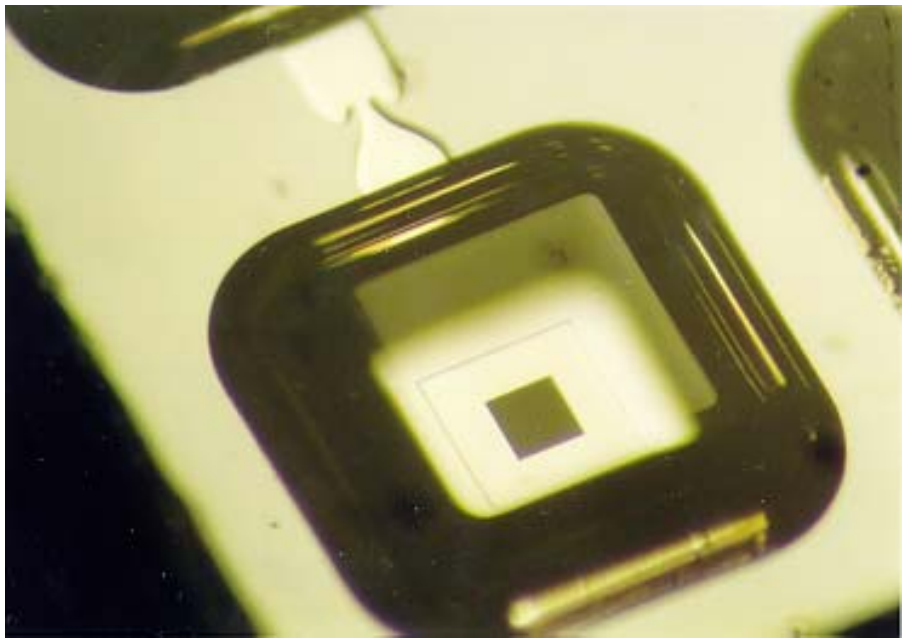
- **Drawn areas define the RIE etched area**
- **Used for definition of recess etch and through etch**

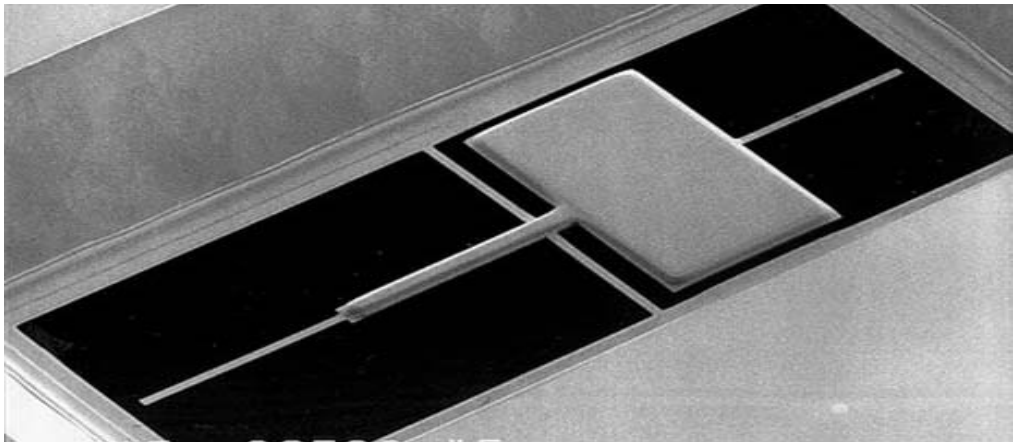




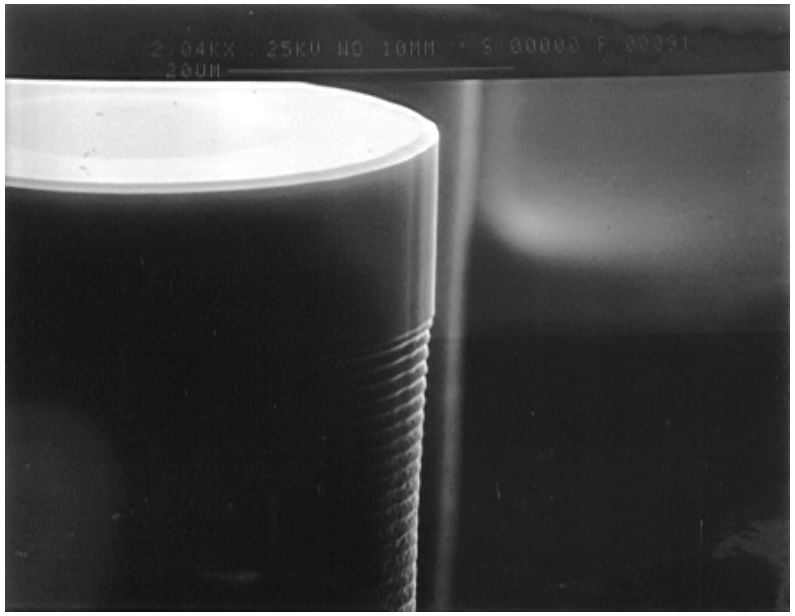
Dry Release Etch (RIE)

- Allows shallow channels in silicon surface
- Allows moving structures
- Allows fluid flow through wafer
- Through epi-thick membranes only (3μm)





Dry silicon etch



Bosch process -- photography by Alcatel

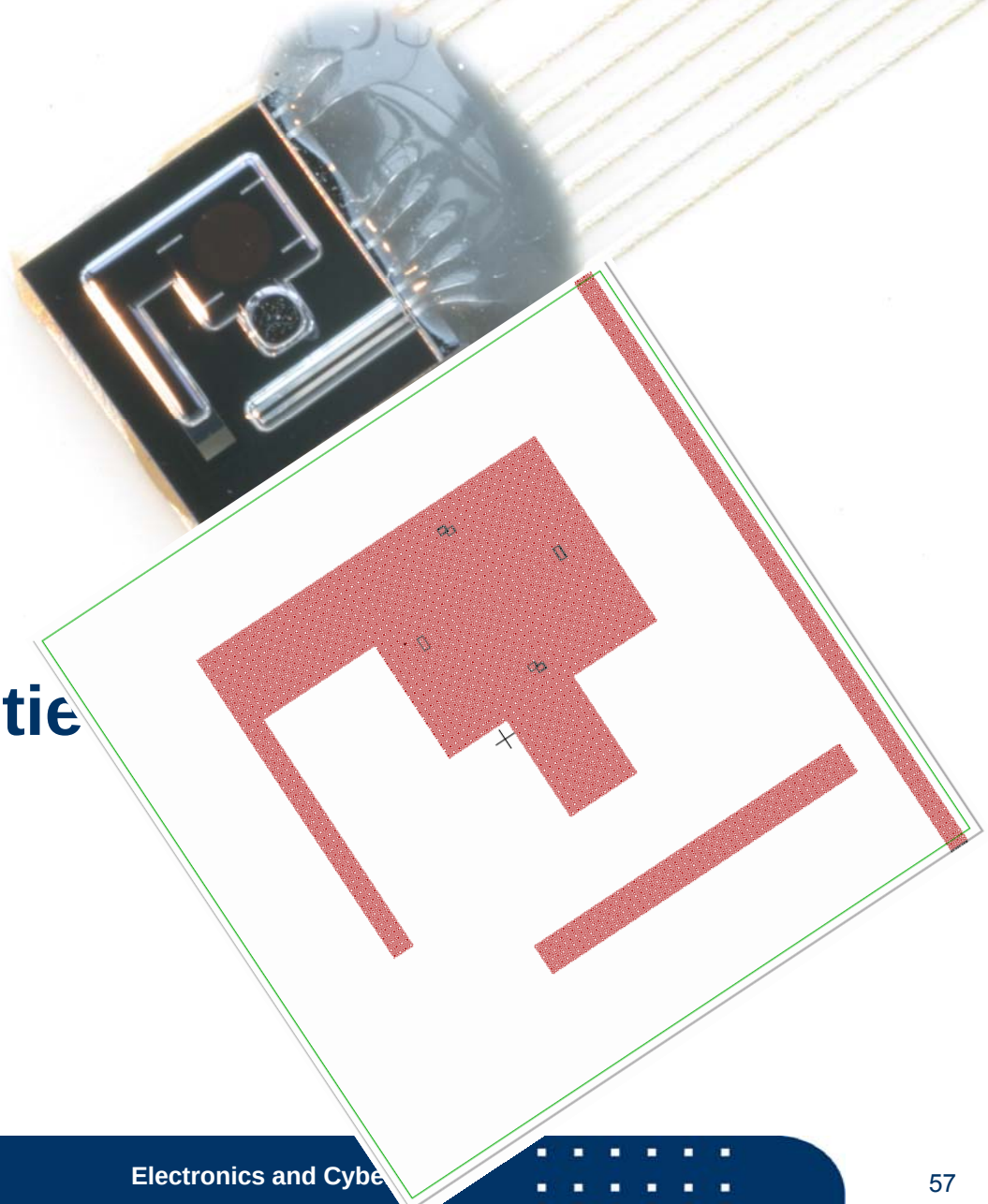
- Plasma assisted etching
- Simultaneous chemical reaction and physical directional bombardment etching
- Vertical (or controlled) walls
- Deep RIE
- Alternating:
- Etch of surface (SF_6)
- Deposition of polymer ($C_4 F_8$)

Alcatel AMS 200

- Production Tool
- Etch rates up to 20 µm/min
- Uniformity < ±5%
- ICP High Density Source
- Chuck: ESC or mechanical clamp
- Wafer sizes: 100 - 200 mm
- Dry Pumping Package

TOGE mask

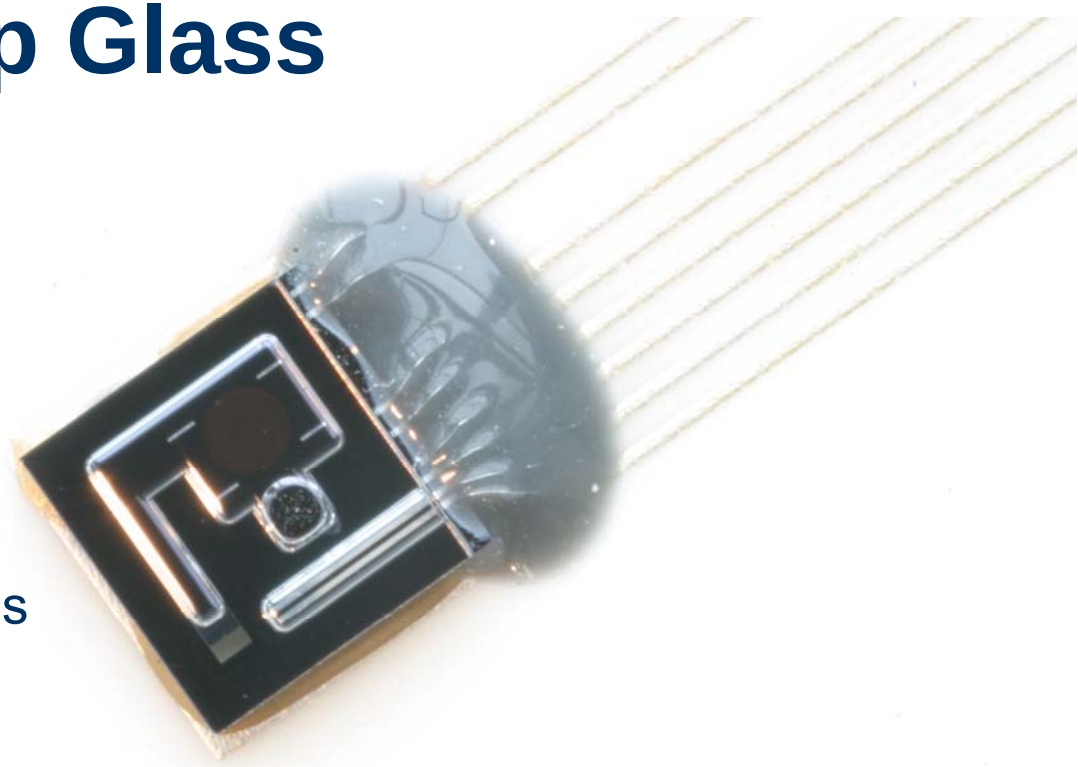
- **Drawn areas define the mask opening on the top glass facing the chip**
- **Used for channels, cavitie part of through etch**

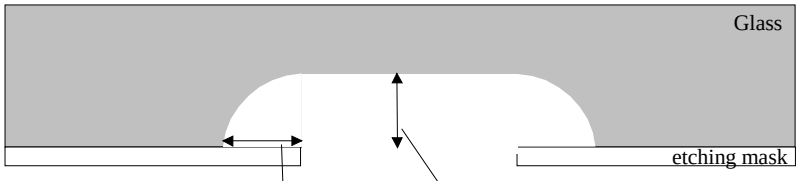


Top Glass

Single-sided structuring of top glass for:

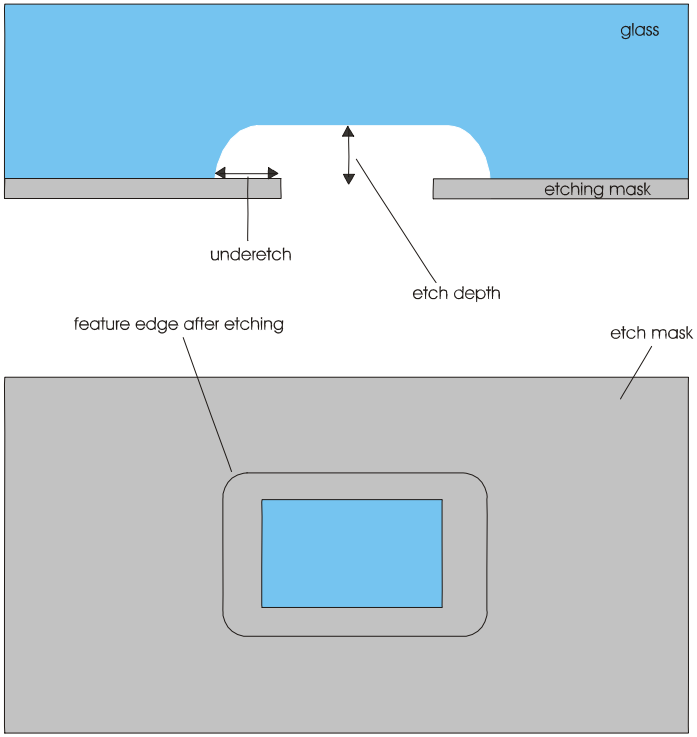
- reference cavity formation
- bond-pad area
- allow movement of structures
- gas/fluid channels





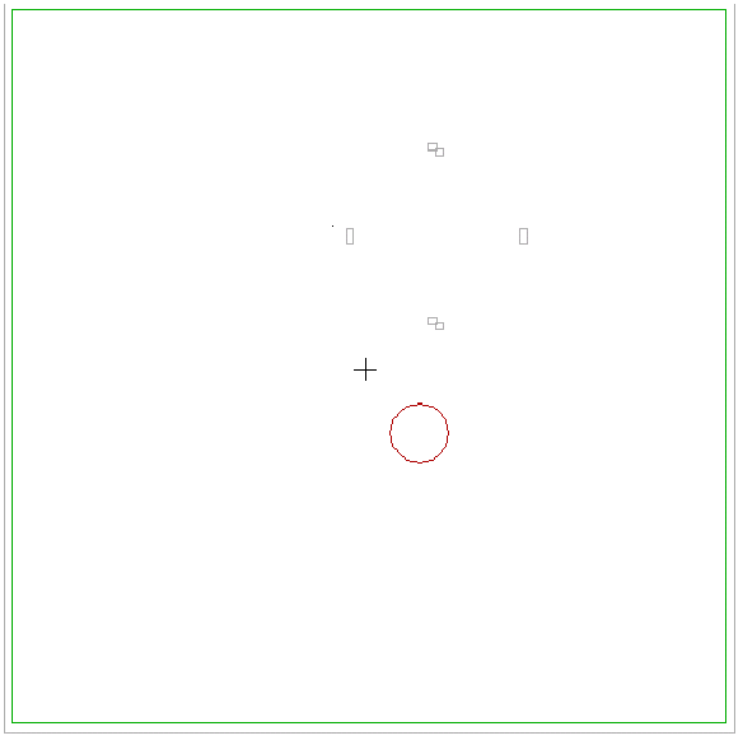
Glass etch

- **Glass etch: Cross section**
- **Isotropic glass etch causes a large under-etch, which has to be considered in design**



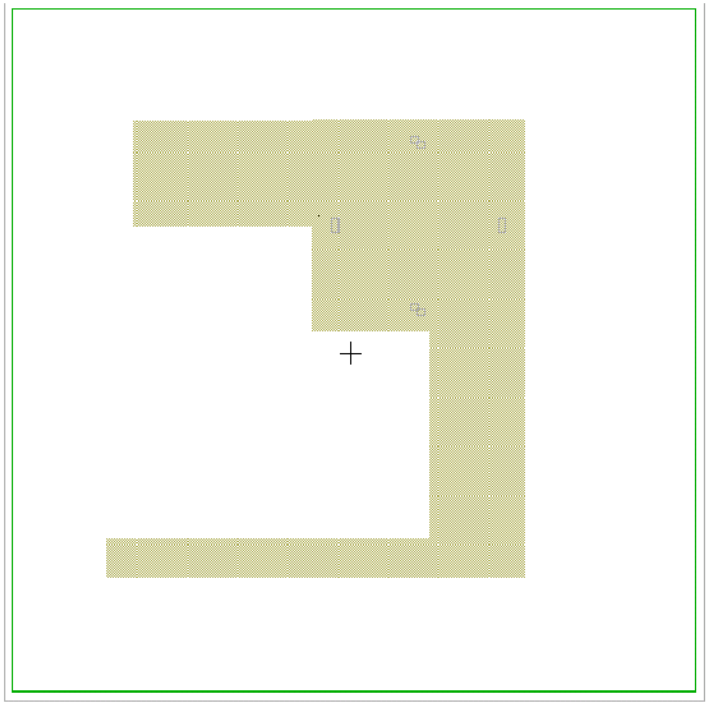
TOGEF mask

- Drawn areas define the mask opening of the isotropically etched top glass on the top side
- Used for through etch of top glass



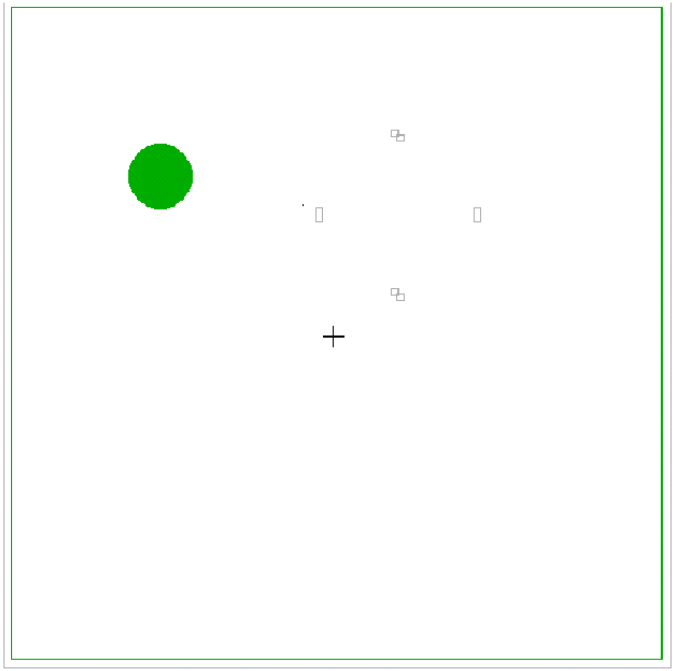
BOGEF mask

- **Drawn areas define the mask opening on the bottom glass facing the chip**
- **Used for channels, cavities, upper part of through etch**



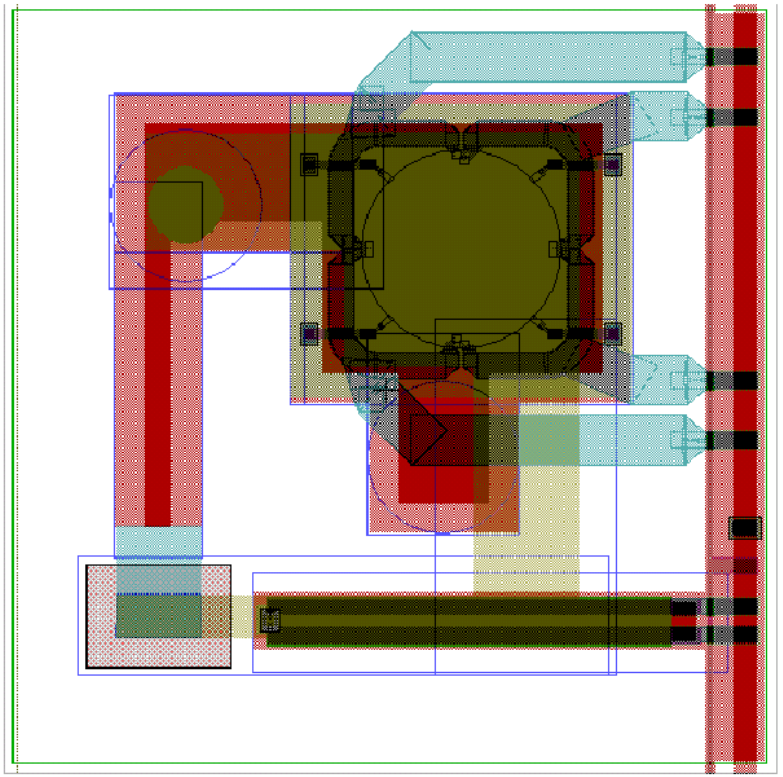
BOGEB mask

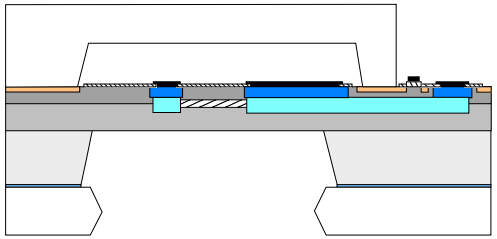
- **Drawn areas define the mask opening of the isotropically etched bottom glass on the bottom side**
- **Used for through etch**



All layers

Check again whether they are drawn according the *layout rules* and the *design limitations* !!





Measured flow rate

Stepper syringe pump