

UNIVERSITY OF OSLO

Faculty of Mathematics and Natural Sciences

Exam in: INF9425 Projects in Analog / Mixed Signal CMOS Construction

Day of exam: Thursday, June the 3rd, 2010.

Exam hours: 14:30 – 17:30.

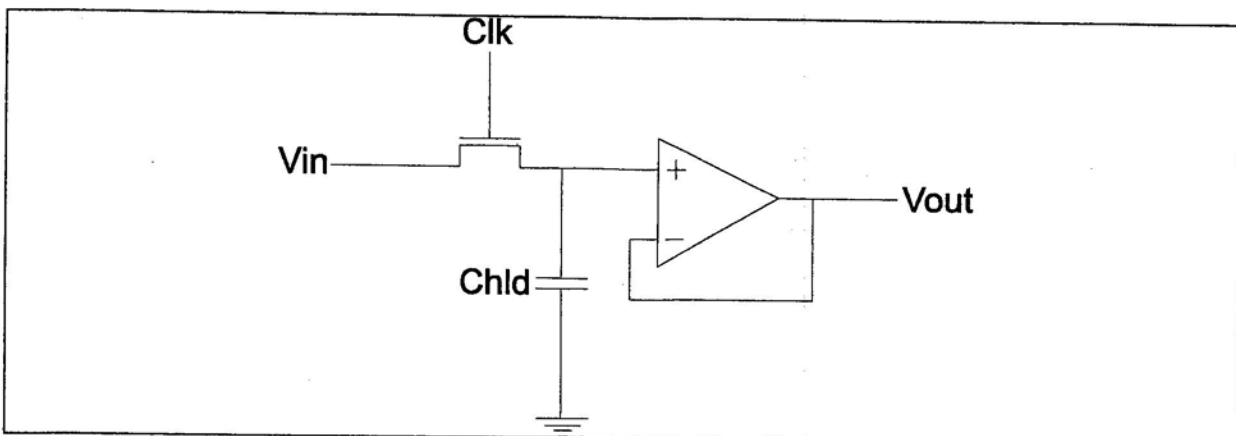
This examination paper consists of 5 pages.

Appendices: None.

Permitted materials: Any written material and calculator.

Make sure that your copy of this examination paper is complete before answering.

Oppgave 1 (Problem 1 has a weight of 17 % out of the total exam.)

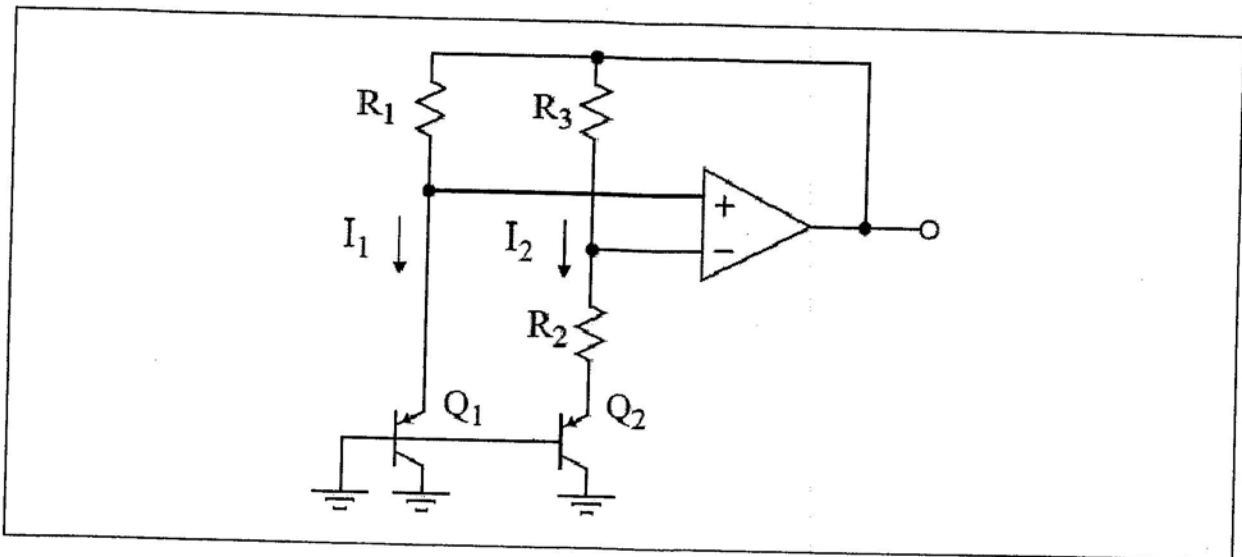


1 a) (weight 6 %)

Consider the Sample-and-Hold circuit above, with $C_{OX} = 1.92 \text{ fF}/(\mu\text{m})^2$, $V_{tn} = 0.5 \text{ V}$, and $W/L = 2\mu\text{m} / 0.5 \mu\text{m}$, supply-voltages $\pm 2.5 \text{ V}$ and the input signal varying between -0.5 V and 0.5 V . The switch introduces a hold step. What is the minimum size of C_{hd} if the absolute value of the offset due to charge injection should be no larger than 5 mV ?

1 b) (weight 6 %)

For the bandgap reference shown below, we have: $V_{EB1-0} = 0.65 \text{ V}$, $T = 300 \text{ K}$, $I_1 = 100 \mu\text{A}$. $\Delta V_{EB} = 59 \text{ mV}$, $J_1 / J_2 = 10$. Find the values of R_1 , R_2 and R_3 .



1 c) (weight 5 %)

Based on problem 1 b), what is the value of K? You may make relevant assumptions based on "Johns & Martin".

Problem 2 (Problem 2 has a weight of 21 % out of the total exam.)

2 a) (weight 6 %)

The following relationships are given for an SC-circuit with input voltage u_1 , output voltage u_2 and the capacitances C_1 and C_2 :

$$C_2 u_2[nT] = C_2 u_2[(n-1)T] - C_1 u_1[(n-1)T]$$

The signal at the input is sampled with the help of an ideal NMOS switch at time, $t = (n-1)T$. The clock signal for this switch is low at $T = nT$. Use the z-transform and write a transfer function for the circuit, in the z-plane.

2 b) (weight 10 %)

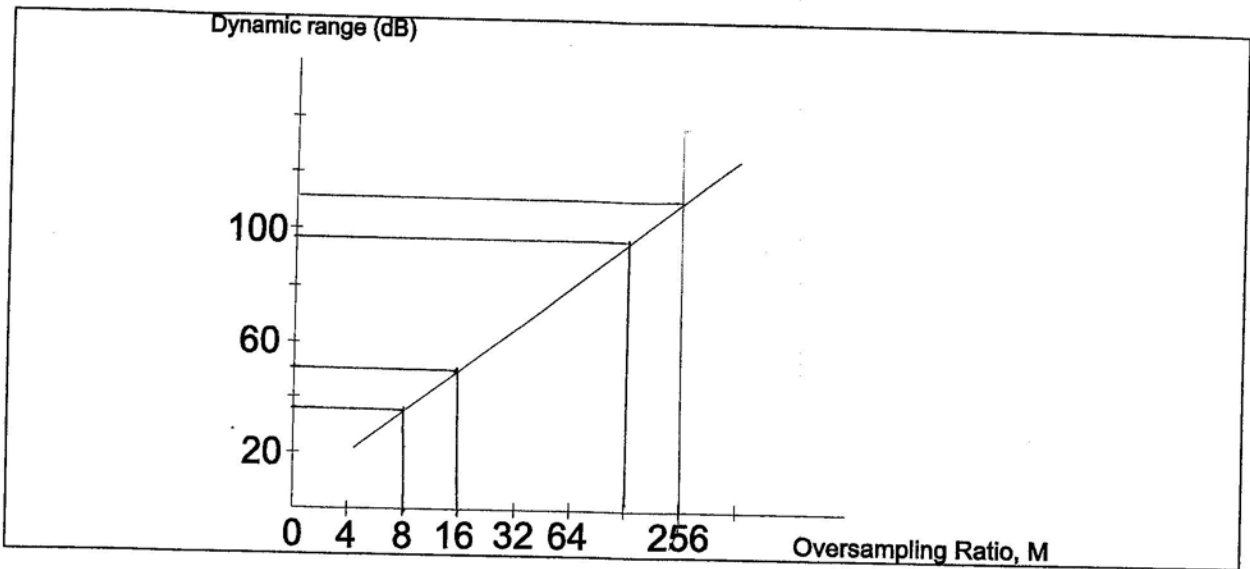
Given a SC-implementation of the following transfer function:

$$H(z) = U_2(z) / U_1(z) = (-C_1/C_2)(1/z-1)$$

Draw schematics for an SC-implementation of $H(z)$, as well as the similar RC-filter implementation.

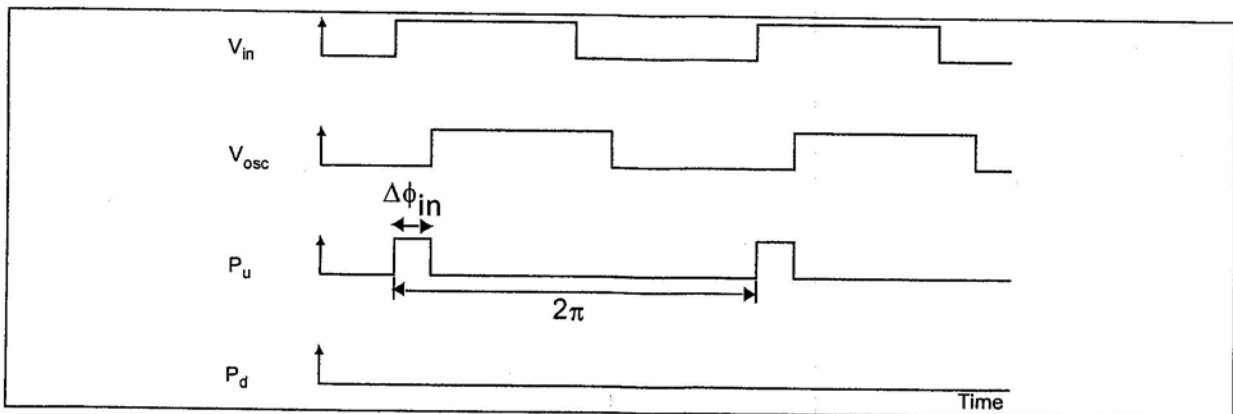
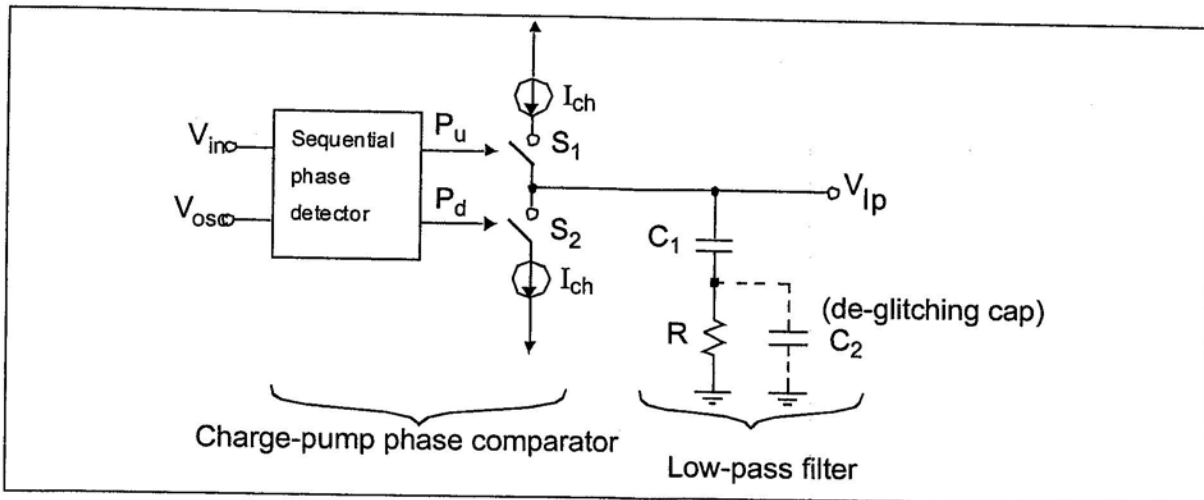
2 c) (weight 5 %)

Consider the illustration below, providing a relation between dynamic range and oversampling rate for an oversampling data converter. Which order, N , (N is a natural number) of the converter is probably belonging to the illustration. Explain your answer.



Problem 3 (Problem 1 has a weight of 26 % out of the total exam.)

Depicted below is a charge-pump phase comparator as well as some typical related waveforms.



3 a) (weight 10%)

Consider the information from the combination of the schematics and the waveforms and explain what is going on in the charge-pump phase comparator.

3 b) (weight 8 %)

Assume that the loop have a time constant of 100 cycles, or $2 \mu\text{s}$, and that the free-running frequency of the oscillator is 50 MHz. Let $K_{\text{osc}} = 2\pi \times 50 \text{ Mrad/s}$ and $I_{\text{ch}} = 10 \mu\text{A}$. $C_2 = 0$. A maximally flat group delay is desired. Design the components of the LP-filter.

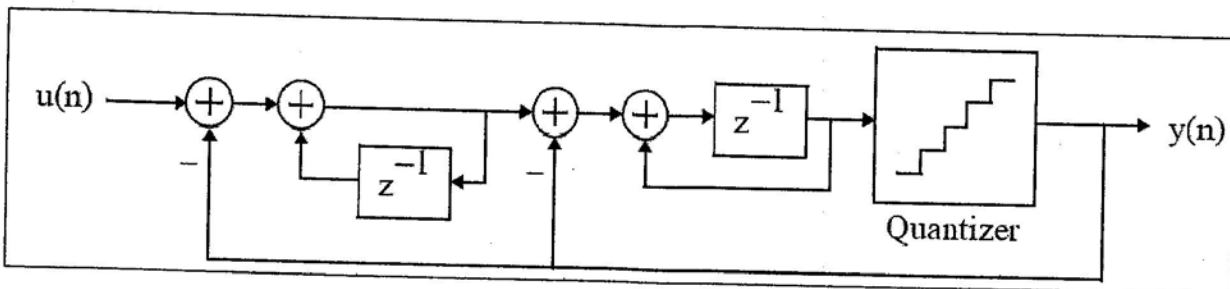
3 c) (weight 8 %)

Consider another case, when the time, $\Delta\phi_{\text{in}}$, is $0.1 \mu\text{s}$, $I_{\text{ch}} = 1 \mu\text{A}$ and $C_2 = 0$. What is the maximum change in the voltage across the capacitor, C_1 , during $\Delta\phi_{\text{in}}$, given that $C_1 = 2 \text{ nF}$?

Problem 4 (Problem 4 has a weight of 26 % out of the total exam.)

4 a) (weight 10 %)

Below you find a description of a $\Delta\Sigma$ modulator. Show how you can develop an expression for P_e (quantization noise power) for this topology, based on the formula below, and relevant assumptions from "Johns & Martin".



$$P_e = \int_{f_0}^{f_0} S_e^2(f) |N_{TF}(f)|^2 df$$

4 b) (weight 8 %)

Show how you may develop an expression for SNR_{max} , based on a) and $P_s = (\Delta^2 2^{2N}) / 8$. Explain what normally happens to a SNR_{max} when the oversampling rate is doubled, in this case? Explain.

4 c) (weight 8 %)

Our mathematical expression for SNR_{max} for this oversampling converter does not provide an upper limit for the sampling rate ("OSR"). How would this be for a practical implementation in CMOS? Explain.

Problem 5 (weight 10 %)

For a given power budget, performance may drop when migrating to newer technologies. This can complicate analog design. Could you please explain?

In the previous problem a part of an oversampling converter was shown. Could you say something about oversampling converters and how they are affected by technology scaling, when compared to Nyquist converters?

Good luck!