Q.1 12.13 of Razavi's

Q.2 12.14 of Razavi's

Q.3 12.16 of Razavi's

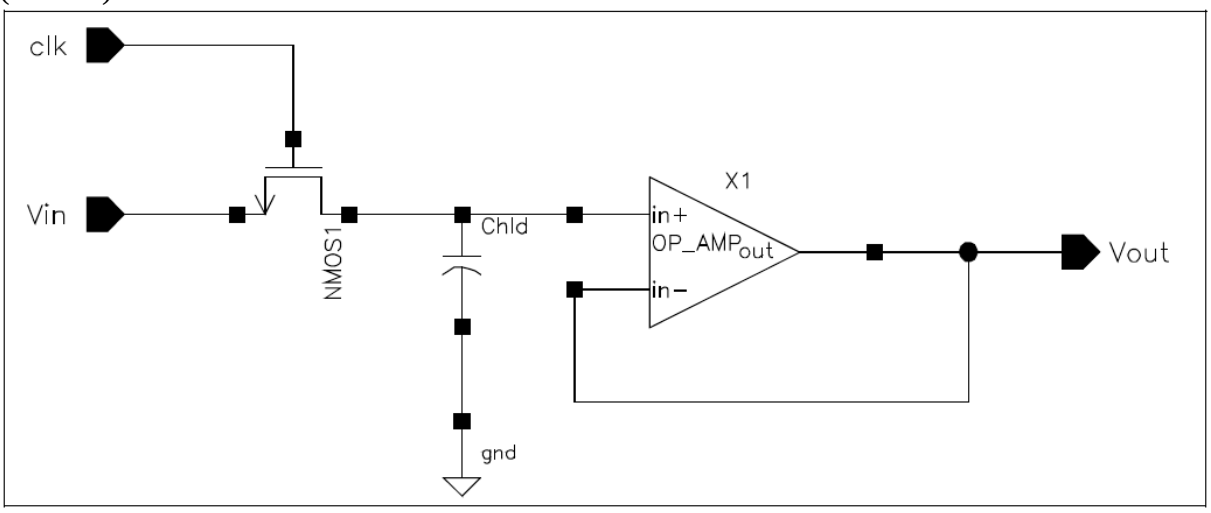
Q.4

In Figure 12.8, if C_H = 2 pF and V_{DD} = 3V, what is the sampling noise power, max SNR and resolution (number of bits)?

Repeat the question if you have a differential sampling switch.

Q.5

a) A simple sample-and-hold ("S/H") circuit is shown in the schematics below. It is implemented in a standard 90 nm CMOS technology, having a supply voltage of 1.0 V. The clock signal ("clk") varies between 0 V and 1 V, while a sine wave varying between 0.3 V AND 0.5 V is connected to the input ("Vin"). Make a sketch depicting the two previously mentioned signals as well as the voltage across the hold capacitor ("Chld"), and the output ("Vout").



b) Consider the S/H from 4 a) and describe certain problems that may arise if Chld is made very small.