Q.1 *14.1 of Razavi's*

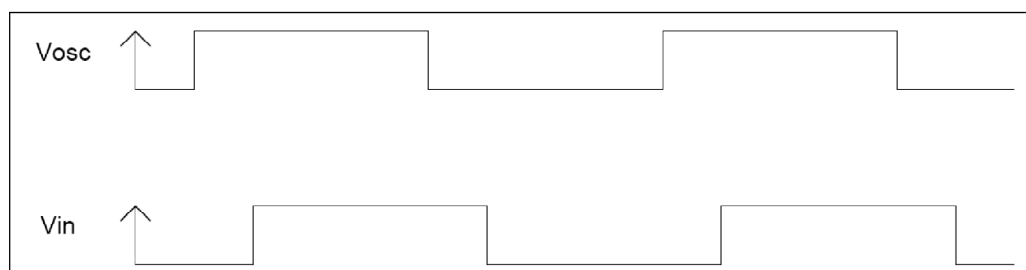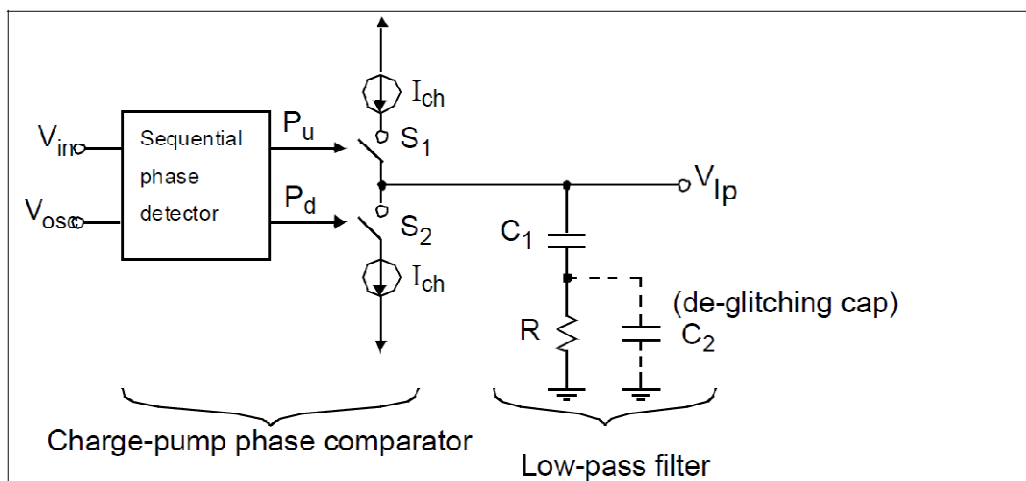*Q.2* *14.2 of Razavi's*

Q.3 *14.3 of Razavi's*

Q.4 *14.13 of Razavi's*

Q.5 *15.2 of Razavi's*

Q.6

a)   A *charge-pump phase comparator* for integrated PLLs is shown below. There is also an example of two waveforms related to it, V_{osc} and V_{in}. Draw the related P_u and P_d waveforms and explain briefly how they relate to V_{in} and V_{osc}.

b)   CMOS technology still continues toward finer scale geometries. Do you think that this development could make any influence on the choice of PLL architectures? Could you explain why and how?