INF4420 / INF9425 INF4420 - Projects in analogue/mixed-signal CMOS design

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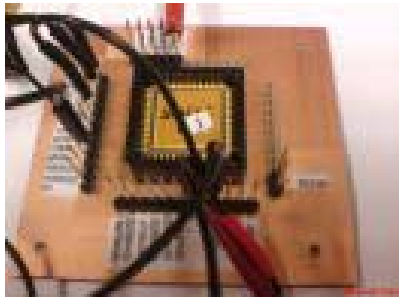

INF4420 / INF9425 – V2011:

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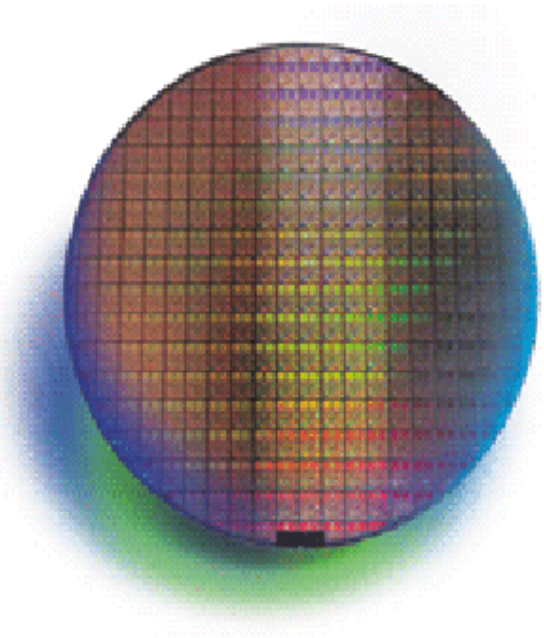
- Martin Severin Orrebakken Haugland
- Kin-Keung Lee – ”Kody”
- Snorre Aunet

INF4420 / INF3410

Outline – Tuesday 25th of January

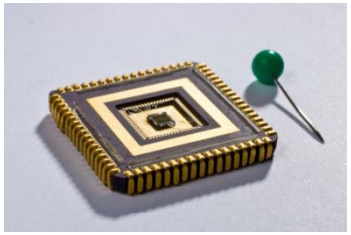
- Practical issues
- Learning goals
- Design project, tools and methods
- Syllabus
- Very brief introduction to various circuit building blocks

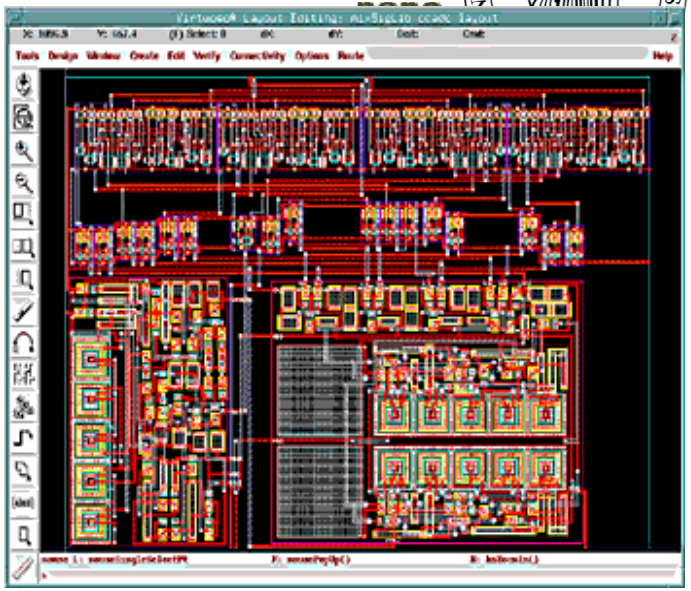
  (sample-and-holds, bandgap references, switched capacitor circuits, Nyquist- and oversampling data converters, oscillators phase-locked loops, CMOS technology etc)

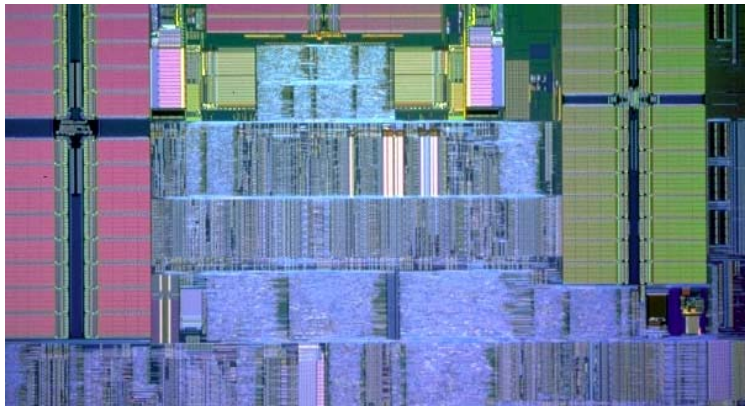


CMOS Integrated Circuits?

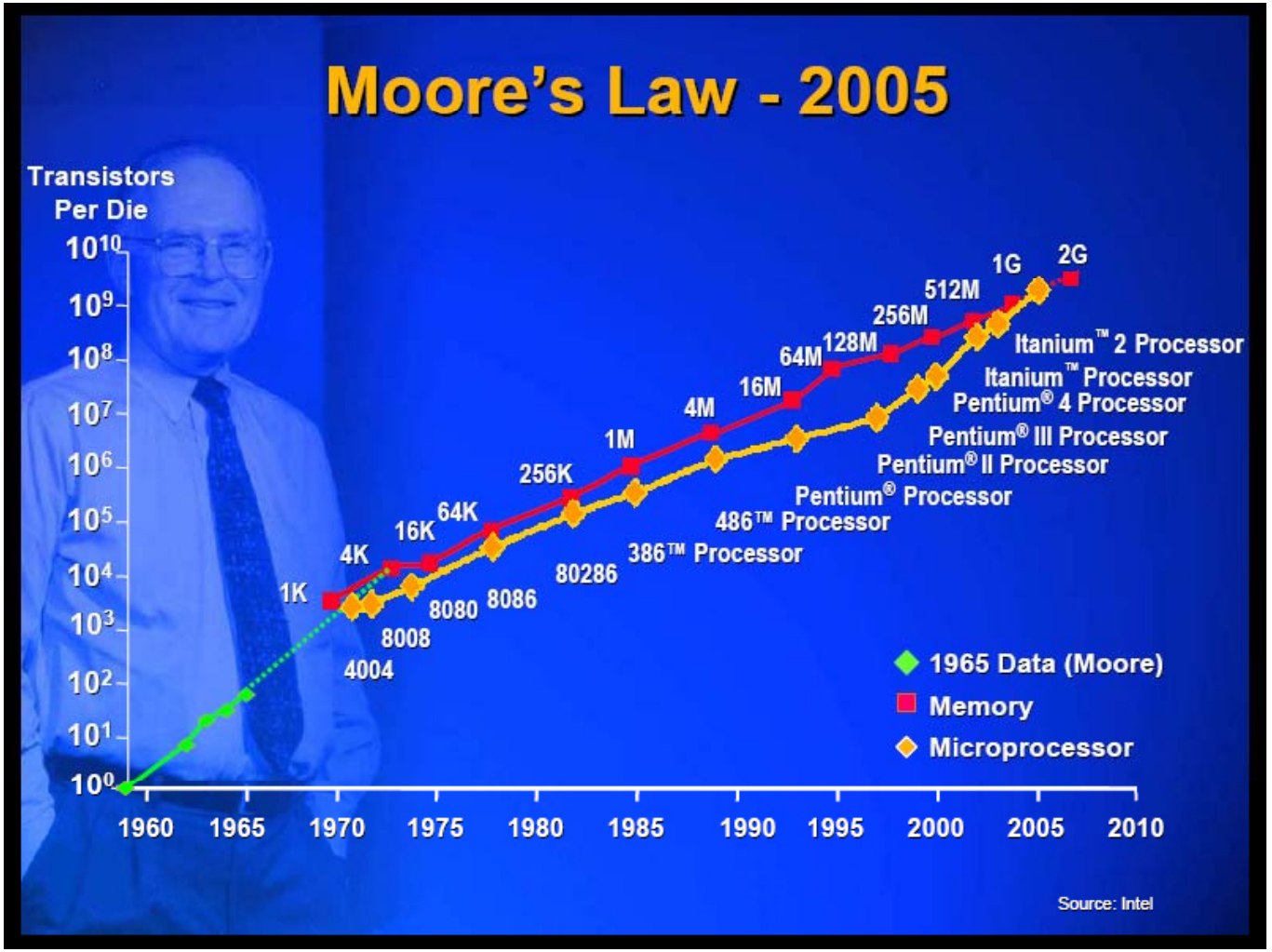
- Digital circuits exploit mainly transistors and interconnect
- Mixed-Signal (Digital AND Analog) also use resistors, capacitors and inductors
- Work-horse of modern Information Technology

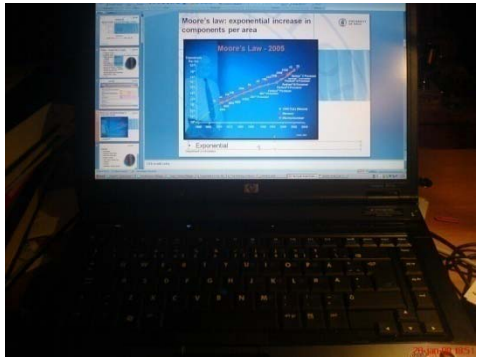






Moore's law: exponential increase in components per area





- Challenge to integrate analog and digital (mixed-signal)

http://www.uio.no/studier/emner/matnat/ifi/INF4420/

- **INF4420 - Projects in analogue/mixed-signal CMOS design**
- Course content - Learning outcomes - Admission - Prerequisites - Overlap - Teaching - Exam information - Other information - Contact us
- **Facts about this course:** Credits: 10 Level: Foundation course at bachelor's level Teaching semester: Every spring semester Examination semester: Every spring semester Language of instruction: English if requested by exchange students, otherwise Norwegian Administrated by: Department of Informatics (Ifi)
  Detailed course information - Current and previous semesters: Spring 2011
- Spring 2010
- Spring 2009
- Spring 2008
- Spring 2007
- Spring 2006
- Spring 2005
- Spring 2004
- Autumn 2003
- **Course content**
- The course provides the know-how and skills needed to design analogue and mixed-signal integrated circuit modules using modern program tools. The main focus of the course is complex systems such as data converters (A/D, D/A) and phase-locked loops (PLL). An introduction is given to CMOS technology and methods in order to implement passive components such as transistors, condensers and coils. In addition, matching, optimisation and noise deflection are all key aspects. The execution of project tasks will be a central part of the teaching.
- **Learning outcomes**
- Students will have the skills needed to design an integrated mixed-signal circuit in CMOS using modern design tools.
- **Admission**
- Students who are admitted to study programmes or individual courses at UiO must each semester register which courses and exams they wish to sign up for in StudentWeb.
- **International applicants**, if you are not already enrolled as a student at UiO, please see our information about admission requirements and procedures for international applicants.
- **Prerequisites**
- **Formal prerequisites**
- In addition to fulfilling the basic entrance requirements to higher education in Norway, applicants have to meet the following special admission requirements:
- Mathematics R1 or Mathematics (S1+S2)
- The special admission requirements may also be covered by equivalent studies from Norwegian upper secondary school or by other equivalent studies. Read more about special admission requirements.
- **Overlap**
- 10 credits against INF3420 - Prosjekter i analog/mixed-signal CMOS konstruksjon. 6 credits against INF239. 3 credits against INF238.
- **Teaching**
- 3 hours of lectures and 2 hours of working in groups every week. Some of the teaching will be given as supervision in labs.
  There are obligatory tasks to be handed in and passed in order to be admitted to take the exam.
- **Exam information**
- Individual grading of project assignment (50%)and final exam (ca 50%). Oral/written.
- **Assessment and grading**
- Course grades are awarded on a descending scale using alphabetic grades from A to E for passes and F for fail.
- Course Auditor: Per Olaf Pahr
- **Other information**
- The subject is regarded equal to INF3420 - Prosjekter i analog/mixed-signal CMOS konstruksjon when practicing exam regulations.
- **Contact us**
- **Department of Informatics (Ifi)**
- **Visiting address:**
  Informatics builidng, First floor, room 2316, Gaustadalléen 23
- **Visiting hours:**
  Monday-friday 12:00-15:00
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  NO-0316 Oslo
- **Phone:** +47 22 85 24 10
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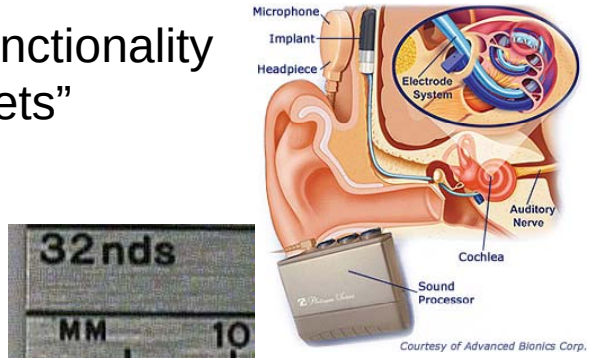
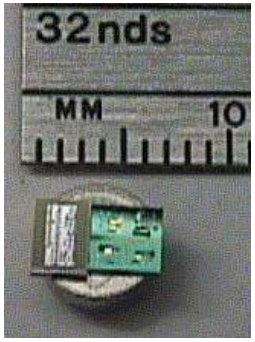
-

Why ASICs (Application Specific Integrated Circuits) ??

- Advantages:
  - Reduced size
  - Improved performance and functionality
  - Easier to hide ”company secrets”
  - Reduced cost
  - Reduced power consumption
  - Less radiated noise

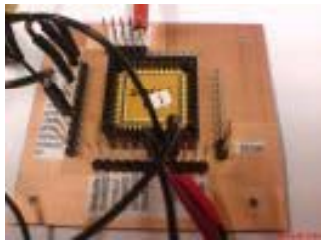


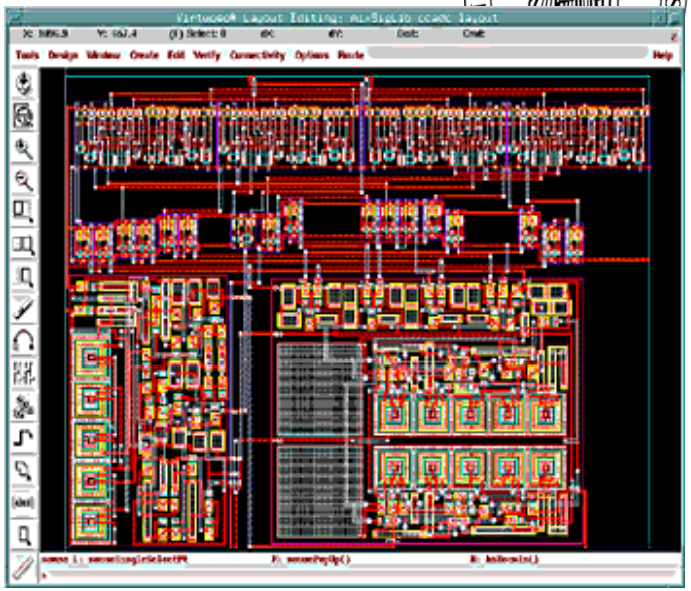


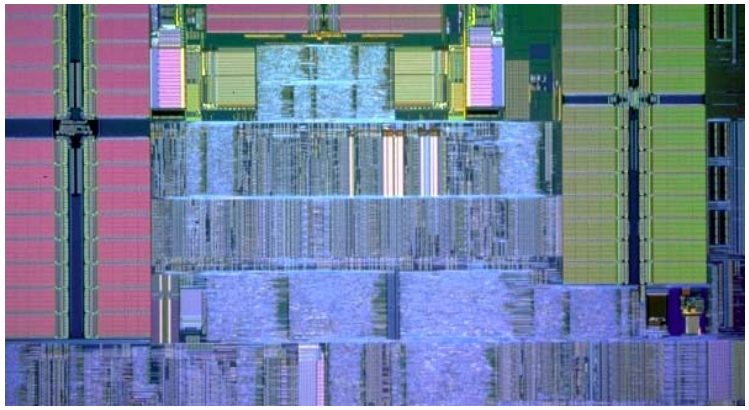
- Disadvantages:
  - Increased start-up cost
  - High power density - Heat
  - Hard to find top competence
  - Time consuming development and production
  - Substantial ”Time-to-market”

What is an integrated circuit?

- Transistors
  - Several options
- Capacitors
  - How to implement
  - Linearity
- Resistors
  - How to implement
  - Area
- Inductors
  - How to implement
  - Quality factor
- Parasitic components
  - Calculate
  - Minimize

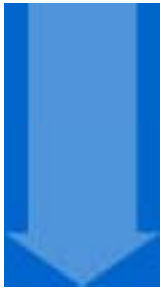


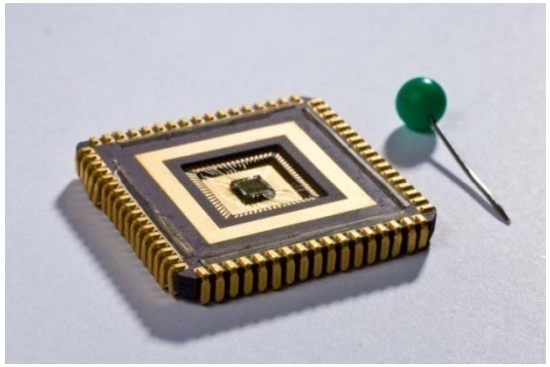




Design methods; digital from HDL, full custom analog

- Digital systems:
  - Automatic synthesis
    - VHDL
    - Schematic
- Analog systems:
  - Module based
  - Full-custom





Low Power..

KISEL ELLER MJUKVARA

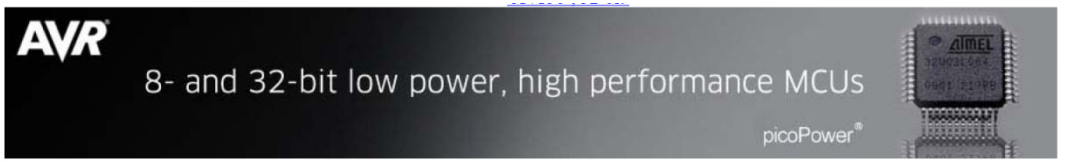
Och till slut – är pendeln på väg att svänga från mjukvara till hårdvara? Idag handlar allt om energiförbrukning och i valet mellan programmerbara system och "hårda" ASIC-lösningar är det ingen större tvekan om vad som är energieffektivast. Och det blir samtidigt allt lättare att konstruera med hjälp av färdiga IP-block.

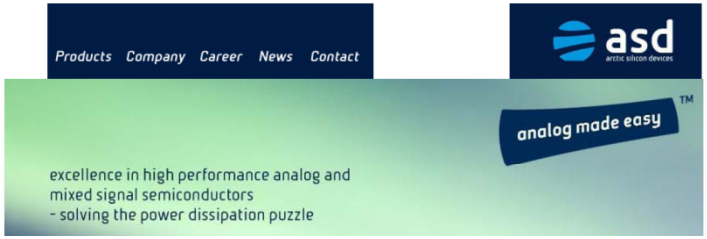
Om det här hade jag ett långt och intressant samtal med Kathryn Kranen, vd för EDA-företaget Jasper. Kathryn Kranen hävdar med bestämdhet att hon ser allt fler halvledarkonstruktioner, inte färre. Till och med företag som inte tidigare gjort egna kretsar tar nu steget till kisel för att klara sina krav.

Det här är något som vi snart kommer att återkomma till. Ännu så länge saknas hårda data, men de exploderande mjukvarukostnaderna gör att hårdvara inte nödvändigtvis är dyrare än mjukvara. Hårdvarukonstruktörernas disciplin och effektiva verifiering kanske gör att det till slut lönar sig med hårdvara.

Men det återstår att se. ■■■

Göte Fagerfjäll





Mandatory design project

- Design and implement mixed-mode circuit:
  - Example: ADC, SC-filter, PLL, DAC (2008)
  - System for automatic removal of mismatch (2009)
  - SAR Analog-to-Digital Converter (2010)
  - Milestones during the process
  - 2 persons in each group
  - Teaching assistant, Kin Keung Lee, will follow up
- Write a project report
  - LaTeX or similar
- Submission: Early in May
- Counts 40 % in the final grading (exam 60%)

Challenge in 2008: Digital-to-Analog Converter (”DAC”)

INF 4420 – Prosjektoppgave: Digital til Analog Omformer – 2008 (SA 18.02.2008)

1 Introduksjon

Det skal lages en data-konverter av typen ”Two-stage balanced current DAC”, illustrert i figur lengre ned.

- DAC’en skal ha en oppløsning tilsvarende minimum 6 bit.
- Anta i utgangspunktet at maksimalt et en spenningsreferanse og en strømkilde er tilgjengelig, og dermed ikke trenger konstrueres.
- Digitalt ord inn (unipolart) skal være på følgende form, forutsatt 6 bit oppløsning: 00…0, 00…1, …, 11…1.
- Utgangssignalet skal være nedad begrenset til 0.3 V og oppad begrenset til 0.7 V.
- Positiv forsyninsspenning (”Vdd”) er 1.0 V. Negativ forsyningsspenning (”Vss”) er 0 V.
- Maksimal DNL: +/- 1 LSB
- Kretsen slik den er i kretsskjema mangler buffer, for eksempel i form av en spenningsfølger, som gjør den i stand til å drive en kapasitiv last i form av I/O-celle (”pad”). Det er frivillig evt å lage et slikt buffer, ikke påkrevd.
- Søk en best mulig konstruksjon ut fra effektforbruk og areal.

2 Milepæler

For å sikre gjennomføring innenfor tidsrammen settes det delmål med oppgitte frister. Studentene har ansvaret for å få disse delmålene godkjent av gruppelærer.

11/3-08 Det skal leveres inn et dokument på inntil 2 sider som beskriver hvordan dere har forstått oppgaven, og skisserer hvordan dere har tenkt å løse den.

25/3-08 Testbenk for systemet skal være ferdig.

6/5 08 Design og simuleringsarbeidet for hele kretsen skal være ferdig for både skjema og utlegg, og LVS inkludert. Gruppelærer skal eventuelt godkjenne at kretsen fungerer tilfredsstillende på bakgrunn av demonstrasjon.

3 Krav til prosjektgjennomføring

Målsetningen er å lage en digital-til-analog omformer (”DAC”) med minimum 6 bit nøyaktighet. Gruppens medlemmer må i fellesskap gå gjennom oppgaven og fordele arbeidsoppgaver, men samtlige skal kunne stå inne for, og redegjøre for konstruksjonen. Arbeidsfordelingen mellom deltakere i prosjektet skal rapporteres. Under følger noen tilleggsopplysninger og nærmere spesifisering.

3.1 Praktisk arbeid

1. Komplette skjema, ned til transistornivå, skal tegnes. Det skal lages symboler for de ulike byggeblokkene som inngår i det komplette systemet som utgjør dataomformeren.

2. Benytt statistiske (”Monte-Carlo”) simuleringer for å verifisere funksjonalitet under prosessvariasjoner.

3. Når simuleringsresultatene er tilfredsstillende skal det tegnes fysisk utlegg (”layout”) for hver av byggeblokkene, som til slutt settes sammen til den komplette kretsen.

4. Det er en del spesielle utfordringer i forbindelse med design av systemer som inneholder mixed-signal (analoge og digitale) byggeblokker. Identifiser slike utfordringer og foreta tiltak for å løse disse.

5. Benytt Layout Versus Schematic (”LVS”) for delkretser og totalsystem, for å verifisere samsvar mellom kretsskjema og tilsvarende utlegg, og lette konstruksjonen. Resultatene fra LVS skal vedlegges prosjektrapporten.

4. Krav til rapport.

Sentralt i bedømmingen av arbeidet vektlegges rapportens kvalitet. Skriv den i LaTeX eller tilsvarende program. De ulike fasene av prosjektet skal dokumenteres. Dette inkluderer bla plot av skjematikk samt simueringsresultater som demonstrerer funksjonalitet hos de ulike byggeblokkene. LVS rapporter fra Cadence hører også hjemme her. Begrunn og dokumenter de ulike valgene dere har gjort. Dette inkluderer blant annet dimensjonering av aktive og passive komponenter, problematikk omkring matching, tiltak mot støy, samt layout.

Husk at bidrag fra de ulike gruppemedlemmene skal være identifiserbare.

Rapporten skal også inneholde informasjon om hvor Cadence-filer ligger tilgjengelige for etterkontroll av resultater.

Sensor bedømmer rapporten. Derfor er det viktig at denne er mest mulig forståelig for sensor.

5. frister for innlevering.

Prosjektet skal være avsluttet og rapport innlevert senest 9/5-2008 kl. 12:00. Alle gruppene må presentere resultatene av prosjektet etter innlevering. Følg med på fagets hjemmeside for evt andre beskjeder. Vurdering baseres på en bedømming av arbeidets kvalitet, og rapportens kvalitet, slik dette framgår av sistnevnte. En prosentuell score vektes inn i endelig karakter for faget.

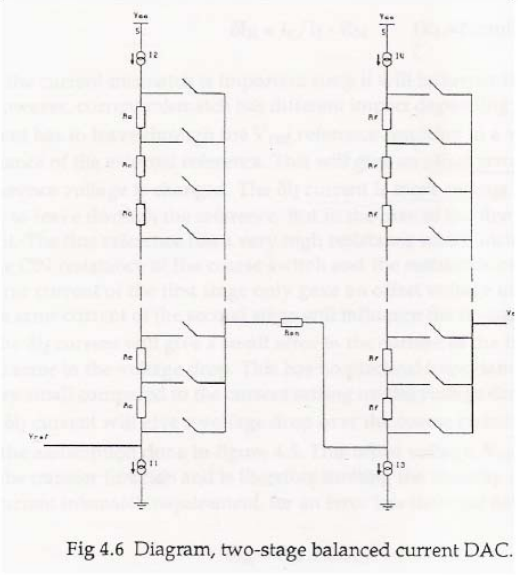


Fig 4.6 Diagram, two-stage balanced current DAC.

Fra ”High-Speed Data Converters Fully Integrated in CMOS”, Leif Hanssen, dr. scient. avhandling., Ifi, UiO, 1990.

Lykke til!!

INF4420 Project 2009 (1/2)

INF4420 project description

Some years from now, you have been hired by an undisclosed chip maker as their mixed signal designer, partly because of your acheivements in the INF4420 course. The company is currently working hard towards finishing their new flagship product. The system designers in your group already have very promising high level simulation results of the product. From these simulations they have derived the specifications for each building block.

The OTAs are central components in this system, as a lot of the specifications for the final product relies on OTA performance. Your group's analog designer already have a working folded cascode OTA which almost meets the spec, except for the offset voltage. This is not easily correctable in the layout because the required transitor sizing would be impractical and incur other unacceptable side effects.

At the next meeting, you suggest doing a digital calibration loop[1] for the OTA's offset voltage. The OTA's designer advice you that the trimming can be done easily by drawing a compensation current from the input-stage differential pair.

For this product, timing is not tight so you should have plenty of time for running the calibration. However, if you can make it faster, it will be much easier to apply to future products, without having to go through an expensive redesign.

1 Measuring the OTA performance

The existing OTA is available from `/hom/jorgenam/cadence_stm90/INF4420`. Use the library manager to add this path (Edit → Library path...). Using an ideal 100 fF capacitor as load, connect the OTA in a closed loop unity gain feedback, and measure the following:

- Gain-bandwidth product (GBW)
- Phase margin (PM)

If you like, you can also measure

- Noise
- Slew rate (how does this compare to the theory?)
- Output swing
- Settling behaviour
- Or other relevant parameters

[1]The workings of the calibration loop will be described later.

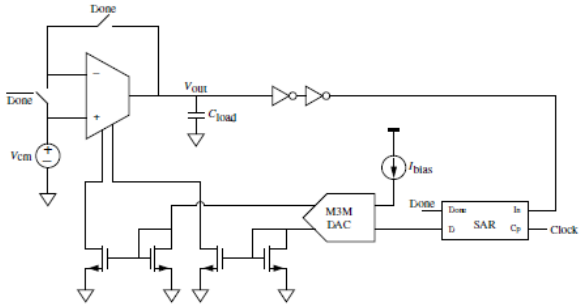


Figure 1: Digital trimming of the OTA's offset voltage (All NMOS are 0.5/0.5 μm)

Next, set up a testbench to find the variation in offset voltage. Use a montecarlo (MC) analysis with 100 runs.

- What is the standard deviation, σ, of the offset voltage?
- If we cover 6σ variation, how many percent of the manufactured OTAs will function to spec?
- What is the 6σ value?

Remembering that g_m is the transistor parameter that relates a change in gate voltage to a change in drain current, we can find the maximum required compensation current as $I_{\text{bias}} = 6\sigma \times g_m$. To find the g_m you can use an operating point analysis (remember to save operating point) and the results browser which you find under the tools-menu in ADE.

- What is the value of g_m of transistor M1 or M2 in the OTA?
- What is the value of I_{bias}?

2 Simulating the calibration loop

It's now time to simulate the entire calibration loop using the supplied components `OTA_trim`, `DAC_ideal`, and `SAR`. `OTA_trim` is the same as `OTA` but with an added current-mode trimming port. `DAC_ideal` is an ideal 7 bit D/A converter with radix 1.77 (sub-binary resolution).

If we run the OTA in open loop, an offset voltage will cause the output to rail (assuming sufficient gain). We can use this to detect if the offset voltage is too high or low. To properly buffer the output to a clean digital level, we can add inverters as buffers.

The DAC outputs a differential current approximately proportional to the input word (it does have some redundancy). This current is applied to the trimming port of

INF4420 project 2009 (2/2)

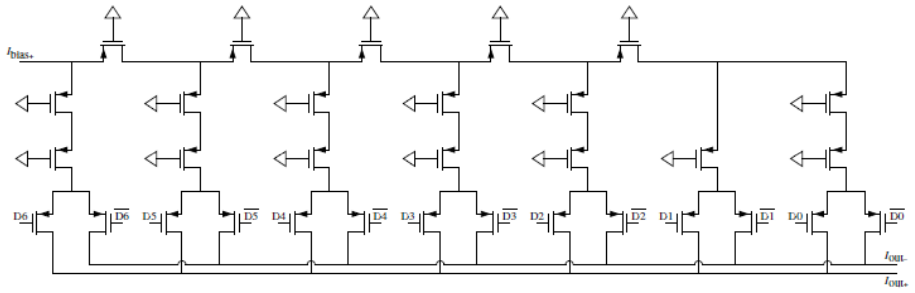


Figure 2: M3M DAC schematics (all PMOS are 0.5/0.2 μm)

the OTA through a current mirror. Thus, we now have a digital input for trimming the OTA's offset voltage. To find the suitable digital correction word, we will use a successive approximation register (SAR). The SAR tests each bit, starting at the MSB. If the OTA output swings above the common mode output voltage, the tested bit is cleared. After testing each bit, the SAR signals that it is done, and that normal system operation can resume. Thus, this signal can be used to switch the OTA between open loop and closed loop unity gain feedback.

- Simulate the system to verify its functionality
- What is the offset voltage after calibration?
- What is the σ of the offset voltage now?

Make a testbench and measure how the added trimming circuitry affect the performance of the OTA.

- Is the performance different compared to your previous measurements?
- What can be done to counter this?

3 DAC design

- Draw ideal transfer functions for a radix 2 converter and a radix 1.77 converter in the same plot.

Figure 3 depicts the schematics of a so called M3M DAC. The mosfets are all in the triode region.

- How does this structure compare to the more familiar R2R DAC?
- Make a testbench where you compare the transfer function of the ideal DAC with the M3M DAC.

Replace the ideal DAC in your calibration loop test bench with the M3M DAC.

- How does this affect the performance of the calibration loop?

Draw layout for the M3M DAC and the current mirror, remember to verify its correctness using DRC and LVS. Finally, do a parasitic extraction of the layout.

- Simulate the calibration loop with the extracted netlists.

4 Project requirements

The transistor sizing given in this document are reasonable guidelines to get you started. You are free to change this if neccessary.

Document everything, including but not limited to, all relevant schematics, layout, and simulation results. Discuss the choices you have made in designing and testing. Everything should be clear just from reading the documentation.

5 Deliverables

1. Do the first part of the project, described in Sect 1. Deadline March 19.
2. Do the second part of the project, described in Sect 2. Deadline April 2.
3. Finalize the project by completing the third and final part of the project, described in Sect 3, and write your final report. Deadline May 11.

In the first two deliverables, write a short report observing the guidelines in Sect 4. The final report must be comprehensive and document the entire project (i.e. include all deliverables). Only this final report will contribute towards your final grade. Please make all schematics and layout available for inspection.

JAM, February 12, 2009

Project, 2010 (1/2)

INF4420 Project

Amir Hasanbegovic
February 3, 2010

Successive approximation register (SAR) analog to digital converter (ADC)

Project introduction

Data converters are one of the fundamental building blocks in integrated circuit design. Their purpose is to interface the analog and digital domains. Data converters can be realized in many different ways and may be found in a wide variety of applications. One often used ADC topology is the SAR ADC, see Figure 1. This topology uses a DAC, sample and hold, comparator and digital circuitry in order to convert an analog signal into a digital form of representation.

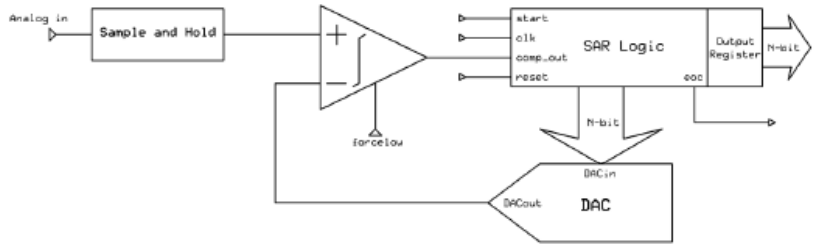


Figure 1) SAR ADC

Your task is to design a *current steering digital to analog converter* and an *output register*, which is going to be implemented in a SAR ADC topology.

There are several (ideal) components supplied that may be used in the project. These components can be found here: */ifi/midgard/h01/amirh/tsmc90nmlp2/INF4420Project*

To get access to these components bring up the Library Manager in Cadence, go to (Edit->Library Path), then type in the library name "INF4420Project" and the library path displayed above. If you want to *edit* the files, copy them to your cadence folder using Library Manager.

The workload in the project is intended for groups consisting of two students.

Task 1: Design a testbench for the DAC and SAR ADC introduction

- Make a suitable testbench for the DAC.
- Write a small report (2 pages maximum) regarding the SAR ADC architecture and include the following in your report:
  - Describe the functionality of a typical SAR ADC architecture.
  - Pros and cons of the SAR ADC architecture.
  - Other aspects that may be relevant.

  (This report may be included in your final report as parts of the introduction or similar)
- Get yourself familiar with the supplied SAR ADC components and implement the *output register* using the supplied (ideal) building blocks.

Task 2: DAC design

Current steering DACs are based on an array of current sources that are switched to the output node depending on the input digital code. There are several different ways of implementing such a topology, however tradeoffs between these topologies should be taken into consideration. This will be up to you as designers to evaluate. The basic concept is illustrated in Figure 2.

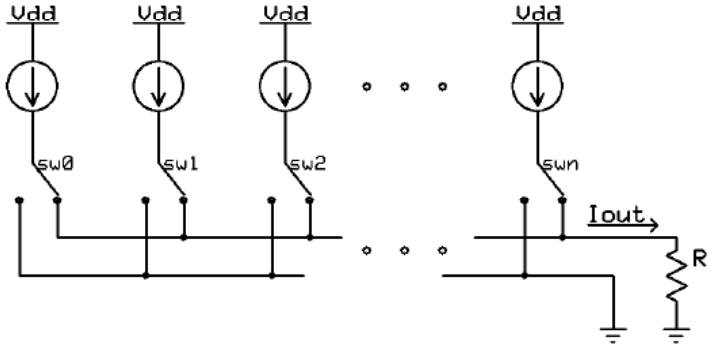


Figure 2) Basic concept

Project, 2010 (2/2)

The *minimum* specification requirements for the DAC are:

- Minimum 6bit resolution
- Sample rate > 8Ms/s
- DNL < +/- 0.5LSB
- INL < +/- 0.5LSB
- Minimum output signal range of 600mV. (i.e 0-600mV)

For this particular implementation the supply voltage is 1.2V and you may assume you have a 1uA current source available for biasing.

There are several other DAC specifications that are important, such as power consumption, settling time etc. Identify these specifications and include them in your final report.

Task 3: Implementation of DAC into SAR ADC

Implement your DAC design into the SAR ADC topology. Make necessary modifications to the ideal components if your implementation has higher specifications then the minimum (for example resolution).

- Assign a ramp up signal to the ADC input and verify that you get corresponding digital values on the ADC output.

Project requirements

Group members must jointly go through the project description and assign work assignments. It must be made visible in the report how the distribution of work has been assigned throughout the project. The following (*but not limited to*) tasks must be addressed before the project can be regarded as complete:

1) It is expected that all circuits/sub-circuits have a schematic and appropriate symbol. The final DAC should be made up of a single symbol.

2) After the DAC schematic is complete and all simulation results (including Monte Carlo simulations) are satisfactory, a layout of the complete system must be made. There are certain issues that are often encountered when doing analog/mixed-signal layout. Find out what they could be and describe them in your final report. Make an effort to implement countermeasures.

3) When you have completed the layout, run Design Rule Check (DRC) and Layout Versus Schematic (LVS). These checks have to be free of errors. The LVS output log must be included in the final report as an appendix.

4) The next step is to do back annotation of parasitic components (R and C) to the schematic view, or parasitic extraction as it is also called. This will result in a netlist with parasitic resistances and capacitances.

5) On the basis of the extracted netlist, you may now do post layout simulations (Monte Carlo simulations included). Her you must carry out the appropriate simulations and compare them with the previous simulation results that were solely based on the schematics.

Report requirements

The final report may be written it the text editor of your choice, but the report must be well organized and easy to read. All central aspects of the project must be supplied by relevant figures and plots. It is important to document/justify the choices you make regarding both the schematic and layout. (Important topics may be; matching, transistor dimensions, choice of components etc.) Plots of all the schematics and the layout, with clearly visible parameters such as dimensions must be included as an appendix for all circuits/sub circuits. References that you may have used in the project must also be included. All schematics and layouts must be made available for inspection, with the exact directory path specified in your final report. Everything must be understandable just from reading the final report.

Submissions and approvals

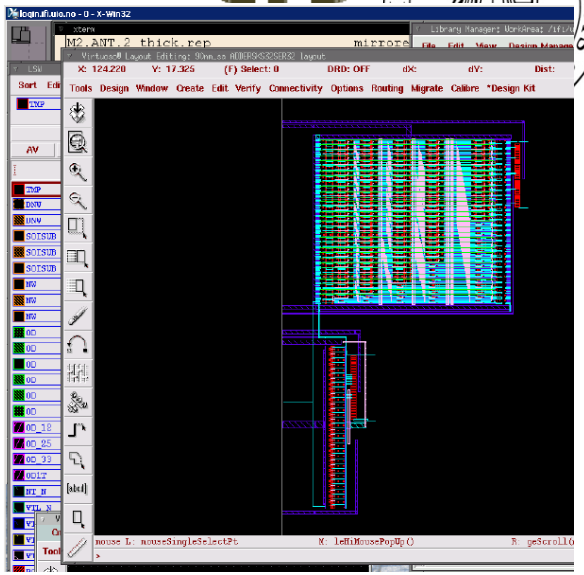
- Task 1. ***Mandatory*** hand-in.
  - Schematics (approved by lab advisor) ***Deadline February 15.***
- Task 2.
  - Schematic (approval by lab advisor) ***Deadline March 15.***
  - Layout (approval by lab advisor) ***Deadline April 12.***
- Task 3. ***Deadline April 19.***
- Final Report. ***Deadline May 4.***

Cadence (http://www.cadence.com/)

- Widely used IC design tool worldwide, both in companies and academia
- Very large system
  - PCB-design
  - IC-design
    - Synthesis
    - Schematic entry
    - Simulator (Analog Environment / Spectre)
    - Layout (Virtouso)
- DRC and LVS performed by Calibre (Mentor)

Full-custom (”handmade”) design flow

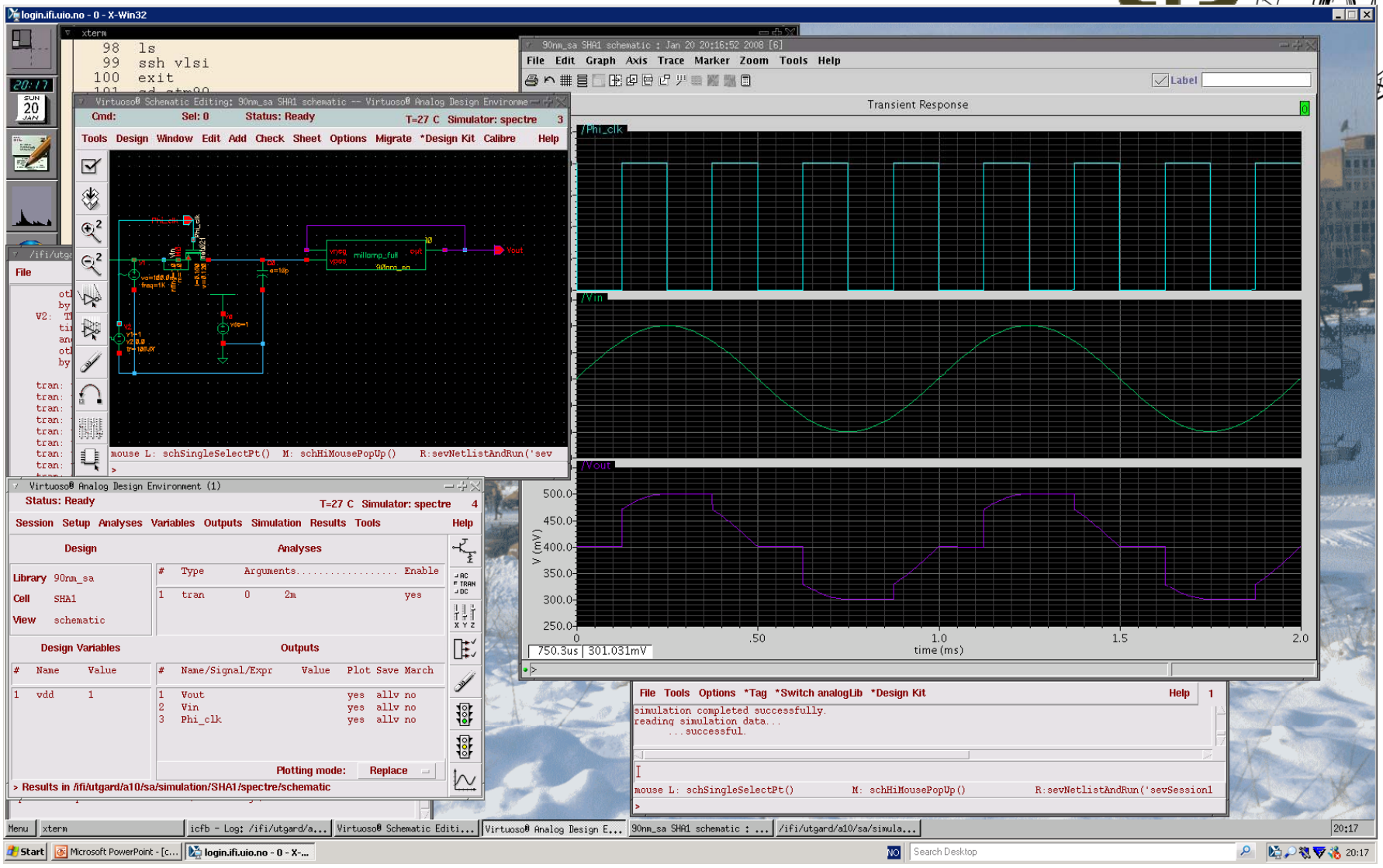
- Design and calculation
  - Design equations
  - Dimensioning for matching
- Schematic entry
  - Simulations on cells and top level
  - Several interactions
- Layout
  - Module interface
  - Symmetry/hierarchy
  - Post Layout Simulations on critical modules
- Next module….



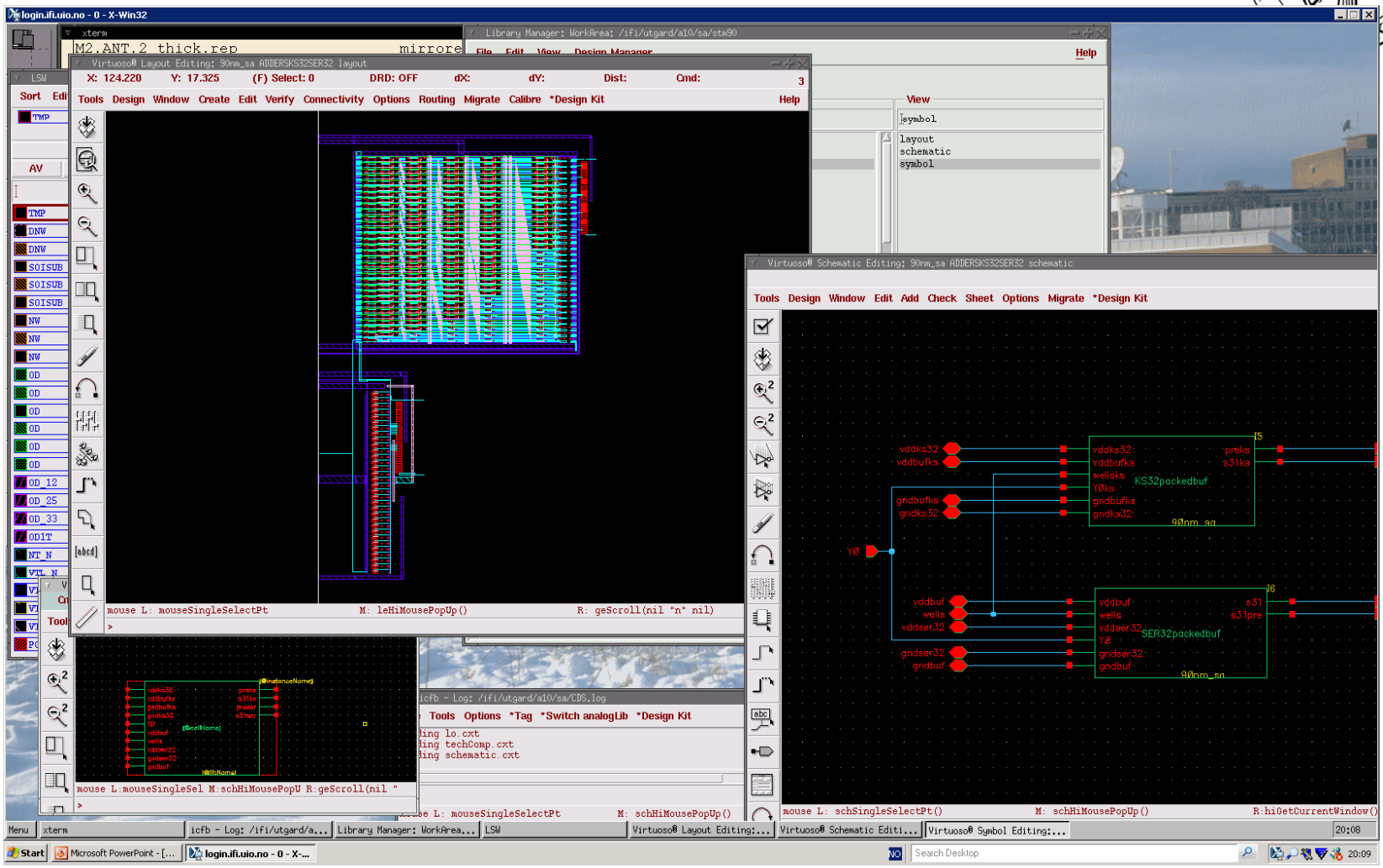
Cadence forts.

- Start-up:
  - Web manual
- Standard libraries:
  - tsmcN90rf
  - analogLib
- Design views:
  - Symbol
  - Schematic
  - Layout

Schematic entry and simulations in Cadence



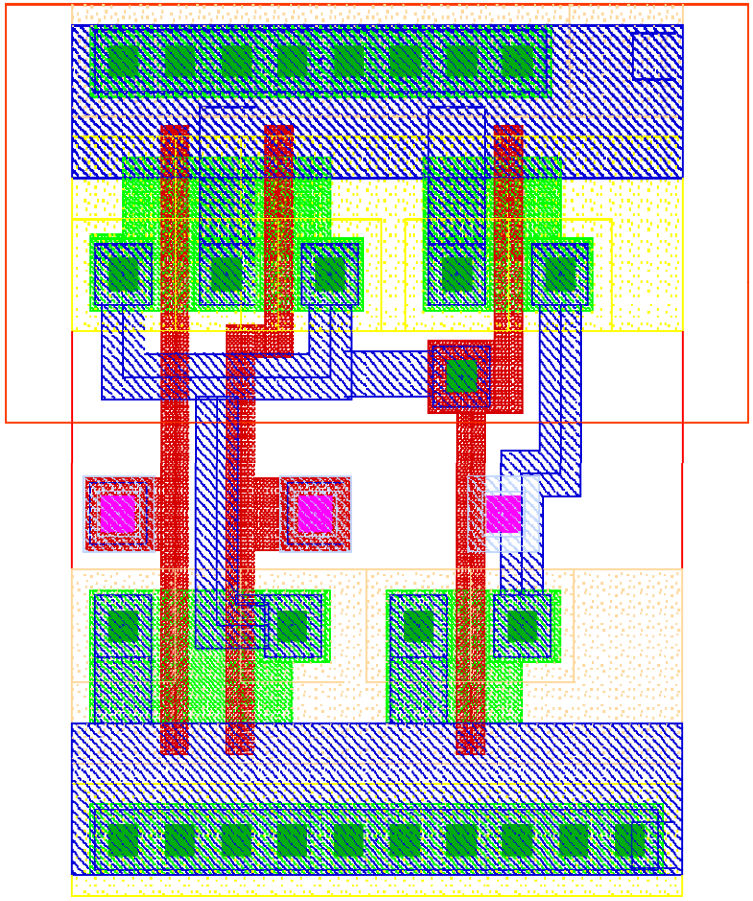
Symbol, schematic and layout (cadence)



Process

- TSMC 90 nm low power CMOS:
  - Minimum gate length: 90nm
  - 1 Poly-layer
  - 9 Metal-layers
  - True triple well
  - Three different threshold voltages
  - Supply voltage: 1.2 V typ.
  - Very advanced process

AND-gate



Challenges regarding the project

- Project administration
- Theoretical analysis and circuit design
- Design errors
  - LVS
- Parasitic components
  - Extraction and Post Layout Simulation (PLS)
- Process variations
  - Simulations (Corner + Monte-Carlo)
- Noise
  - Component and crosstalk
- Good layout practice / Symmetry

Practical information

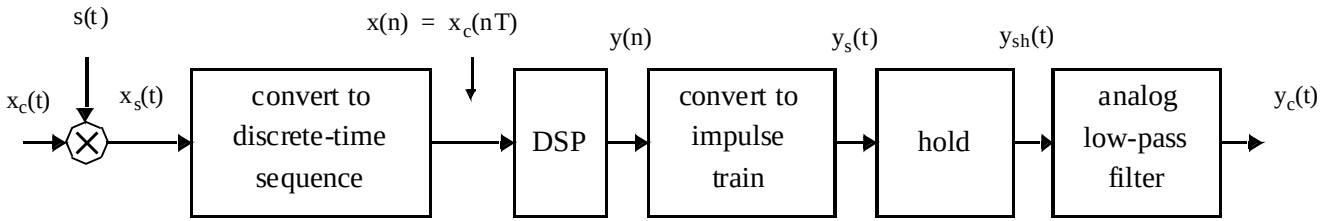
- Lectures:
  - Tuesdays . 9.15 – 11.00, Perl 2453 (should not collide with FYS3240).
  - From. 22/2: Tuesday . 9.15 – 12.00 (Might be 9:15 – 11:00 in most cases)
- Syllabus:
  - Behzad Razavi: Design of Analog CMOS Integrated Circuits (from chap. 11-18.)
  - Selected additional material and lecture notes
  - LTH: Cadence 4.4
  - IFI: Lokal guide til Cadence
- Exercises
  - 2 hours per week – Perl 2453, wednesdays 12:15-14. Kin Keung Lee, kklee@ifi.uio.no
- Project supervision/design lab
  - 2/4 hours each week – Time: 12:15-14:00. Martin S. O. Haugland, mshaugla@ifi.uio.no, Kin Keung (”Kody”) Lee .
  - Ole Johan Dahls hus; Chill 3443
- Software:
  - Cadence 5.00 or 6.00 ((?))
  - TSMC 90 nm design kit
- Where to run the software:
  - Win PC running X-Win connected to Linux server /remote desktop and Linux
  - Linux computer
- Student reference group
  - 1-2 students

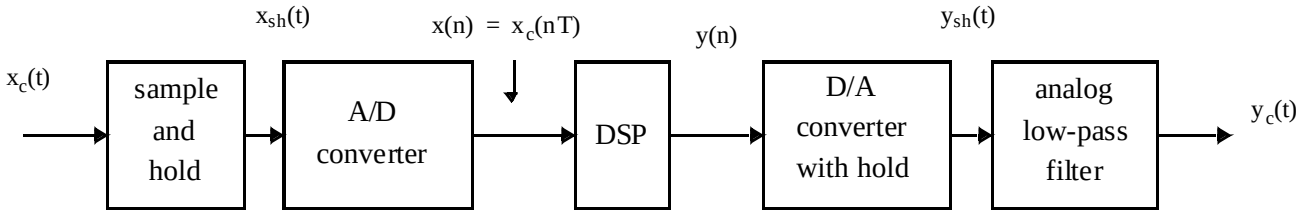
What do we expect from you?

- The course is demanding
- Theoretical background
  - INF3410 analog microelectronics, or similar
  - FYS3220 linear circuit theory, or similar
  - INF3440 signal processing, or similar
- Prepare for the lectures
- Exercises
- Use the reference group and course evaluations to provide feedback to the INF4420 staff

Final exam – a few words

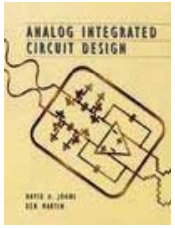
- Thursday 6th of June, starting 14:30 (4 hours)
- Problems usually related to most of the relevant chapters in the book (11-18), and material from the lectures

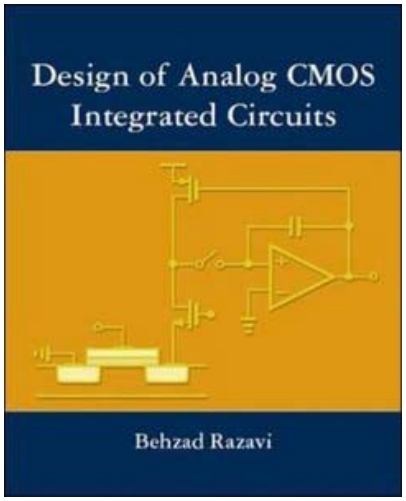




Syllabus; chapters 11-18 (Razavi)+ data converters (Johns & Martin ++)

- Chapter 11 Bandgap references
- Chapter 12 Introduction to Switched Capacitor Circuits
- Chapter 13 Nonlinearity and mismatch
- Chapter 14 Oscillators
- Chapter 15 Phase-locked loops
- Chapter 16 Short-Channel effects and Device models
- Chapter 17 CMOS processing technology
- Chapter 18 Layout and packaging
- Chapter 14 in J&M
- Oversampling converters + additional material on data converters





Bandgap references (chapter 11 in Razavi)

A High Precision Curvature Compensated Bandgap Reference without Resistors

Jianghua Chen*, Xuewen Ni, Bangxian Mo and Zhanfei Wang
Institute of Microelectronics, Peking University, Beijing 100871, P. R. China
* Email: chenjianghua@ime.pku.edu.cn

A High Precision Curvature Compensated Bandgap Reference with
Jianghua Chen; Xuewen Ni; Bangxian Mo; Zhanfei Wang;
Solid-State and Integrated Circuit Technology, 2006. ICSICT '06. 8th Inte
23-26 Oct. 2006 Page(s):1748 - 1750
Digital Object Identifier 10.1109/ICSICT.2006.306414
AbstractPlus | Full Text: PDF(124 KB) **IEEE CNF**
Rights and Permissions

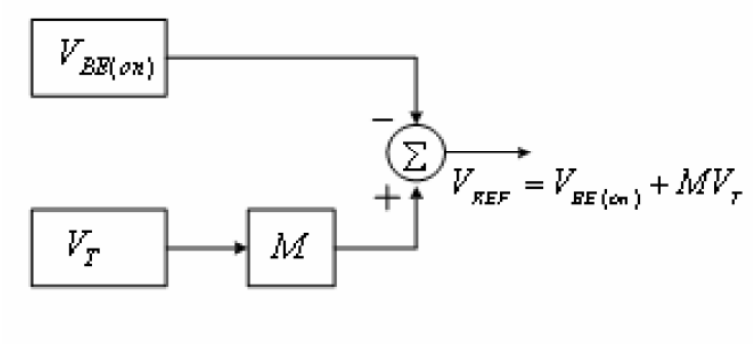


Figure 1 General bandgap reference architecture.

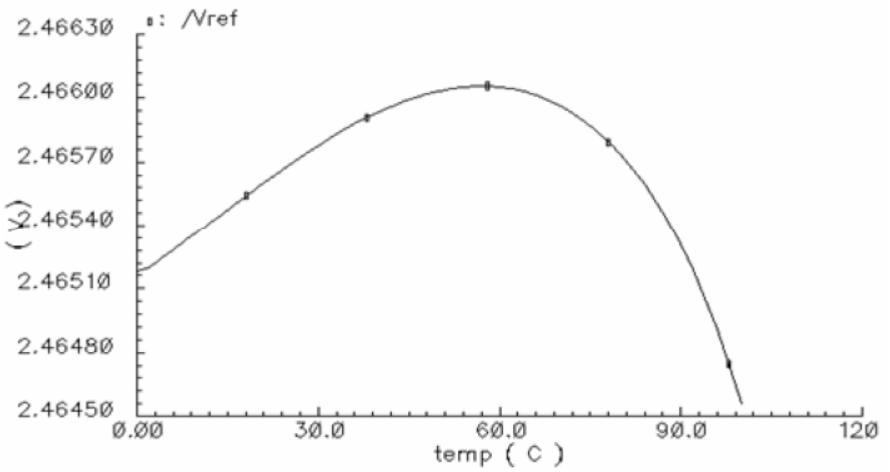


Figure 4 Output reference Verf vs. temperature.

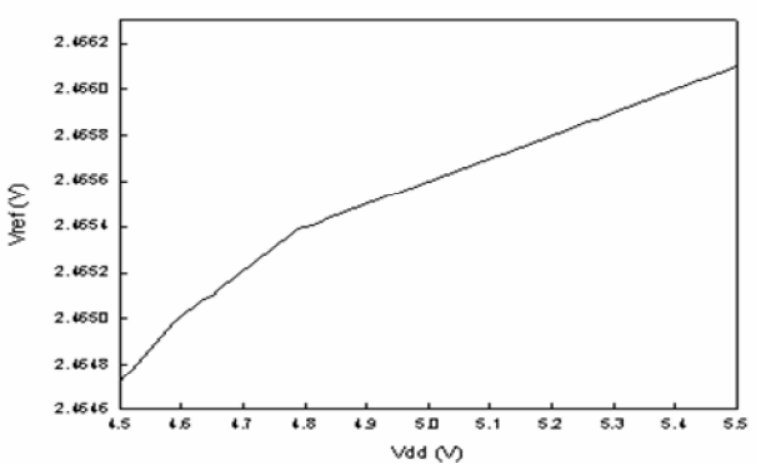
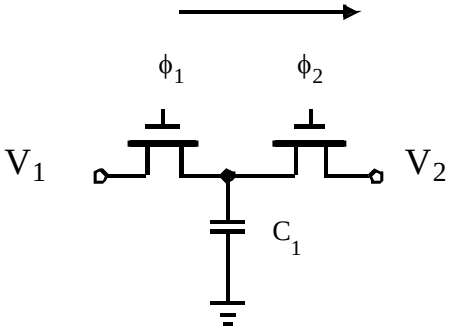
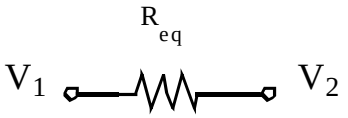


Figure 5 Output reference Vref vs. power supply Vdd.

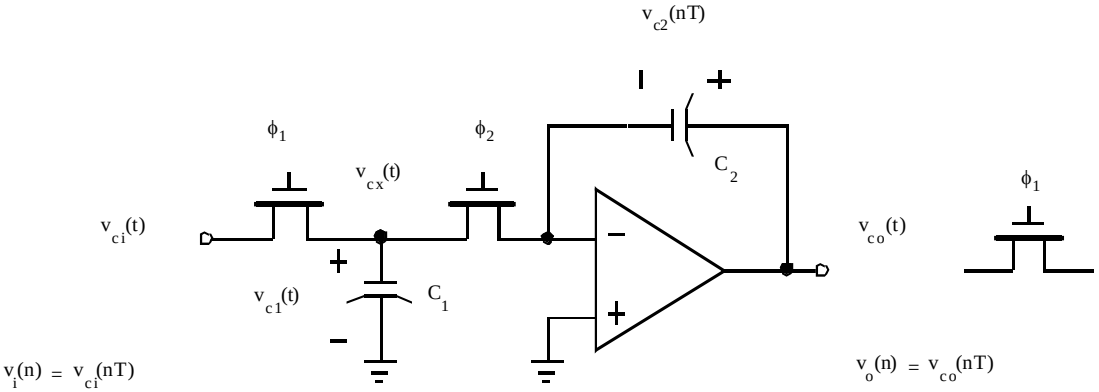
Chapter 12 Intro to Switched Cap. circuits



$\Delta Q = C_1(V_1 - V_2)$ every clock period



$$R_{eq} = \frac{T}{C_1}$$

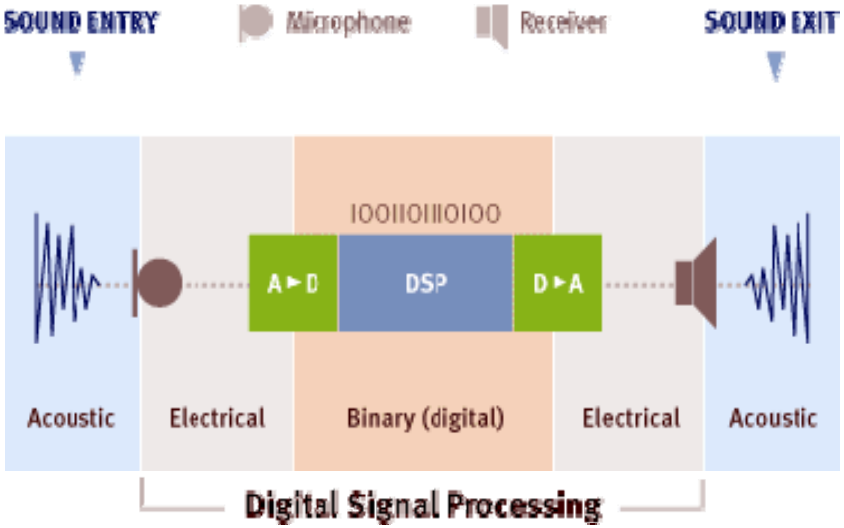


Chapter 13 Nonlinearity and mismatch

- Nonlinearity
- Mismatch

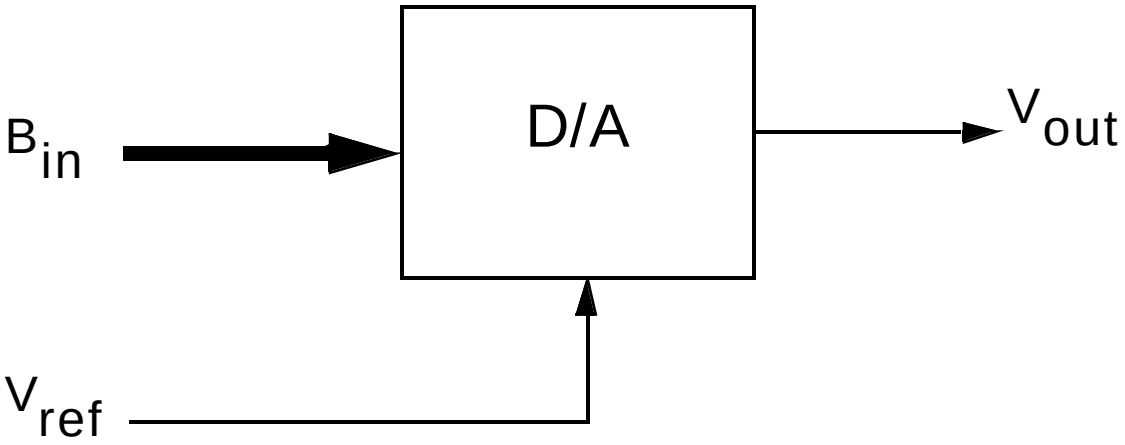
Data converter fundamentals

- Ideal D/A and A/D
- Quantization noise
- Signed codes
- Performance limitations



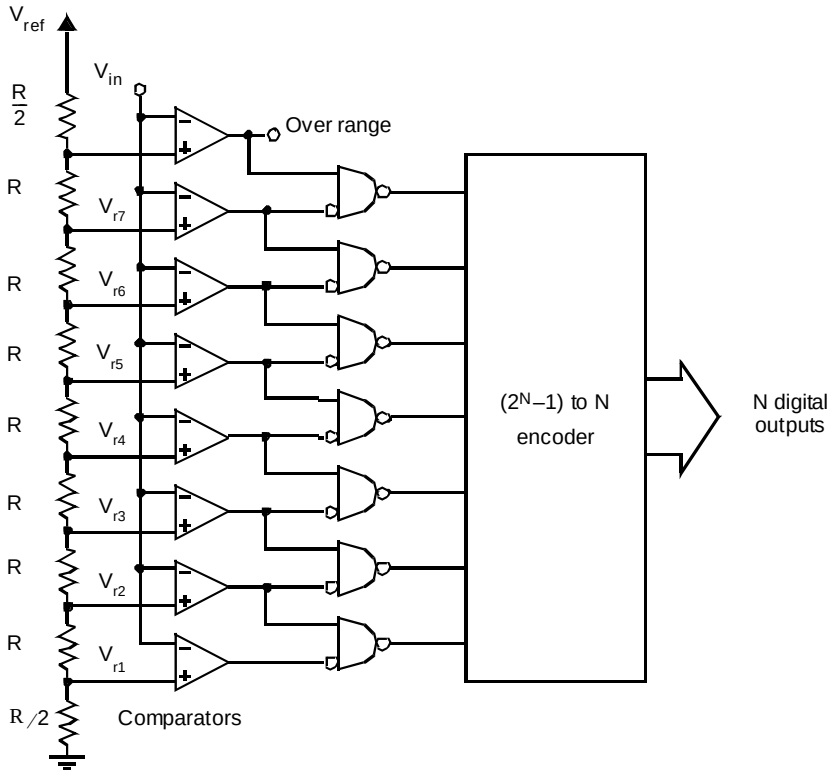
Nyquist-Rate D/A Converters

- Decoder-based converters
- Binary-scaled converters
- Thermometer-code converters
- Hybrid conv.



Nyquist-Rate A/D Converters

- Integrating converters
- Successive approx. converters
- Algorithmic converters
- Flash (parallell) conv.
- Two-step, interpolating,
- Folding, pipelined conv.



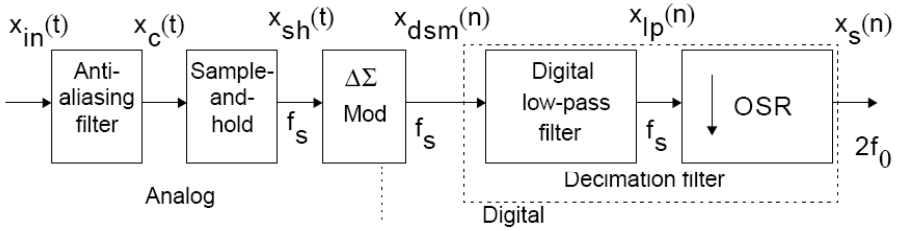
Two consequences of the Nyquist-theorem and anti-aliasing filters

(Wikipedia):

- If the highest frequency *B* in the original signal is known, the theorem gives the lower bound on the sampling frequency for which perfect reconstruction can be assured. This lower bound to the sampling frequency, 2*B*, is called the Nyquist rate.
- If instead the sampling frequency is known, the theorem gives us an upper bound for frequency components, $B<fs/2$, of the signal to allow for perfect reconstruction. This upper bound is the Nyquist frequency, denoted fN.
- An **anti-aliasing filter** is a filter used before a signal sampler, to restrict the bandwidth of a signal to approximately satisfy the sampling theorem. Since the theorem states that unambiguous interpretation of the signal from its samples is possible only when the power of frequencies outside the Nyquist bandwidth is zero, the anti-aliasing filter would have to have perfect stop-band rejection to completely satisfy the theorem. Every realizable anti-aliasing filter will permit some aliasing to occur; the amount of aliasing that does occur depends on how good the filter is.

Chapter 14 in ”Johns & Martin”Oversampling Converters

- Oversampling (>> 2 Nyquist bandwidth) relaxes requirements for matching
- High resolution, low to medium speed
- Noise shaping & oversampling
- N+1 order modulator gives a certain SNR for lower OSR than N-order mod.
- 24 bit Audio conv.



Chapter 14 ("Razavi") Oscillators

Oscillators are an integral part of many electronic systems. Applications range from clock generation in microprocessors to carrier synthesis in cellular telephones, requiring vastly different oscillator topologies and performance parameters. Robust, high-performance oscillator design in CMOS technology continues to pose interesting challenges. As described in Chapter 15, oscillators are usually embedded in a phase-locked system.

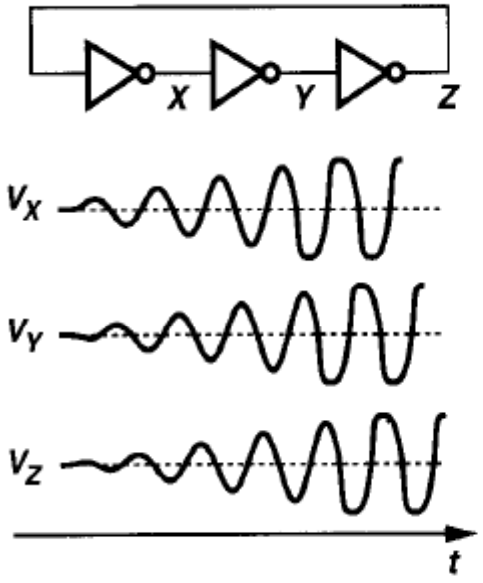
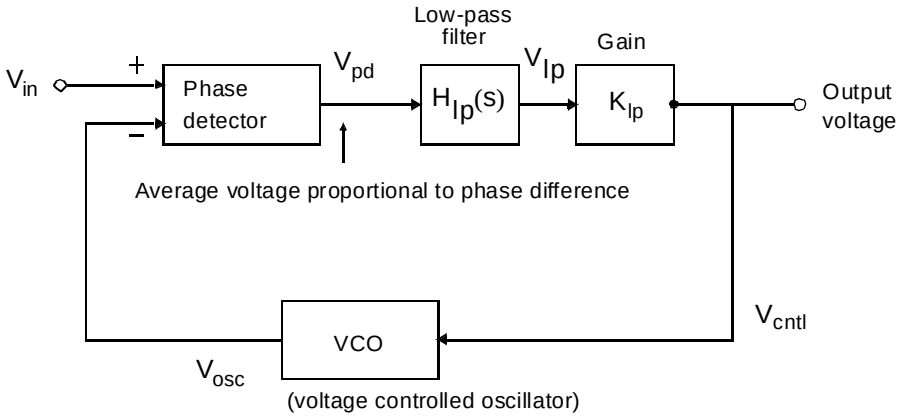


Figure 14.13 Ring oscillator using CMOS inverters.

Chapter 15 Phase-locked loops

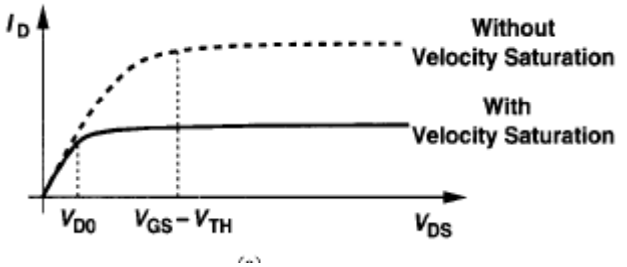
- Application examples:
- clock multiplication,
- Freq. generation: The PLL output is a signal with frequency N times the input frequency where N may be a fractional number
- FM demodulation (The input is a FM signal (IF) The output is the demodulated baseband signal
- Products: TV and wireless



Chapter 16 Short-Channel Effects and Device Models

The square-law characteristics derived for MOSFETs in Chapter 2 provide moderate accuracies for devices with minimum channel lengths of greater than 4 μm, a value corresponding to technologies in production in the early 1980s. As device dimensions continue to scale down, reaching below 0.2 μm by the year 2000, higher order effects necessitate more complex models so as to attain enough accuracy in simulations.

The problem of device models in CMOS technology has constantly haunted analog designers, manifesting itself as substantial discrepancies between simulated and measured results. A number of comprehensive books [1, 2, 3] and hundreds of papers deal with the subject in great detail, but our objective here is to provide a basic understanding of short-channel effects and review some of the SPICE models developed to reflect such phenomena. Knowledge of these issues also proves useful in interpreting the anomalies that the designer may encounter in SPICE simulations.



Chapter 17 CMOS Processing Technology

Published: Monday, Jan. 24, 2011 /
Updated: Monday, Jan. 24, 2011 08:08 AM
Altera Unveils 28-nm Device Portfolio Tailored to Customers' Diverse Design Requirements
Industry's Most Diverse Product Offering Meets Expanding System Needs in Performance, Power and Cost

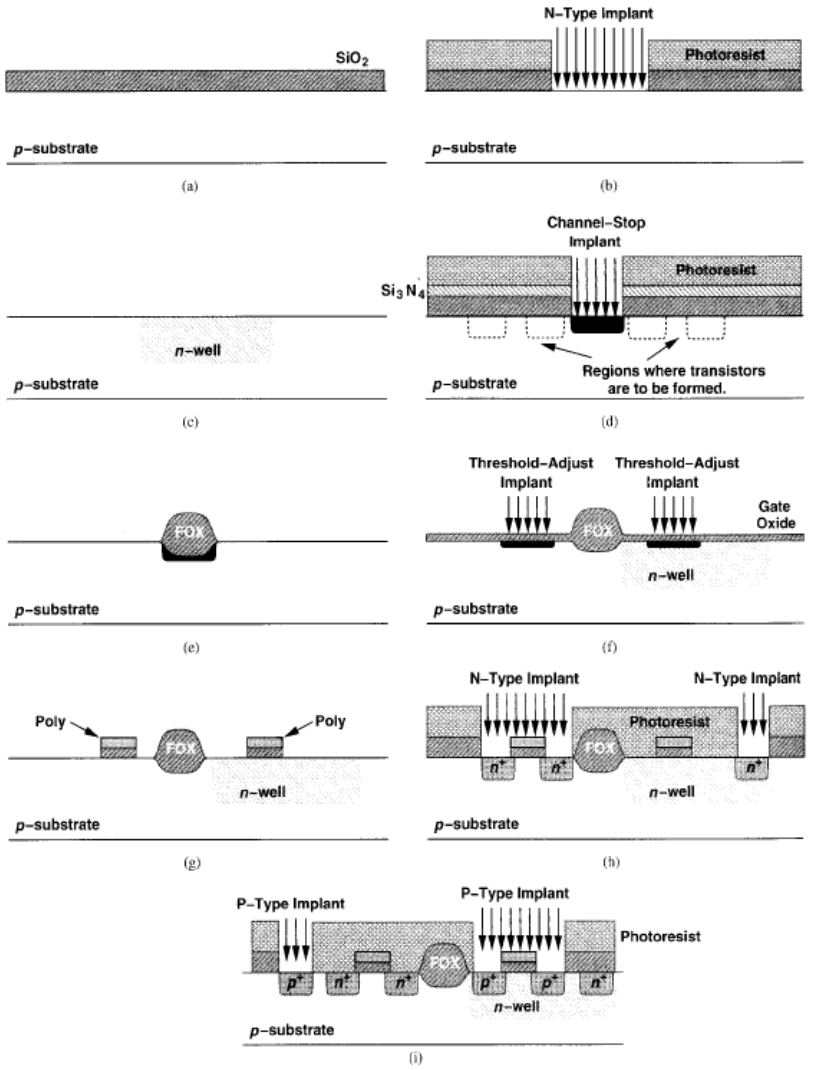
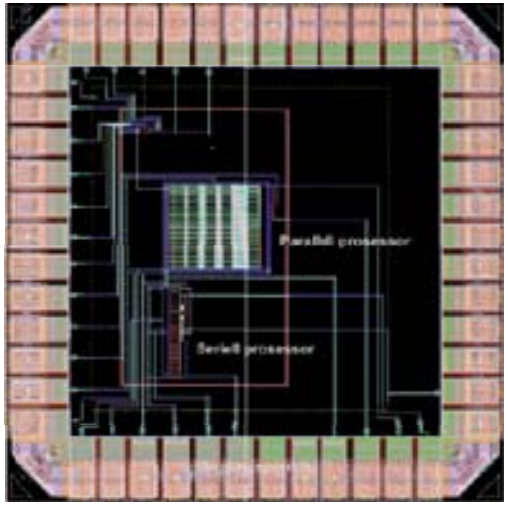
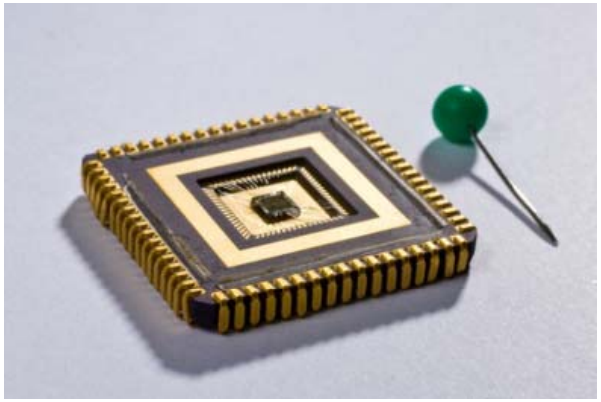
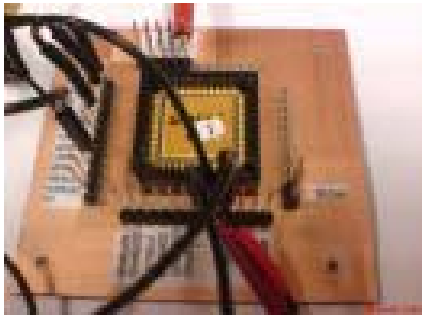


Figure 17.8 Fabrication sequence of MOS devices.

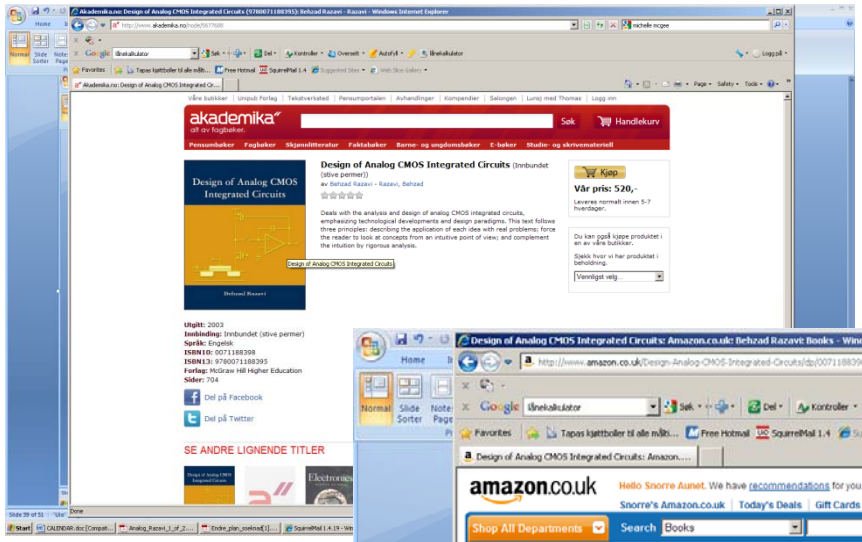
Chapter 18 Layout and Packaging







www.akademika.no / www.amazon.co.uk



Next week:

- Sample and Hold circuits ++
- Messages are given on the INF4420 homepage.
- Questions: sa@ifi.uio.no , 22852703 / 90013264