Bandgap references, sampling switches

Tuesday, February 1st, 9:15 – 12:00

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Outline – Tuesday, February 1st

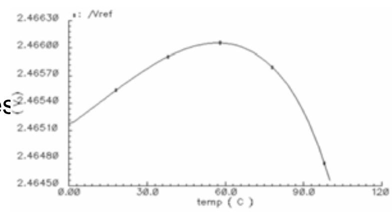

Figure 4 Output reference Verf vs. temperature.

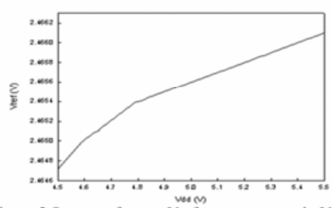

Figure 5 Output reference Vref vs. power supply Vdd.

A High Precision Curvature Compensated Bandgap Reference without Resistors

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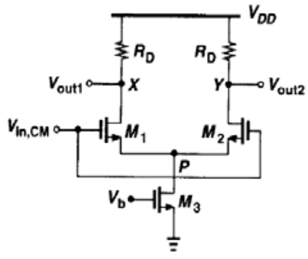
Bandgap references for stable dc quantities

- References that exhibit little dependence on supply and process parameters and a *well defined* dependence on temperature
- The required temperature dependence assume one of three forms:
- 1) proportional to absolute temp. ("PTAT")
- 2) constant G-m behaviour
- 3) temperature independent
- Design for supply-independent biasing and define temperature variation



(a)

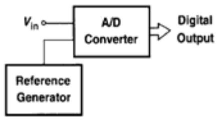


Figure 11.28 A/D converter using a reference generator.

1.2 Supply independent biasing ("Razavi" pp. 377.)

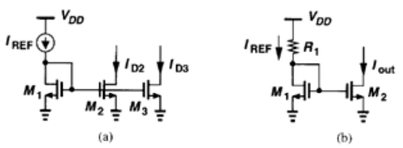


Figure 11.1 Current-mirror biasing using (a) an ideal current source, (b) a resistor.

- A resistor tied between the supply voltage (" Vdd ") and the gate gives a circuit quite sensitive to V_{DD} variations.

$$\Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_{m1}} \cdot \frac{(W/L)_2}{(W/L)_1}.$$

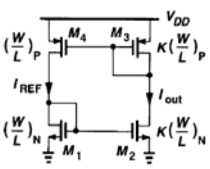


Figure 11.2 Simple circuit to establish supply-independent currents.

- Less sensitive solution where the circuit bias itself, with I_{ref} being a replica of I_{out} ($\lambda \approx 0$)

$I_{out} = K\, I_{ref}$

Uniquely defining currents by adding a resistor

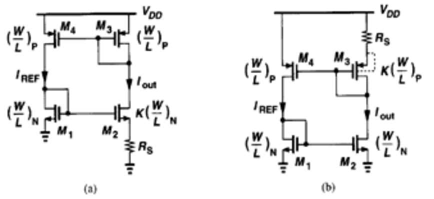


Figure 11.3 (a) Addition of R_S to define the currents, (b) alternative implementation eliminating body effect.

require that $I_{out} = I_{REF}$ because they have identical dimensions. We can write $V_{GS1} = V_{GS2} + I_{D2}R_S$, or

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}} + V_{TH1} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox} K(W/L)_N}} + V_{TH2} + I_{out}R_S. \quad (11.2)$$

Neglecting body effect, we have

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}}\left(1 - \frac{1}{\sqrt{K}}\right) = I_{out}R_S, \quad (11.3)$$

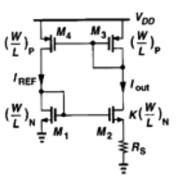
and hence

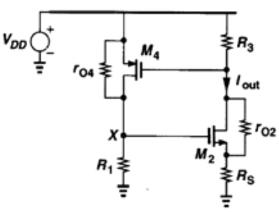
$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N} \cdot \frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2. \quad (11.4)$$

- The current becomes independent of the supply voltage (but still a function of process and temperature).
- The assumption $V_{TH1} = V_{TH2}$ introduces some error, but a simple remedy is shown in Fig. 11.3 b), by eliminating the body effect by tying the source and bulk of each PMOS transistor.

These circuits exhibit little supply voltage dependence if the channel length modulation is neglible → long channels

Ex. 11.1 Estimating the change in I_{out} for a small change ΔV_{dd} for the BG-ref. in Fig 11.3 a)





- In some applications the supply sensitivity given by (11.6) is prohibitively high. Also, owing to various capacitive paths, the supply sensitivity of the circuit rises at high frequencies.

Solution

Simplifying the circuit as depicted in Fig. 11.4, where $R_1 = r_{O1} \| (1/g_{m1})$ and $R_3 = r_{O3} \| (1/g_{m3})$, we calculate the "gain" from V_{DD} to I_{out}. The small-signal gate-source voltage of M_4 equals $-I_{out}R_3$ and the current through r_{O4} is $(V_{DD} - V_X)/r_{O4}$. Thus,

$$\frac{V_{DD} - V_X}{r_{O4}} + I_{out}R_3 g_{m4} = \frac{V_X}{R_1}. \quad (11.5)$$

If we denote the equivalent transconductance of M_2 and R_S by $G_{m2} = I_{out}/V_X$, then

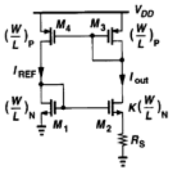
$$\frac{I_{out}}{V_{DD}} = \frac{1}{r_{O4}}\left[\frac{1}{G_{m2}(r_{O4} \| R_1)} - g_{m4}R_3\right]^{-1}. \quad (11.6)$$

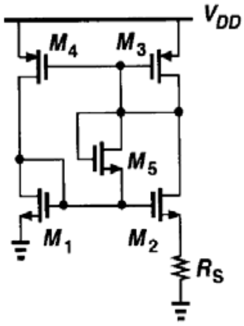
Note from Chapter 3 that

$$G_{m2} = \frac{g_{m2} r_{O2}}{R_S + r_{O2} + (g_{m2} + g_{mb2})R_S r_{O2}}. \quad (11.7)$$

Interestingly, the sensitivity vanishes if $r_{O4} = \infty$.

Adding a start-up device





$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N} \cdot \frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2. \qquad (11.4)$$

- If all transistors in Fig. 11.3 a) carry zero current when the supply is turned on, they may remain off indefinitely because the loop can support a zero current in both branches.
- This is not predicted by (11.4) since we divided by SQRT(I_{out}), assuming Iout ≠ 0; The circuit can settle in two different operating conditions. (”start-up” problem)
- Fix: Adding M_5; path from Vdd through M3 and M1 to ground.

11.3 Temperature-independent References

- Little dependence on temperature is essential in many analog circuits.
- If a reference is temperature-independent it is usually process-independent as well.
- Adding two quantities having opposite temperature coefficients (”TCs”) displays a zero TC;

  $\alpha_1 \delta V_1/\delta T + \alpha_2\ \alpha_1 \delta V_1/\delta T = 0$

  Two voltages that have negative and positive TCs must be identified.
- Bipolar devices in CMOS provide well defined TCs.

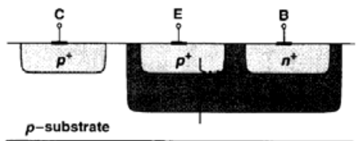


Figure 11.10 Realization of a *pnp* bipolar transistor in CMOS technology.

Negative TC voltage from pn-junction (11.3.1)

- $I_C = I_s \exp(V_{BE}/V_T)$, $V_T = kT/q$
- $I_S \sim \mu k T n_i^2$
- μ: mobility of carriers
- n_i: intrinsic ≈ minority carrier concentration of silicon
- Temperature dependency; $\mu \;\alpha\; \mu_0 T^m$, where m ≈ -3/2, and $n_i^2 \;\alpha\; T^3 \exp[-E_g/(kT)]$, where E_g ≈ 1.12 eV is the bandgap energy of silicon.
- $I_S = bT^{4+m} \exp[-E_g/(kT)]$, b is a proportionality factor.
- $V_{BE} = V_T \ln(I_C / I_S)$
- We can compute the derivative of V_{BE} with respect to T. Assume I_C is constant

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \cdot \ln \frac{I_C}{I_S} + V_T \underbrace{\frac{\partial [\ln(I_C/I_S)]}{\partial T}}_{A}$$

MATH. RULES:

$$y = u \cdot v \Rightarrow y' = uv' + u'v \quad (1)$$

$$\frac{dy}{dx} = \frac{dy}{du} \cdot \frac{du}{dx} \quad (2)$$

$$\frac{d}{dx}(\ln x) = \frac{1}{x} \quad (3)$$

$$\frac{d}{dx}[\ln h(x)] = \frac{h'(x)}{h(x)} \quad (4)$$

$$\left[\frac{u}{v}\right]' = \frac{u'v - uv'}{v^2} \quad (5)$$

A=?

4 th rule:

$$h(x) = I_C / I_S$$

$$h'(x) = (I_C' \cdot I_S - I_C \cdot I_S') / I_S^2$$

$$\Updownarrow$$

$$\left(\frac{\partial I_C}{\partial T} \cdot I_S - I_C \cdot \frac{\partial I_S}{\partial T}\right) / I_S^2$$

$$\Updownarrow$$

$$h'(x) = \frac{-I_C \frac{\partial I_S}{\partial T}}{I_S^2}$$

$$A = \left[\frac{-I_C \frac{\partial I_S}{\partial T}}{I_S^2}\right] \bigg/ \frac{I_C}{I_S} = \frac{-\frac{\partial I_S}{\partial T}}{I_S} = -\frac{1}{I_S} \cdot \frac{\partial I_S}{\partial T}$$

Substituting:

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \cdot \ln - \frac{V_T}{I_S} \frac{\partial I_S}{\partial T} \quad (11.9)$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} - \underbrace{\frac{V_T}{I_S} \frac{\partial I_S}{\partial T}}_{C} \quad (11.9)$$

$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m} \exp(-E_g/kT) + bT^{4+m}\left(\exp(-E_g/kT)\frac{E_g}{kT^2}\right) \quad (11.10)$$

$$\wedge \quad I_S = bT^{4+m} \exp(-E_g/kT) \quad (11.8)$$

$$C = \left[\frac{V_T}{\underbrace{bT^{4+m} \exp(-E_g/kT)}_{I_S}}\right] \cdot b(4+m)T^{3+m}\exp(-E_g/kT) + bT^{4+m}\left(\exp(-E_g/kT)\right)\left(\frac{E_g}{kT^2}\right)$$

$$= \frac{V_T (4+m) T^{3+m} + V_T T^{4+m} \left(\frac{E_g}{kT^2}\right)}{T^{4+m}} = (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2} \cdot V_T \quad (11.1\text{[}...\text{]})$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T} \ln \frac{I_C}{I_S} - (4+m)\frac{V_T}{T} - \frac{E_g}{kT^2} V_T \quad (11.12)$$

Temperature coefficient of V_{BE} at a given Temperature, T

With the aid of (11.9) and (11.11), we can write

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T}\ln\frac{I_C}{I_S} - (4+m)\frac{V_T}{T} - \frac{E_g}{kT^2}V_T \quad (11.12)$$

$$= \frac{V_{BE} - (4+m)V_T - E_g/q}{T}. \quad (11.13)$$

Equation (11.13) gives the temperature coefficient of the base-emitter voltage at a given temperature T, revealing dependence on the magnitude of V_{BE} itself. With $V_{BE} \approx 750$ mV and $T = 300°$K, $\partial V_{BE}/\partial T \approx -1.5$ mV/°K.

From (11.13), we note that the temperature coefficient of V_{BE} itself depends on the temperature, creating error in constant reference generation if the positive-TC quantity exhibits a *constant* temperature coefficient.

11.3.2 Positive-TC Voltage

- If two bipolar transistors operate at unequal current densities, the *difference* between their base-emitter voltages is directly proportional to the absolute temperature
- Q_1 and Q_2 identical and biased at nI_0 and I_0 AND negligible base currents:

$$\Delta V_{BE} = V_{BE1} - V_{BE2} \quad (11.14)$$

$$= V_T \ln\frac{nI_0}{I_{S1}} - V_T \ln\frac{I_0}{I_{S2}} \quad (11.15)$$

$$= V_T \ln n. \quad (11.16)$$

Thus, the V_{BE} difference exhibits a positive temperature coefficient:

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q}\ln n. \quad (11.17)$$

Interestingly, this TC is independent of the temperature or behavior of the collector currents.[1]

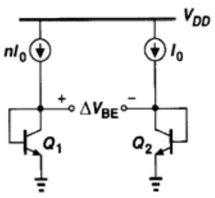


Figure 11.6 Generation of PTAT voltage.

Ex. 11.2 Calculating ΔV_{BE} for the circuit of Fig. 11.7

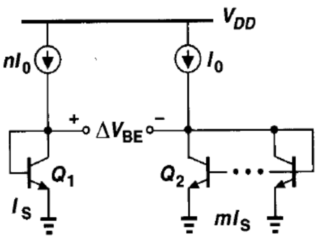


Figure 11.7

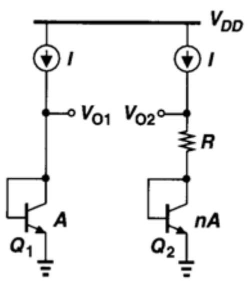
Solution

Neglecting base currents, we can write

$$= V_T \ln \frac{nI_0}{I_S} - V_T \ln \frac{I_0}{mI_S}$$
$$= V_T \ln(nm).$$

The temperature coefficient is therefore equal to $(k/q)\ln(nm)$.

11.3.3 Bandgap reference (concept Fig. 11.8 pp. 384)



- Negative and positive TC voltages combined for a reference having a nominally zero temperature coefficient.
- -1.5 mV / degree K at room temp.
- 1.5 / 0.087 = 17.2
- Ln n = 17.2 translates to a prohibitively large n
- Q_1: unit transistor, $V_{01} = V_{02}$

$$V_{REF} = \alpha_1 V_{BE} + \alpha_2 (V_T \ln n)$$

$\partial V_{BE}/\partial T \approx -1.5$ mV/°K whereas $\partial V_T/\partial T \approx +0.087$ mV/°K

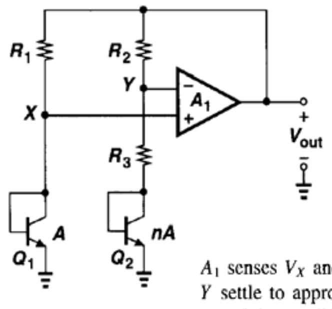
$$\alpha_2 \ln n \approx 17.2$$

for zero TC:

$$V_{REF} \approx V_{BE} + 17.2 V_T \approx 1.25 \text{ V}.$$

to be equal. Then, $V_{BE1} = RI + V_{BE2}$ and $RI = V_{BE1} - V_{BE2} = V_T \ln n$. Thus, $V_{O2} = V_{BE2} + V_T \ln n$, suggesting that V_{O2} can serve as a temperature-independent reference if $\ln n \approx 17.2$ (while V_{O1} and V_{O2} remain equal).

Actual Implementation of Bandgap Reference (Fig. 11.9)



A_1 senses V_X and V_Y, driving the top terminals of R_1 and R_2 ($R_1 = R_2$) such that X and Y settle to approximately equal voltages. The reference voltage is obtained at the output of the amplifier (rather than at node Y). Following the analysis of Fig. 11.8, we have $V_{BE1} - V_{BE2} = V_T \ln n$, arriving at a current equal to $V_T \ln n / R_3$ through the right branch and hence an output voltage of

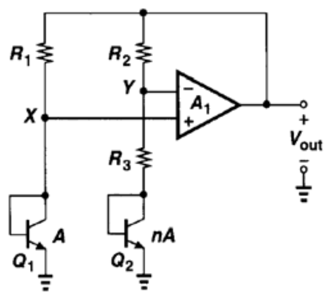
$$V_{out} = V_{BE2} + \frac{V_T \ln n}{R_3}(R_3 + R_2) \qquad (11.22)$$

$$= V_{BE2} + (V_T \ln n)\left(1 + \frac{R_2}{R_3}\right). \qquad (11.23)$$

For a zero TC, we must have $(1 + R_2/R_3)\ln n \approx 17.2$. For example, we may choose $n = 31$ and $R_2/R_3 = 4$. Note these results do not depend on the TC of the resistors.

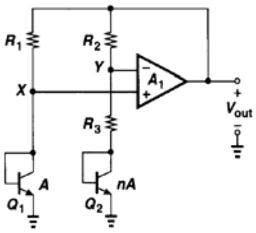
The circuit of Fig. 11.9 entails a number of design issues. We consider each one below.

Design issues for the BG-ref



- Collector Current variation
- Compatibility with CMOS Technology
- Op Amp offset and output impedance
- Feedback Polarity
- Nadgap Reference exhibiting nominally-zero TC is given by a few fundamental numbers
- Supply Dependence and Start-Up
- Curvature Correction

Collector Current variation ("issue 1/7")



- The circuit in Fig. 11.9 violates the earlier assumption that the collector currents of Q1 and Q2 (given by V_T ln n / R_3) are proportional to T, whereas

  $\partial V_{BE}/\partial T \approx -1.5$ mV/°K

  was derived for a constant current. What happens to the temp. coeff. of V_{BE} if the collector currents are PTAT?

iterative solution, let us assume $I_{C1} = I_{C2} \approx (V_T \ln n)/R_3$. Returning to Eq. (11.9) and including $\partial I_C/\partial T$, we have

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T}\ln\frac{I_C}{I_S} + V_T\left(\frac{1}{I_C}\frac{\partial I_C}{\partial T} - \frac{1}{I_S}\frac{\partial I_S}{\partial T}\right). \quad (11.24)$$

Since $\partial I_C/\partial T \approx (V_T \ln n)/(R_3 T) = I_C/T$, we can write

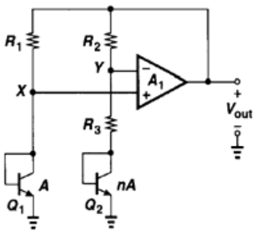
$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T}\ln\frac{I_C}{I_S} + \frac{V_T}{T} - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T}. \quad (11.25)$$

Equation (11.13) is therefore modified as

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (3+m)V_T - E_g/q}{T}, \quad (11.26)$$

indicating that the TC is slightly less negative than -1.5 mV/°K.

Compatibility with CMOS Technology ("issue 2/7")



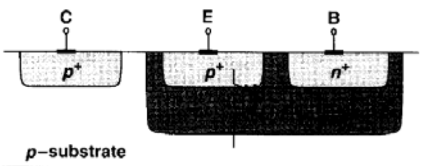


Figure 11.10 Realization of a *pnp* bipolar transistor in CMOS technology.

- Derivation of a temperature independent voltage relies on the exponential characteristics of bipolar devices for both negative and positive-TC quantities
- We seek structures in standard CMOS that exhibit such characteristics
- Nwell- process; pnp as depicted
- Other possibilities; pwell- / triple-well / BiCMOS

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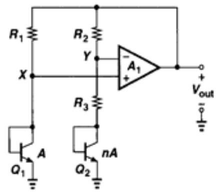
BG-reference from Fig. 11.8 implemented with pnp transistors



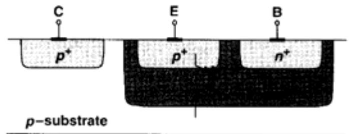


Figure 11.10 Realization of a *pnp* bipolar transistor in CMOS technology.

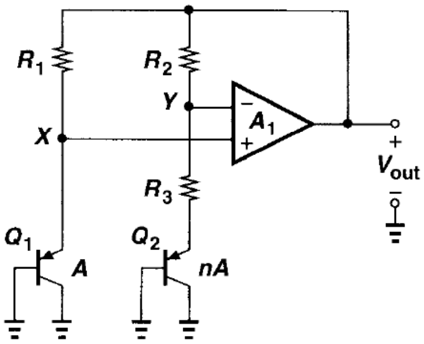
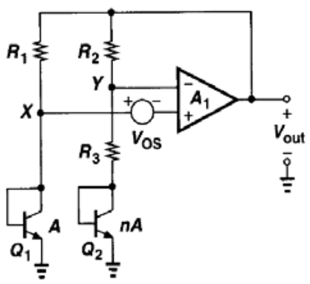


Figure 11.11 Circuit of Fig. 11.9 implemented with *pnp* transistors.

Op Amp Offset and Output Impedance (”issue 3/7”)



- Vout ≠ 0 when Vx = Vy
- The input offset voltage introduces error in the output voltage
- V_{OS} is amplified by $1 + R_2 / R_3$ (eq. 11.28)
- V_{OS} varies with temperature (chapter 13)
- Reduce offset by using large devices in a carefully chosen topology (chapter 18).

troduces error in the output voltage. Included in Fig. 11.12, the effect is quantified as $V_{BE1} - V_{OS} \approx V_{BE2} + R_3 I_{C2}$ (if A_1 is large) and $V_{out} = V_{BE2} + (R_3 + R_2) I_{C2}$. Thus,

$$V_{out} = V_{BE2} + (R_3 + R_2)\frac{V_{BE1} - V_{BE2} - V_{OS}}{R_3} \qquad (11.27)$$

$$= V_{BE2} + \left(1 + \frac{R_2}{R_3}\right)(V_T \ln n - V_{OS}). \qquad (11.28)$$

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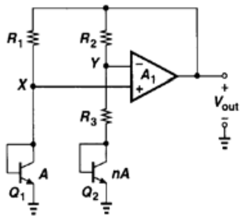
Feedback Polarity ("issue 4/7")



- Feedback Polarity

Feedback Polarity In the circuit of Fig. 11.9, the feedback signal produced by the op amp returns to both of its inputs. The negative feedback factor is given by

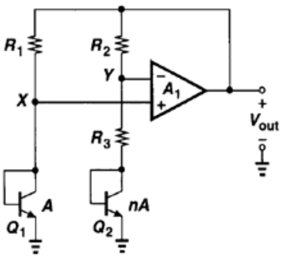
$$\beta_N = \frac{1/g_{m2} + R_3}{1/g_{m2} + R_3 + R_2}, \tag{11.31}$$

and the positive feedback factor by

$$\beta_P = \frac{1/g_{m1}}{1/g_{m1} + R_1}. \tag{11.32}$$

To ensure an overall negative feedback, β_P must be less than β_N, preferably by roughly a factor of two so that the circuit's transient response remains well-behaved with large capacitive loads.

Bandgap Reference ("issue 5/7") producing a reference voltage based on the bandgap voltage of silicon (E_g/q)



$$V_{REF} \approx V_{BE} + 17.2V_T \tag{11.20}$$

$$\approx 1.25\ \text{V}. \tag{11.21}$$

Bandgap Reference The voltage generated according to (11.20) is called a "bandgap reference." To understand the origin of this terminology, let us write the output voltage as

$$V_{REF} = V_{BE} + V_T \ln n \tag{11.33}$$

and hence:

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{BE}}{\partial T} + \frac{V_T}{T}\ln n. \tag{11.34}$$

Setting this to zero and substituting for $\partial V_{BE}/\partial T$ from (11.13), we have

$$\frac{V_{BE} - (4+m)V_T - E_g/q}{T} = -\frac{V_T}{T}\ln n. \tag{11.35}$$

If $V_T \ln n$ is found from this equation and inserted in (11.33), we obtain:

$$V_{REF} = \frac{E_g}{q} + (4+m)V_T. \tag{11.36}$$

Thus, the reference voltage exhibiting a nominally-zero TC is given by a few *fundamental* numbers: the bandgap voltage of silicon, E_g/q, the temperature exponent of mobility, m, and the thermal voltage, V_T. The term "bandgap" is used here because as $T \to 0$, $V_{REF} \to E_g/q$.

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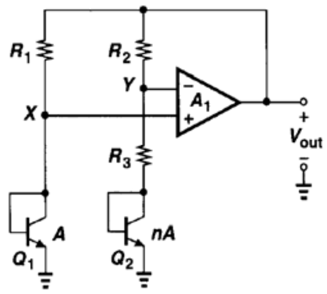
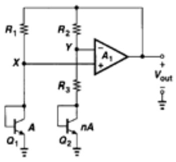
Supply Dependence and Start-Up ("issue 6/7")



- The output voltage is relatively independent of V_{dd} as long as the open loop gain (A_{OL} = $V_{out}/(V^{+} - V^{-})$) of the op amp is sufficiently high.
- A start-up mechanism may be required because if V_x and V_y are equal to zero, the differential input pair of the op amp may turn off.

Curvature correction ("issue 7/7")



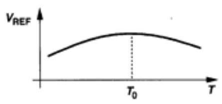


Figure 11.16 Curvature in temperature dependence of a bandgap voltage.

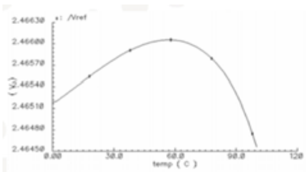
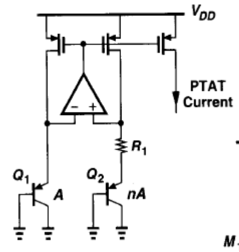


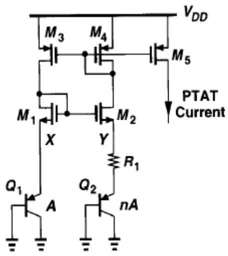
Figure 4 Output reference Verf vs. temperature.

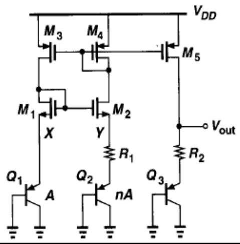
- The TC is typically zero at one temperature and positive or negative at others (due to temperature variation of base emitter voltages, collector currents and offset voltages).
- Curvature correction techniques are seldom used in CMOS (but used in bipolar impl.) due to offset- and process variations from sample to sample.

Figure 11.17 Variation of the zero-TC temperature for difference samples.

11.4 PTAT Current Generation (Fig. 11.18-11.20)



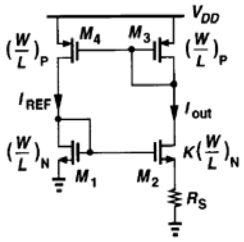




* The bias currents of the bipolar transistors are proportional to absolute temperature.
* Fig. 11.19: M_1-M_2 and M_3-M_4 are identical pairs, to ensure $V_x = V_Y \rightarrow I_{D1} = I_{D2} = V_T \ln n / R_1$
- The circuit in 11.19 may be modified to provide a BG-ref voltage as well (Fig. 11.20).
- Fig. 11.20

$$V_{REF} = V_{BE3} + \frac{R_2}{R_1} V_T \ln n, \qquad (11.37)$$

Constant Gm-biasing (11.5)



A simple circuit used to define the transconductance is the supply-independent bias topology of Fig. 11.3. Recall that the bias current is given by

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N} \frac{1}{R_S^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2. \qquad (11.38)$$

Thus, the transconductance of M_1 equals

$$g_{m1} = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_N I_{D1}} \qquad (11.39)$$

$$= \frac{2}{R_S}\left(1 - \frac{1}{\sqrt{K}}\right). \qquad (11.40)$$

- Often desirable to bias transistors so that noise, small signal gain and speed is not affected by transconductance variations
- Transconductance may be defined by the topology from Fig. 11.3
- In real life, R_S does vary with temperature and process.
- If the temperature coefficient of the resistor is known, bandgap and PTAT reference generation techniques can be utilized to cancel the temperature dependence. Process variations, however, limit the accuracy with which the transconductance is defined.
- If having a precise clock → SC impl.

Constant Gm-biasing by Switched Capacitor ”resistor”

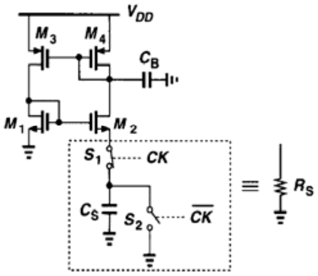


Figure 11.21 Constant-G_m biasing by means of a switched-capacitor “resistor.”

- Precise clock frequency must be available
- Change R with Switched Capacitor (”SC”) equivalent
- May give more compact realization

Outline – Tuesday, February 1st

11.1 General considerations
11.2 Supply-independent biasing
11.3 Temperature-independent References
    11.3.1 Negative TC-voltage
    11.3.2 Positive TC-voltage
    11.3.3 Bandgap reference
11.4 PTAT Current generation
11.5 Constant-Gm Biasing (?)

12.2 Sampling Switches
12.3 Switched Capacitor amplifiers (?)

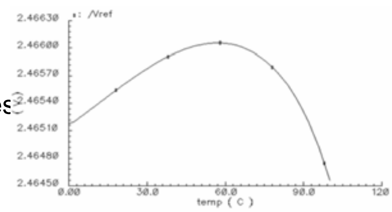


Figure 4 Output reference Verf vs. temperature.

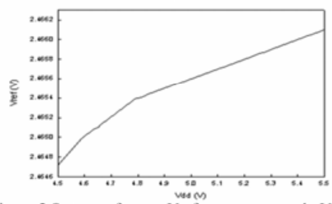


Figure 5 Output reference Vref vs. power supply Vdd.

A High Precision Curvature Compensated Bandgap Reference without Resistors

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* Email: chenjianghua@ime.pku.edu.cn

Introduction to Switched Cap. Circuits (ch. 12 in ”Razavi”)

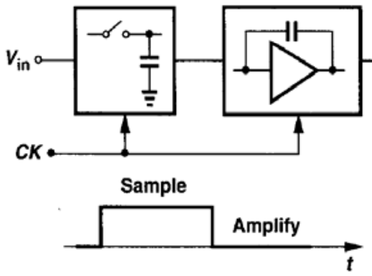


Figure 12.7 General view of switched-capacitor amplifier.

- Continous time processing, examples: audio, video, analog systems.
- ”Sample-data / discrete time”; The input is sampled at periodic instants of time, ignoring its value at other times. The circuit then processes each ”sample” producing a valid output at the end of each period.
- Switched capaitor circuits are used in filters, comparators, ADCs and DACs.

MOSFETs as switches (ch. 12.2 in ”Razavi”)

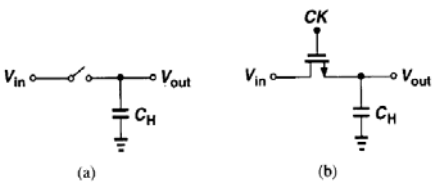


Figure 12.8 (a) Simple sampling circuit, (b) implementation of the switch by a MOS device.

- Nice properties of MOS transistors as switches;
- Can be on while carrying zero current

  The source and drain need not follow the gate voltage (not the case with bipolar transistors, typically necessitating complex bipolar circuits for sampling)
- Used widely in SC-filters, Sample-and-Hold circuits, ADCs and DACs (both Nyquist and oversampling converters)

Track (/sample-) and Hold capabilities of a sampling circuit (ch. 12.2 in "Razavi")

- Nice properties of MOS

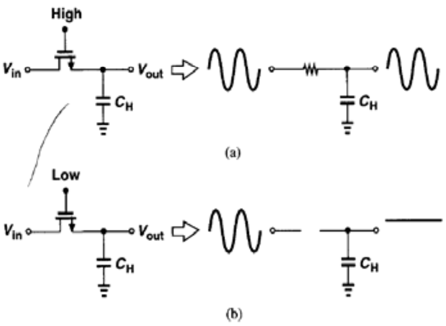
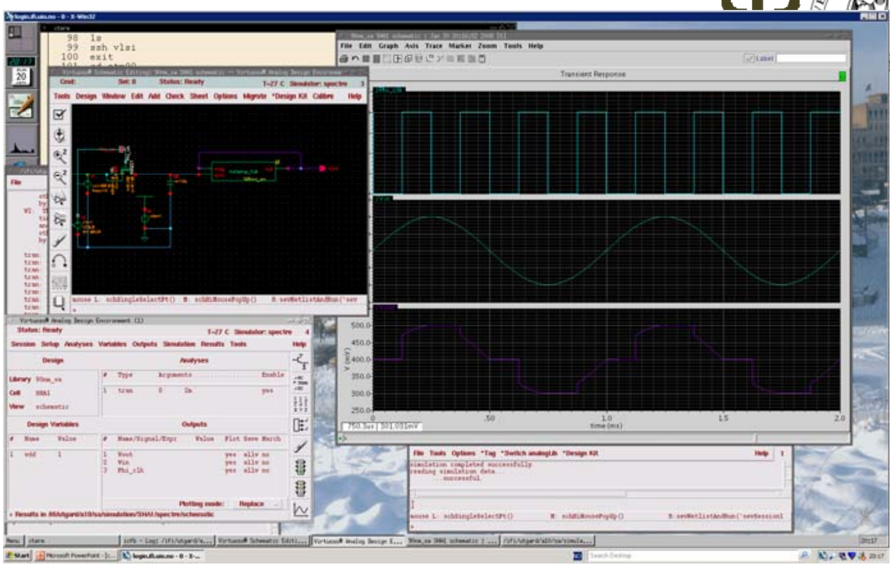


Figure 12.10 Track and hold capabilities of a sampling circuit.

Schematic entry and simulations in Cadence



Next week:

- Sample and Hold circuits, Data converter fundamentals
- Messages are given on the INF4420 homepage.
- Questions: sa@ifi.uio.no , 22852703 / 90013264