Sampling switches, charge injection, Nyquist data converter fundamentals

Tuesday, February 8th, 9:15 – 11:35

Snorre Aunet (sa@ifi.uio.no)
Nanoelectronics group
Department of Informatics
University of Oslo

Last week – Tuesday, February 1st

11.1 General considerations
11.2 Supply-independent biasing
11.3 Temperature-independent References
   11.3.1 Negative TC-voltage
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   11.3.3 Bandgap reference
11.4 PTAT Current generation
11.5 Constant-Gm Biasing

12.2 Sampling Switches
12.3 Switched Capacitor amplifiers
Today, February the 8th

- 12.2 Sampling switches
- 12.2.1 MOSFETS as Switches
- 12.2.2 Speed considerations
- 12.2.3 Precision considerations
- 12.2.4 Charge injection cancellation
- 12.3 Switched-Capacitor Amplifiers
  - 12.3.1 Unity-Gain Sampler / buffer
  - 12.3.2 Noninverting amplifier
  - 12.3.3 Precision Multiply-by-Two Circuit
- 12.4 Switched-Capacitor Integrator
- 12.5 SC common-mode feedback
- Data converter fundamentals
  ("Maloberti"+++)

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Track (/sample-) and Hold capabilities of a sampling circuit
12.2 in "Razavi"

Figure 12.10 Track and hold capabilities of a sampling circuit.
S/H signals (clk, $V_{in}$, $V_{CH}$, $V_{out}$)

**Track (/sample-) and Hold capabilities of a sampling circuit**

1/2 (ch. 12.2 in "Razavi")

- CK goes high at $t = t_0$, $V_{in} = 0$ for $t \geq 0$. $C_H$ initially has a voltage equal to $V_{dd}$.
- At $t = t_0$, $M_1$ operates in **saturation**, but falls into the **triode** region after some time, when $V_{out} = V_{dd} - V_{TH}$. Discharging continues until $V_{out}$ approaches zero.
- Current when in **saturation**:
  \[ I_{DS} = \frac{\mu C_{ox} W}{2L} (V_{DD} - V_{TH})^2 \]
Track (/sample-) and Hold capabilities of a sampling circuit

II/II (ch. 12.2 in "Razavi")

• CK goes high at $t = t_0$, when $V_{out} = 0$ V, and $V_{dd} = 3$ V.
• $M_1$'s source is connected to $C_H$, and the transistor turns on with $V_{GS} = 3$ V, but $V_{DS} = 1$ V. Thus, $M1$ operates in the triode ("linear") region, charging $C_H$ until $V_{out}$ approaches 1 V.

A couple of observations regarding the MOS switch

(ch. 12.2 in "Razavi")

• We have seen that a MOS switch can conduct current in either direction simply by exchanging the role of the source and drain terminals.
• When the switch is on, $V_{out}$ follows $V_{in}$.
• When the switch is off, $V_{out}$ remains constant (Fig 12.10 b)).
(Ex. 12.2 in "Razavi") Vout as a function of time, for Fig. 12.9 (a) 
(λ = 0)

\[ V_{out}(t) = \frac{2 \cdot \lambda \cdot \lambda I_C}{\lambda \cdot \lambda I_C - 2} \]

Solution:

\[ V_{out}(t) = V_{DD} - \frac{2 \cdot \lambda \cdot \lambda I_C}{\lambda \cdot \lambda I_C - 2} \]

Maximum output of NMOS S/H (ch. 12.2 in "Razavi", pp. 412)

- Assume \( V_{in} = V_{DD} \) (for the circuit from Fig. 12.9 b))
- \( V_{gs} = V_{dd}, \) initially : \( V_{DS} = V_{DD} \rightarrow V_{DS} \geq V_{GS} - V_{TH} : \) saturation
- \( T \) goes, \( V_{out} \rightarrow V_{DD} - V_{TH} \) (since the "overdrive" voltage vanishes and the current available for charging \( C_H \) go to negligible values)
- But: Given enough time, \( V_{out} \) will approach \( V_{DD} \) due to subthreshold currents conducted by the transistor.
- Serious limitation: If the input signal is close to \( V_{DD} \), the output provided by an NMOS switch cannot track the input (fast enough – remember subthreshold conduction).
- Similar problem with PMOS.
Ex. 12.3  \textbf{R}_{on} \text{ variation in sampling switch (ch. 12.2 in "Razavi")}

- Time for the output to settle within a given accuracy (ex. 0.1 \%) depends on the input voltage \( (T = \text{R}_{on}\text{C}) \).

- MOS devices operating in deep triode region are sometimes called zero-offset switches to emphasize that they exhibit no dc shift between the input and output voltages.

- Nonexistent in bipolar technology, the zero offset property proves crucial in precise sampling of analog signals.

\begin{equation}
\Delta V 
\end{equation}

Ex. 12.3  \textbf{Sampling speed considerations}

- \textbf{Speed}: Time from zero to maximum input level after the switch turns on, or more relevant: time to settle within a certain "error band", \( \Delta V \).

- Sampling speed is given by the on-resistance of the switch and the value of the sampling capacitor.

- \( R_{on} \) depends on input level, giving a greater time constant for more positive inputs (in the case of NMOS switches).
D/A (DAC) settling time and sampling rate

- In a DAC the **setting time** is defined as the time it takes for the converter to settle within some specified amount of the final value (usually 0.5 LSB).
- The **sampling rate** is the rate at which samples can be continuously converted and is typically the inverse of the settling time.

**Ex. 12.3** Complimentary MOS switch

- NMOS on resistance increases as the input voltage becomes more positive (and vice versa)
- PMOS on-resistance has the opposite behaviour and decreases as the input voltage becomes more positive.
- Combine PMOS and NMOS for complementary switches and rail-to-rail swings (when needed).
Complementary switches need complementary clocks

- The complementary switch reveals much less variation in on-resistance than that corresponding to each switch alone.
- For high-speed input signals the PMOS and NMOS switches must turn off simultaneously. (If for example the NMOS turns off $\Delta t$ seconds earlier than the PMOS, the output voltage tends to track the input for the remaining $\Delta t$ seconds, giving rise to distortion in the sampled value.)

Fig. 12.18 shows a complementary clock generator for moderate precision.

A BiCMOS Sample-and-Hold for satellite communications

Source: Aasaar, Leif Helluma
**Department of Informatics, University of Oslo, Norway
**Norwegian Telecom Research, Kjeller, Norway

Summary

30 MHz is a commonly used intermediate frequency (IF) in satellite communication systems. Direct injection of this high frequency signal requires a very expensive ADC capable of operation at a clock rate near this frequency. However, a narrow-band 6-12 MHz can be filtered down to 6-4 MHz with a simple low-pass filtered at 11 MHz, thus undersampling allows conversion using a simple ADC with an accuracy of 0-8 bits. This ADC can be realized in CMOS with low area and power consumption.

This configuration has lower requirements on the sample-and-hold. Two features needing special attention are analog input bandwidth and aperture uncertainty (jitter). Other important specifications include minimal harmonic distortion (THD), signal-to-noise plus distortion ratio (SNDR), and undersampling distortion (IRD).

A BiCMOS sample-and-hold consists of an input MOSFET switch, a hold capacitor and an output-gain output buffer. The high-band input frequency makes this an inadequate solution. The ON-resistance of this switch varies with the input level, resulting in variations in timing and phase, hence distortion. Limited slew rate on the switch gate voltage combined with a high dV/dt for the input signal also introduce uncertainties.

BiCMOS offers the possibility of designing a practical sample-and-hold with good performance and a lower component count. A BiCMOS sample and hold circuit has been made with a special effort to overcome problems concerning the high analog input frequency. The input switch is implemented as a double-pulse gate controlled switch. In simple terms this switch works as an input/buffer hold mode with the buffer being held by a high input current and the input voltage being sampled simultaneously. The output buffer and the data hold line have been implemented with BiCMOS. A 1-bit current-sharing DAC switches between the sample and hold mode, turning current on and off in a saw-tooth-shaped waveform. With this configuration an input bandwidth of 8 MHz with a 3.5 pF load capacitor has been obtained. Input sampling rates are limited to 2.4 MHz. The current has been implemented in a 2 micron BiCMOS technology offered by Hammar. The active area is 0.03 mm$^2$ and the circuit consumes approximately 20 mW.

- 2 µm BiCMOS, 1993
- "...A traditional CMOS Sample-and-Hold contains an input MOSFET switch, a hold capacitor and an unity-gain buffer. The high analog input frequency makes this an inadequate solution. The ON-resistance of the switch varies with the input level, resulting in variation in magnitude and phase, hence distortion. Limited slew rate on the switch gate voltage combined with a high dV/dt for the input signal also introduce aperture uncertainty (jitter)…" 8. februar 2011
**Charge injection due to channel capacitance**

- When the clock signal goes low, the charge is distributed equally between the drain and source of M1.
- is linearly related to $V_{\text{th}}$, resulting in a gain error for the S/H.

There is also a linear relationship to $V_{\text{th}}$, which is nonlinearly related to $V_{\text{in}}$ (through $V_{\text{sb}}$) resulting in distortion for the overall S/H.
- Equal distribution (S/D) imprecise; worst-case: all charge to one node.

**Charge injection leads to gain error, dc offsets and nonlinearity**

- In reality the fraction of charge that exits through the source and drain terminals is a relatively complex function of various parameters such as impedance seen at each terminal to ground and the transition time of the clock. No good rule of thumb.
- Most circuit simulators model charge injection quite inaccurately.
- The assumed linear function of the input voltage, leading to gain error and dc offset (only) is imprecise, due to nonlinear behaviour of $V_{\text{th}}$ upon $V_{\text{in}}$. 

\[
Q_{\text{ch}} = WL C_{\text{int}} (V_{\text{dd}} - V_{\text{in}} - V_{\text{th}}).
\]

\[
\Delta V = \frac{WL C_{\text{int}} (V_{\text{dd}} - V_{\text{in}} - V_{\text{th}})}{2C_{G}}.
\]

\[
V_{\text{out}} = V_{\text{in}} - \frac{WL C_{\text{int}} (V_{\text{dd}} - V_{\text{in}} - V_{\text{th}})}{C_{G}}.
\]
Clock feedthrough

- Clock transitions are coupled through gate-drain and gate-source overlap capacitances.
- The error, $\Delta V$, is independent of the input level, manifesting itself as a constant offset in the input/output characteristic.

\[
\Delta V = V_{CK} \frac{WC_{ov}}{WC_{ov} + C_H},
\]

kT/C noise

- A resistor charging a capacitor gives rise to a total rms noise voltage of $\text{SQRT (kT/C)}$.
- The noise gets stored on the capacitor along with the instantaneous value of the input voltage.
- In order to achieve low noise the sampling capacitor must be sufficiently large, thus loading other circuits and degrading the speed.
Charge injection cancellation

Fig. 12.24: The deposited channel charge is absorbed by the latter.

Dimension \( W_2 = 0.5W_1 \) and \( L_1 = L_2 \). But: The approach is not very attractive as the underlying assumption of equal splitting between S and D is generally invalid.

- Fig. 12.26: Attempts to match dimensions leads to cancellation for only one input level.
- Better: **differential operation** (Fig. 12.27) Charge inj. Is common mode disturbance. Nonlinearity of body effect leads to odd order distortion.
- Charge injection limits the speed precision envelope in sampled-data systems.
Some systems exploiting data converters, "Allen & Holberg"

Different ADCs depending on needs

Which ADC Architecture Is Right for Your Application?

By Walt Kester (walt.kester@analog.com)
Main data converter types:

- Nyquist-rate converters:
  - Each value has a one-to-one correspondence with a single input
  - The sample-rate must be at least equal to twice the signal frequency (Typically somewhat higher)

- Oversampled converters:
  - The sample-rate is much higher than the signal frequency, typically 20 – 512 times.
  - The extra samples are used to increase the SNR
  - Often combined with noise shaping

Nyquist Sampling, Oversampling, Noise Shaping

- Figure from [Kest05]
- Straight over-sampling gives an SNR improvement of 3 dB / octave
- \( fs > 2f_0 \) \((2f_0 = \text{Nyquist Rate})\)
- \( \text{OSR} = \frac{f_s}{2f_0} \)
- \( \text{SNR}_{\text{max}} = 6.02N + 1.76 + 10\log(\text{OSR}) \)
Flash ADC from 1926 (Analog Digital Conversion handbook, Analog Devices)

The few documented flash converters are part of Paul M. Reaney's electrochemical PCM telegraphic systems described in a relatively opulent patent filed in 1921 (Reference 1—see further discussion in Chapter 1 of this book). In the ADC, a current proportional to the intensity of light drives a galvanometer which in turn moves a beam of light which activates one of 32 individual photocells, depending upon the amount of galvanometer deflection (see Figure 3.49). Each individual photocell output across part of a string network which produces the final binary code.

Figure 3.48: A 5-bit Flash ADC Proposed by Paul Reaney
Adapted from Paul M. Reaney, "Facsimile Telegraph System," U.S. Patent 1,808,527, Filed July 20, 1921, Issued November 30, 1926

Ideal D/A converter

\[ B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N} \]

\[ V_{out} = V_{ref} (b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) \]
Example: 8-bit D/A converter

An ideal D/A converter has

\[ V_{\text{ref}} = 5 \text{ V} \]

Find \( V_{\text{out}} \) when

\[ B_{\text{in}} = 10110100 \]

\[ B_{\text{in}} = 2^{-1} + 2^{-3} + 2^{-4} + 2^{-6} = 0.703125 \]

\[ V_{\text{out}} = V_{\text{ref}}B_{\text{in}} = 3.516 \text{ V} \]

Find \( V_{\text{LSB}} \)

\[ V_{\text{LSB}} = 5/256 = 19.5 \text{ mV} \]

Ideal A/D converter (Fig. 11.3)

\[ V_{\text{ref}}(b_12^{-1} + b_22^{-2} + \ldots + b_N2^{-N}) = V_{\text{in}} \pm V_x \]

where

\[ -\frac{1}{2}V_{\text{LSB}} \leq V_x < \frac{1}{2}V_{\text{LSB}} \]
Ideal transfer curve for a 2-bit A/D converter (Fig. 2.2)

- A range of input values produce the same output value (Quantization error)
- Different from the D/A case

Quantization noise ("J&M" + "M")

\[ V_Q = V_1 - V_{\text{in}} \]
Quantization noise model

• The model is exact as long as Vq is properly defined
• Vq is most often assumed to be white and uniformly distributed between +/- Vlsb/2

Quantization noise

• The rms-value of the quantization noise can be shown to be:
  \[ V_{Q_{\text{rms}}} = \frac{V_{\text{LSB}}}{\sqrt{2}} \]
• Total noise power is independent of sampling frequency
• In the case of a sinusoidal input signal with p-p amplitude of \( V_{\text{ref}}/2 \):
  \[ \text{SNR} = 20 \log \left( \frac{V_{\text{in_{rms}}}}{V_{Q_{\text{rms}}}} \right) = 20 \log \left( \frac{V_{\text{ref}}/\sqrt{2}}{V_{\text{LSB}}/\sqrt{2}} \right) \]
  \[ \text{SNR} = 20 \log \left( \frac{V_{\text{ref}}}{V_{\text{LSB}}} \right) = 20 \log \left( \frac{2}{\sqrt{2}} \right) \]
  \[ \text{SNR} = 6,02N + 1,76 \text{ dB} = \]
Quantization noise

- Signal-to-Noise ratio is highest for maximum input signal amplitude

Signed codes

- Unipolar / bipolar
- Common signed digital rep.: sign magnitude, 1’s complement, 2’s compl.
- 1’s compl.: Neg. Numbers are complement of all bits for equiv. Pos. Number: 5:0101, -5:1010
- Offset bin: 0000 to the most neg., and then counting up..
  +: closely related to unipolar through simple offset
2's complement

- $5_{10} : 0101 = 2^2 + 2^0$
- $-5_{10} : (0101)' +1 = 1010 + 1 = 1011$

- Addition of positive and negative numbers is straightforward, using addition, and requires little hardware
- 2's complement is most popular representation for signed numbers when arithmetic operations have to be performed

<table>
<thead>
<tr>
<th>Decimal</th>
<th>Sign magnitude</th>
<th>2’s complement</th>
</tr>
</thead>
<tbody>
<tr>
<td>0111</td>
<td>+7</td>
<td>+7</td>
</tr>
<tr>
<td>0110</td>
<td>+6</td>
<td>+6</td>
</tr>
<tr>
<td>0111</td>
<td>+5</td>
<td>+5</td>
</tr>
<tr>
<td>0110</td>
<td>+4</td>
<td>+4</td>
</tr>
<tr>
<td>0011</td>
<td>+3</td>
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<td>0010</td>
<td>+2</td>
<td>+2</td>
</tr>
<tr>
<td>0001</td>
<td>+1</td>
<td>+1</td>
</tr>
<tr>
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<td>0</td>
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<td>-0</td>
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<td>-2</td>
<td>-6</td>
</tr>
<tr>
<td>1011</td>
<td>-3</td>
<td>-5</td>
</tr>
<tr>
<td>1100</td>
<td>-4</td>
<td>-4</td>
</tr>
<tr>
<td>1101</td>
<td>-5</td>
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<tr>
<td>1110</td>
<td>-6</td>
<td>-2</td>
</tr>
<tr>
<td>1111</td>
<td>-7</td>
<td>-1</td>
</tr>
</tbody>
</table>

$7_{10} - 6_{10}$ via addition using two’s complement of -6

- $0000 0000 0000 0000 0000 0000 0000 0000 0111_2 = 7_{10}$
- $0000 0000 0000 0000 0000 0000 0000 0000 0110_2 = 6_{10}$
- Subtraction uses addition: The appropriate operand is negated before being added
- Negating a two’s complement number: Simply invert every 0 and 1 and add one to the result. Example:
  - $0000 0000 0000 0000 0000 0000 0000 0000 0110_2$ becomes $1111 1111 1111 1111 1111 1111 1111 1111 1010_2$
  - $1111 1111 1111 1111 1111 1111 1111 1111 1001_2 + 1_2$
  
  $= 1111 1111 1111 1111 1111 1111 1111 1111 1010_2$

- $0000 0000 0000 0000 0000 0000 0000 0000 0111_2 = 7_{10}$
- $+ 1111 1111 1111 1111 1111 1111 1111 1111 1010_2 = -6_{10}$

$= 0000 0000 0000 0000 0000 0000 0000 0000 0001_2 = 1_{10}$
### Performance Limitations

- Resolution
- Offset and gain error
- Accuracy
- Integral nonlinearity (INL) error
- Differential nonlinearity (DNL) error
- Monotonicity
- Missing codes
- A/D conversion time and sampling rate
- D/A settling time and sampling rate
- Sampling time uncertainty
- Dynamic range

NB! Different meanings and definitions of performance parameters sometimes exist. Be sure what’s meant in a particular specification or scientific paper. There are also more than those mentioned here.

### Resolution

- Resolution usually refers to the number of bits in the input (D/A) or output (ADC) word, and is often different from the accuracy.

Analog-Digital Conversion Handbook, Analog Devices, 3rd Edition, 1986: *An n-bit binary converter should be able to provide 2n distinct and different analog output values corresponding to the set of n binary words. A converter that satisfies this criterion is said to have a resolution of n bits.*

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**Table 1:**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion rate</td>
<td>1000kHz</td>
</tr>
<tr>
<td>Full-scale input</td>
<td>±1V</td>
</tr>
<tr>
<td>Resolution</td>
<td>12b</td>
</tr>
<tr>
<td>Total harmonic distortion</td>
<td>75ppm</td>
</tr>
<tr>
<td>ENOB (100kHz)</td>
<td>7.58b</td>
</tr>
<tr>
<td>SNR (100kHz)</td>
<td>52.1dB</td>
</tr>
<tr>
<td>THD (100kHz)</td>
<td>0.006%</td>
</tr>
<tr>
<td>LSB (100kHz)</td>
<td>1.6mV</td>
</tr>
</tbody>
</table>

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**Figure 8:** SFDR, ENOB, and SNR versus conversion rate. The input frequency and signal setting are 100kHz and 10mVpp, respectively.
Litterature

- Johns & Martin: "Analog Integrated Circuit Design"
- Franco Maloberti: "Data Converters"

Next week:

- Data converter fundamentals, among them some principles especially relevant for your project.
- Messages are given on the INF4420 homepage.
- Questions: sa@ifi.uio.no, 22852703 / 90013264
Transistor stuff.

- **Saturation**: $V_{gs} \geq V_{th}$, $V_{ds}$ sufficiently high so that $V_{gd} < V_{th}$; $V_{ds} \geq (V_{gs} - V_{th})$

- **Triode**: $V_{gs} \geq V_{th}$, $V_{ds}$ sufficiently high so $V_{gd} < V_{th}$

- **Cutoff / subthreshold**: $V_{gs} < V_{th}$