Data converter fundamentals

Tuesday, February 15th, 9:15 – 12:00

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Nanoelectronics group
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Last time, February the 8th

- 12.2 Sampling switches
- 12.2.1 MOSFETS as Switches
- 12.2.2 Speed considerations
- 12.2.3 Precision considerations
- 12.2.4 Charge injection cancellation
- 12.3 Switched-Capacitor Amplifiers
- 12.3.1 Unity-Gain Sampler / buffer
- 12.3.2 Noninverting amplifier
- 12.3.3 Precision Multiply-by-Two Circuit
- 12.4 Switched-Capacitor Integrator
- 12.5 SC common-mode feedback
- Data converter fundamentals ("Maloberti"++)

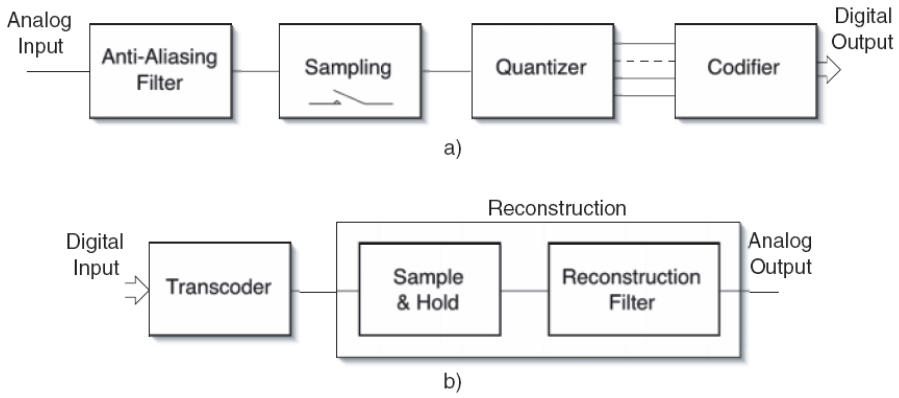
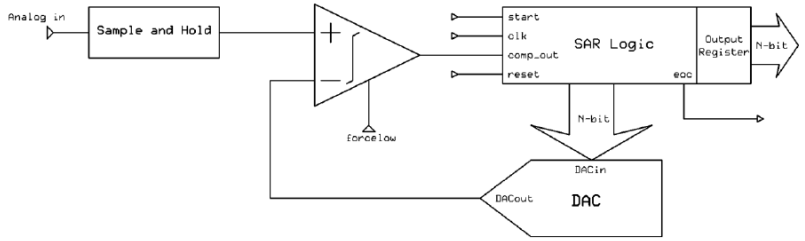
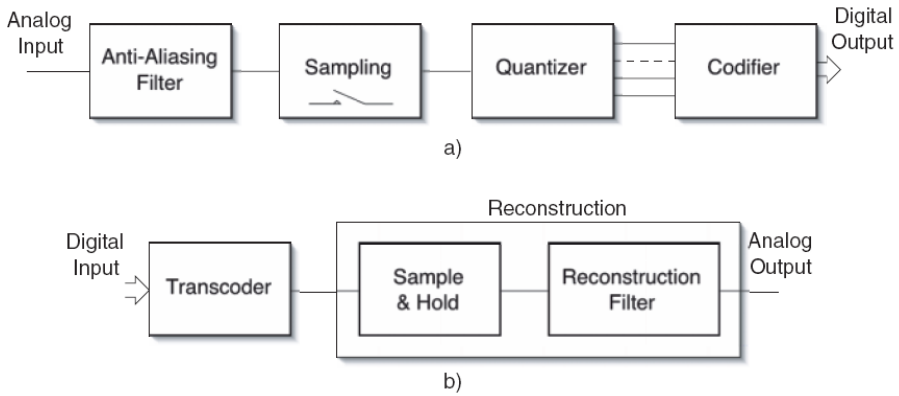


Figure 1.1. Block diagram of the basic functions of an A/D (a) and a D/A (b) converter.



Today, February the 15th

- 1.1 The ideal data converter
- 1.2 Sampling
- 1.2.1 Undersampling
- 1.2.2 Sampling-time jitter
- 1.3 Amplitude Quantization
- 1.3.1 Quantization noise
- 1.3.2 Properties of the
- Quantization Noise
- 1.4 kT/C Noise
- 1.5 Discrete and Fast Fourier
- Transform
- 1.5.1 Windowing
- 1.6 Coding Schemes
- 1.7 The D/A Converter
- 1.7.1 Ideal reconstruction
- 1.7.2 Real Reconstruction
- 1.8 The Z-transform
- (The contents refer to
- ”Maloberti”)



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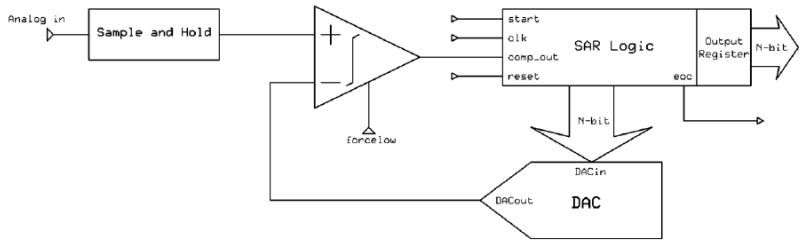


Data conversion (A/D and D/A) split into a series of steps

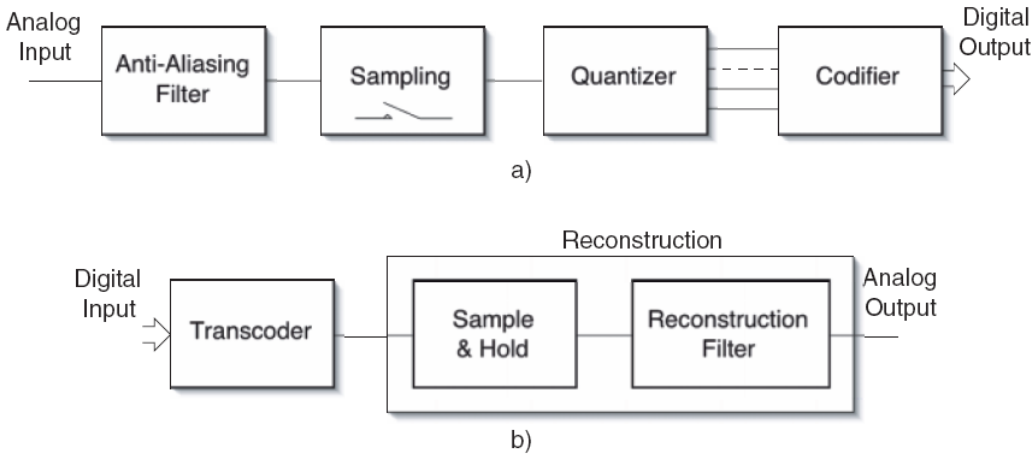
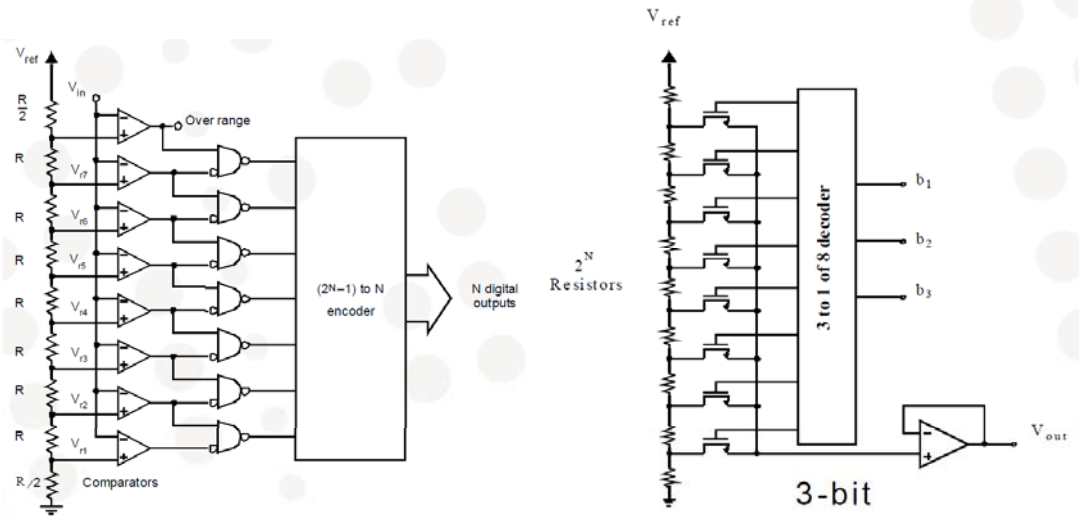


Figure 1.1. Block diagram of the basic functions of an A/D (a) and a D/A (b) converter.



- A/D conversion steps: continous-time anti-aliasing filtering→sampling→quantization→data coding.
- D/A conversion steps: transcoding→sample-and-hold→reconstruction filter

Sampling (chapter 1.2 in “Maloberti”)

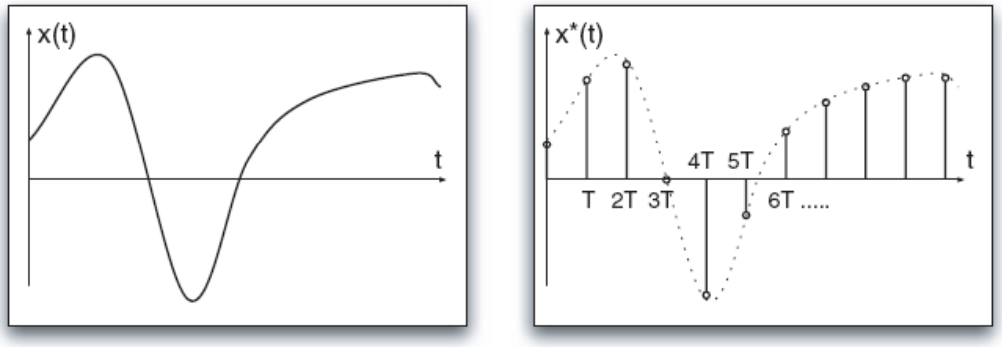
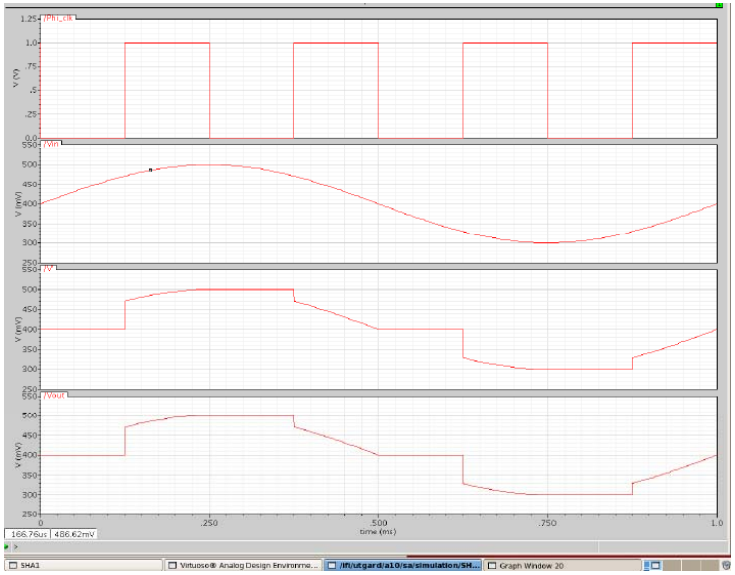


Figure 1.2. Continuous time signal (left) and its sampled data representation (right).

$$x^*(t) = x^*(nT) = \sum x(t)\delta(t - nT). \qquad (1.1)$$



- The output of the sampler is given by equation (1.1). The continous-time signal is transformed into it’s sampled-data equivalent. Practical circuits generates pulses with finite duration and amplitudes representing the input only at exact sampling times, nT (not only delta functions whose amplitude equals the input signal at the sampling times (See lecture notes 2011.02.08.)).
- Sampling a signal is equivalent to the mixing of the signal with a train of deltas.

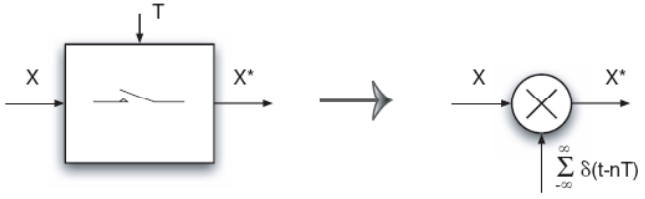


Figure 1.3. Ideal sampler and its non-linear equivalent processing.

Sampling (chapter 1 in “Maloberti”)

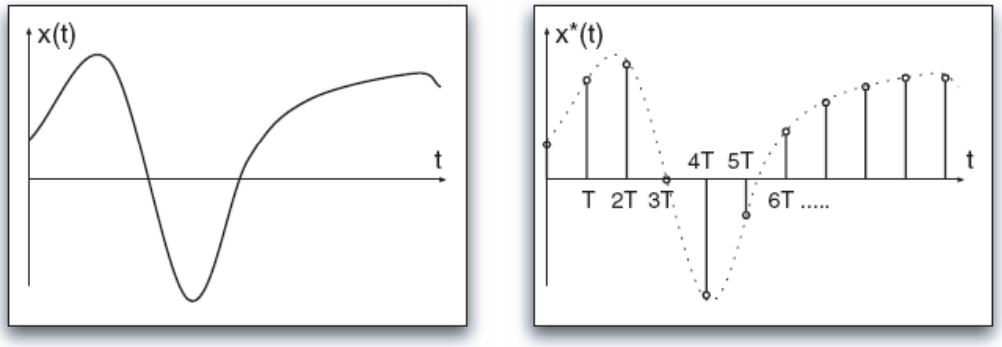


Figure 1.2. Continuous time signal (left) and its sampled data representation (right).

$$\mathcal{L}\left[\sum_{-\infty}^{\infty}\delta(t-nT)\right]=\sum_{-\infty}^{\infty}e^{-nsT}. \qquad (1.2)$$

The use of (1.1), (1.2) and the Laplace transform definition results in

$$\mathcal{L}\left[x^*(nT)\right]=\sum_{-\infty}^{\infty}(X(s-jn\omega_s)=\sum_{-\infty}^{\infty}x(nT)e^{-nsT}, \qquad (1.3)$$

- The Laplace transform of an infinite sequence of deltas is given by eq. (1.2).
- Eq. (1.3) provides useful expressions for the Laplace transform of the sampled output. The right-hand equation will be used to discuss relationships between the s-plane and the z-plane.

Sampling (chapter 1 in “Maloberti”)

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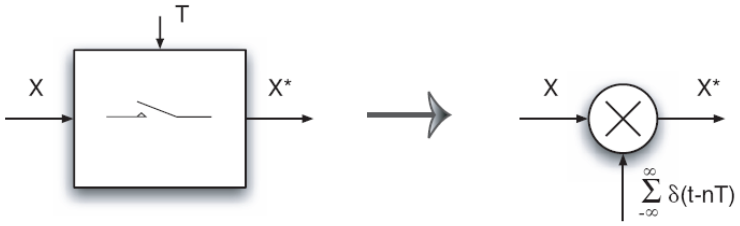
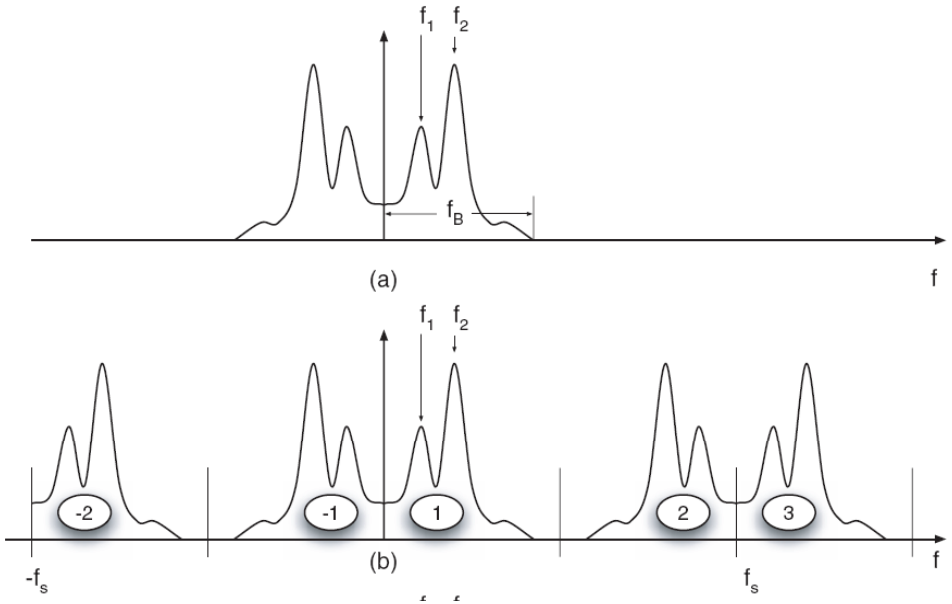


Figure 1.3. Ideal sampler and its non-linear equivalent processing.



- Eq. (1.3) shows that the spectrum of x*(nT) is the superposition of infinite replicas of the input spectrum. These replicas are centered at multiples of the sampling frequency being shifted along the f axis by nf_s (= n/T), n = 0,±1,±2,…, as a result, the spectrum being periodic with period f_s.

- Figure 1.4 a) shows the bilateral spectrum of a continous-time signal.

- Figure 1.4 b) shows the sampled spectrum using $f_s/2 > f_B$

Sampling and aliasing

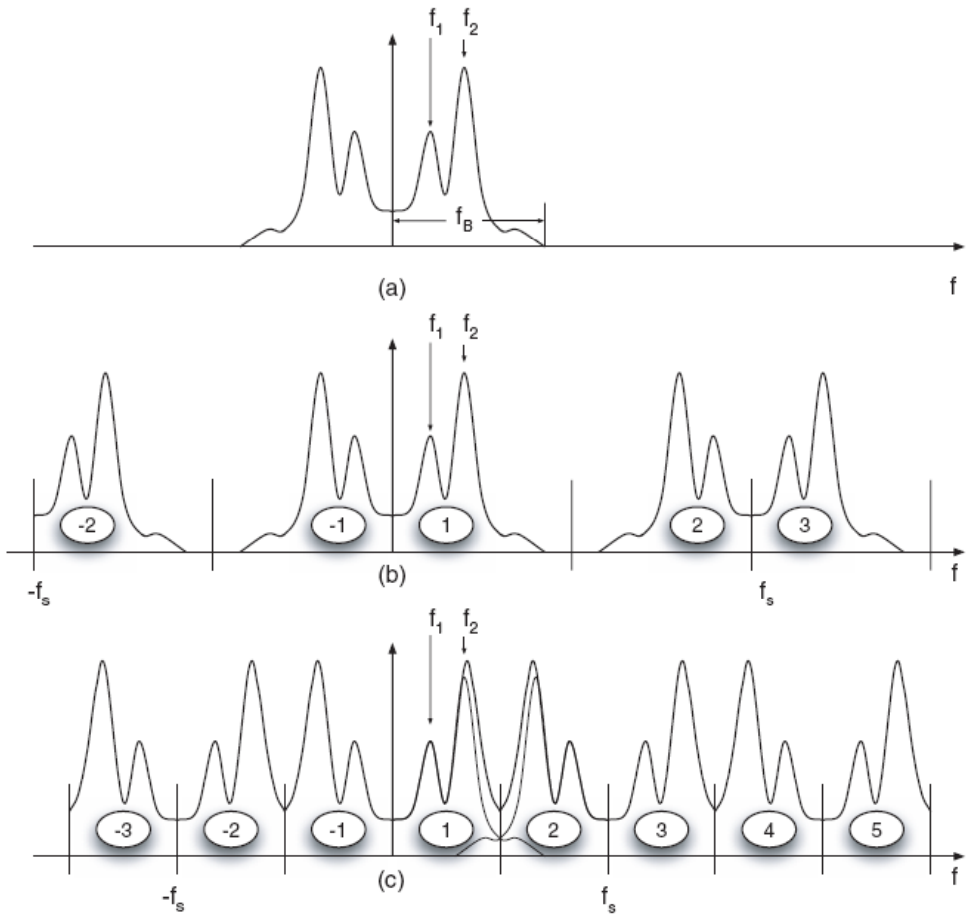


Figure 1.4. a) Bilateral spectrum of a continuous-time signal. b) Sampled spectrum by using $f_s/2 > f_B$. c) Sampled spectrum with $f_s/2 < f_B$.

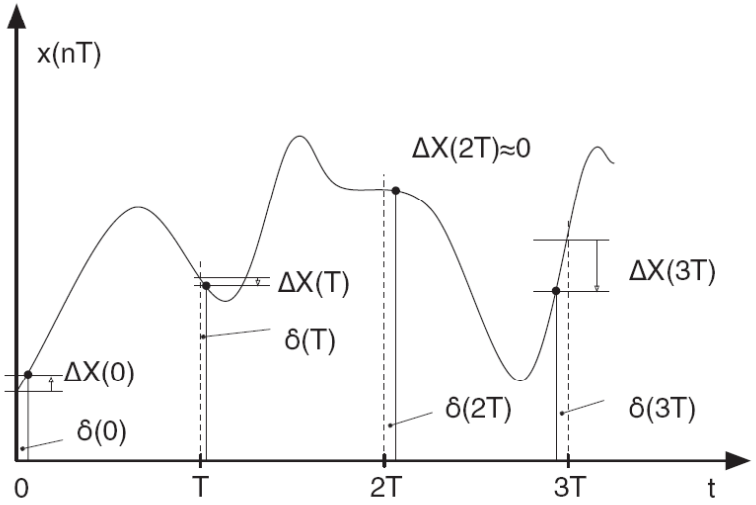
Figure 1.4 a) shows the bilateral spectrum of a continous-time signal.

Figure 1.4 b) shows the sampled spectrum using $f_s/2 > f_B$

The *sampling frequency must be at least twice the bandwidth of the input* for the replicas not to overlap (also for noise and interferences, that can have components at ”any” frequency).

It is necessary to remove out of band interferences whose folding could corrupt the signal band. This is done by an anti-aliasing filter that passes the band of interest and rejects the out of band interferences.

Sampling-time Jitter (ch. 1.2.2)



- Variations in sampling time from the ideal
- Ex: 8-bit converter sampling a 250 MHz sinusoidal mus keep its sampling time uncertainty under 5 ps to maintain 8-bit accuracy.

Figure 1.11. Errors caused by sampling time jitter.

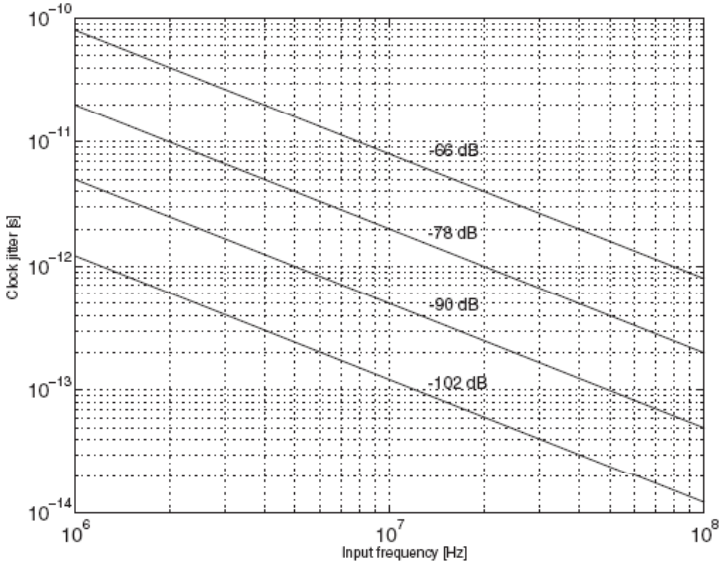


Figure 1.12. Clock jitter at different SNR and input frequencies.

Consider the following input signal: $V_{in} = \frac{V_{ref}}{2}\sin(2\pi f_{in} t)$

If the variation in sampling time is Δt , following equation must be satisfied to keep ΔV less than 1LSB

$$\Delta t < \frac{V_{LSB}}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}}$$

kT/C noise (chapter 1.4 in “Maloberti”)

Remember

The kT/C noise is a fundamental limit caused by sampling. Sampling any signal using 1 pF leads to 64.5 μV noise voltage. If the sampling capacitance increases by k the noise voltage diminishes by $\sqrt{k}$.

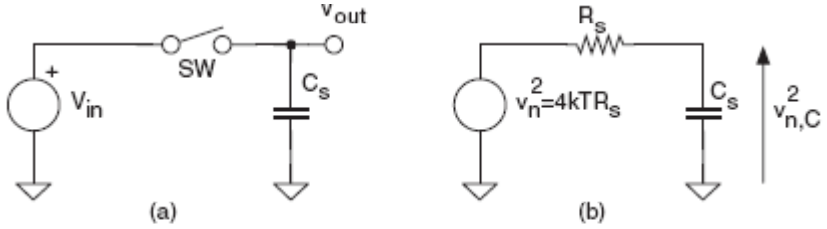


Figure 1.18. Simple model of a sampler and its noise equivalent circuit.

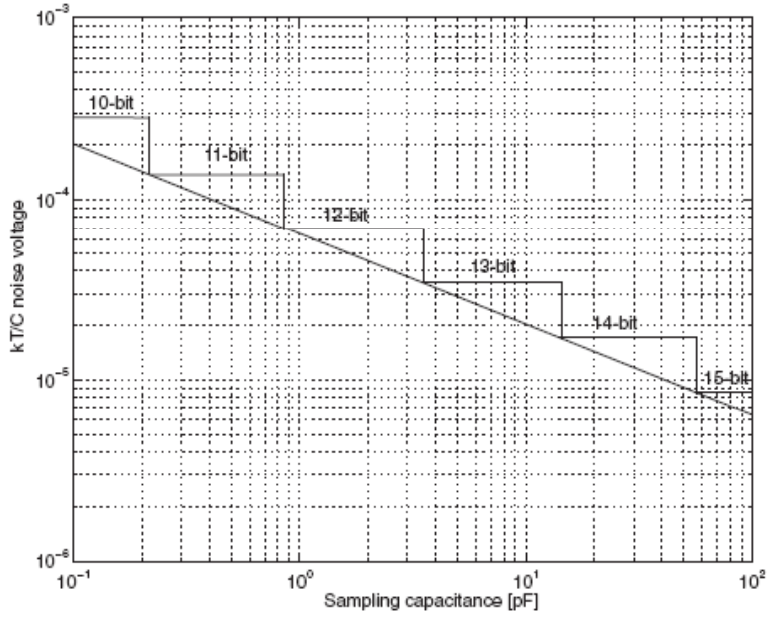


Figure 1.19. kT/C noise voltage versus the capacitance value. The staircase shows the quantization step for 1 V_{FS}.

$$v_{n,C_s}^2(\omega) = \frac{4kTR_s}{1+(\omega R_s C_s)^2}. \qquad (1.24)$$

$$P_{n,C_s} = \int_0^\infty v_{n,out}(f)df = 4kTR_s \int_0^\infty \frac{df}{1+(2\pi f R_s C_s)^2} = \frac{kT}{C_s}. \qquad (1.25)$$

- Unavoidable limit of data converters
- Goes to zero only for infinite sampling capacitance or zero temperature.
- The sampling operates correctly if the time constant $T_S = R_S C_S$ is negligible with respect to the sampling time.
- The bandwidth of the input signal must be much smaller than $1/T_S$.
- The spectrum of the thermal noise is white, = $4kTR_s$.
- The $R_S C_S$ network etsablishes a low-pass filtering that makes the noise spectrum accross the capacitor colored (Eq. 1.24).
- The noise power stored on C_S when the switch goes off is given by eq. 1.25

Coding schemes (ch. 1.6)

- **USB - Unipolar Straight Binary**: is the simplest binary scheme. It is used for unipolar signals. The USB represents the first quantization level, $-V_{ref} + 1/2V_{LSB}$ with all zero's $(\cdots 0000)$. As the digital code increases, the analog input increases by one *LSB* at a time, and when the digital code is at the full scale $(\cdots 1111)$ the analog input is above the last quantization level $V_{ref} - 1/2V_{LSB}$. The quantization range is $-V_{ref} \cdots + V_{ref}$.

CSB - Complementary Straight Binary: the opposite of the *USB*. *CSB* coding is also used for unipolar systems. The digital code $(\cdots 0000)$ represents the full scale while the code $(\cdots 1111)$ corresponds to the first quantization level.

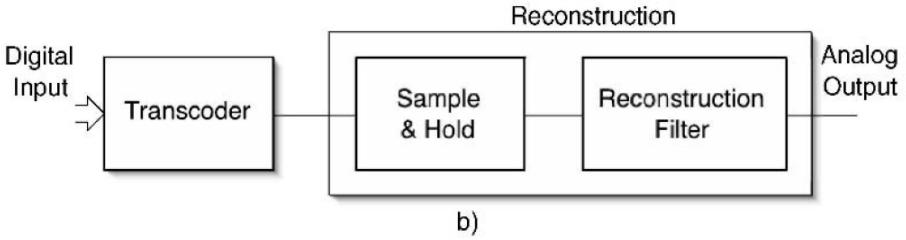
BOB - Bipolar Offset Binary: is a scheme suitable for bipolar systems (where the quantized inputs can be positive and negative). The most significant bit denotes the sign of the input: 1 for positive signals and 0 for negative signals. Therefore, $(\cdots 0000)$ represents the full negative scale. The zero crossing occurs at $(01 \cdots 111)$ and the digital code $(1 \cdots 1111)$ gives the full positive scale.

COB - Complementary Offset Binary: this coding scheme is complementary to the BOB scheme. All the bits are complemented and the meaning remains the same. Therefore, since $(01 \cdots 111)$ denotes the zero crossing in the BOB scheme the zero crossing of COB is becomes $(10 \cdots 000)$.

BTC - Binary Two's Complement: is one of the most used coding schemes. The bit in the *MSB* position indicates the sign in a complemented way: it is 0 for positive inputs and 1 for negative inputs. The zero crossing occurs at $(\cdots 0000)$. For positive signals the digital code increases normally for an increasing analog input. Thus, the positive full scale is $(0 \cdots 1111)$. For negative signals, the digital code is the two's complement of the positive counterpart. This leads $(1 \cdots 0000)$ to represent the negative full scale. The *BTC* coding system is suitable for microprocessor based systems or for the implementation of mathematical algorithms. It is also the standard for digital audio.

CTC - Complementary Two's Complement: is the complementary code of *BTC*. All the bits are complemented and codes have the same meaning. The negative full scale is $(0 \cdots 1111)$; the positive full scale is $(1 \cdots 0000)$.

The D/A converter (ch. 1.7)



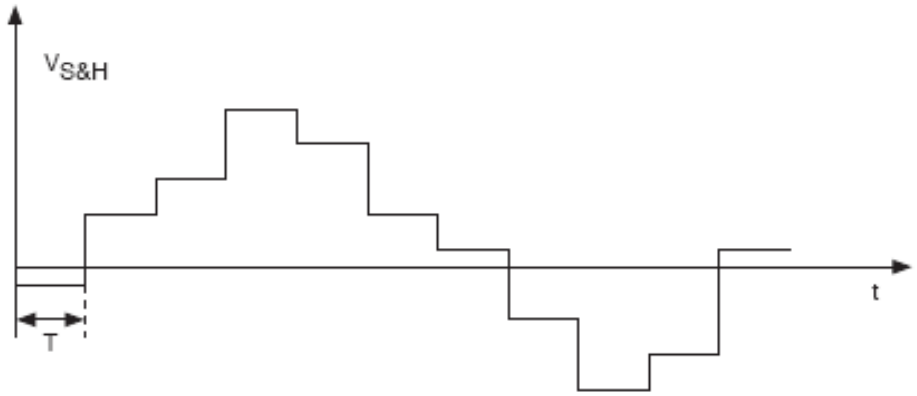


Figure 1.26. Signal waveform after the *S&H* of a *DAC* .

Ideally, reconstruction uses a filter with transfer function

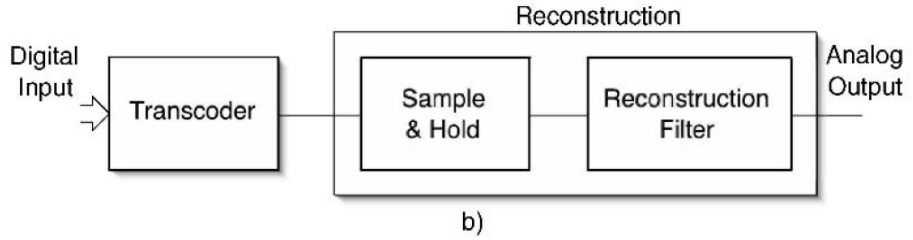
$$H_{R,id}(f) = 1 \quad for \quad -\frac{f_s}{2} < f < \frac{f_s}{2}$$
$$H_{R,id}(f) = 0 \quad otherwise. \qquad (1.37)$$

Unfortunately, the impulse response, $r(t)$, of the ideal reconstruction filter is

$$r(t) = \frac{sin(\omega_s t/2)}{(\omega_s t/2)} \qquad (1.38)$$

- The transcoder generates a sequence of pulses whose amplitude is the analog representation of the digital code. Then, the reconstruction process changes the sequence of pulses into a continous-time signal, obtained by the cascade of a S/H and a filter. The reconstruction filter smoothes the staircase-like waveform by removing high frequency components to obtain the analog result.
- An ideal reconstruction filter is not obtainable

Real reconstruction filters



$$H_{S\&H}(s) = \frac{1 - e^{-sT}}{s\tau}, \qquad (1.39)$$

where τ is a suitable gain factor whose dimension is time for making $H_{S\&H}$ dimensionless.

Equation (1.39) on the $j\omega$ axis becomes

$$H_{S\&H}(j\omega) = j\frac{T}{\tau}e^{-j\omega T/2}\,\frac{sin(\omega T/2)}{\omega T/2}, \qquad (1.40)$$

showing a phase shift proportional to ω and an amplitude attenuation proportional to the *sinc (=sin(x)/x)* function.

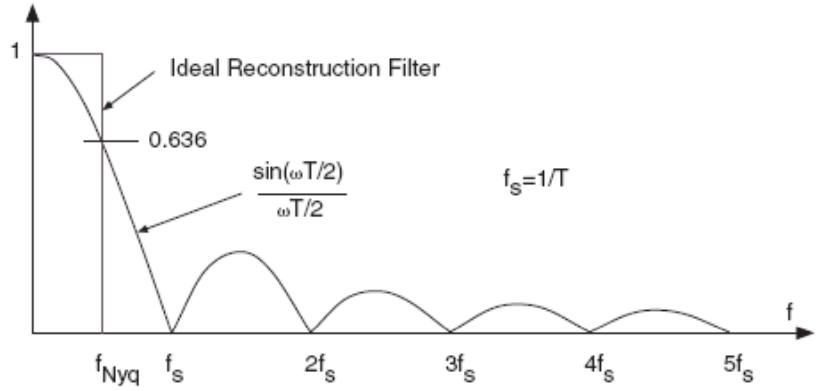


Figure 1.27. Amplitude response of the ideal and real sample-and-hold.

- A real reconstruction filter is an approximation of the ideal reconstruction response, given by eq. 1.39.
- On the jω axis equation 1.39 becomes as in eq. 1.40, showing a phase shift proportional to ω and an amplitude attenuation proportional to the sinc (= sin(x)/x) function.
- Fig. 1.27 include the ideal reconstruction filter as well as the sinc function.

Main data converter types:

- Nyquist-rate converters:
  - Each value has a one-to-one correspondencewith a single input
  - The sample-rate must be at least equal to twice the signal frequency (Typically somewhat higher)
- Oversampled converters:
  - The sample-rate is much higher than the signal frequency, typically 20 – 512 times.
  - The extra samples are used to increase the SNR
  - Often combined with noise shaping

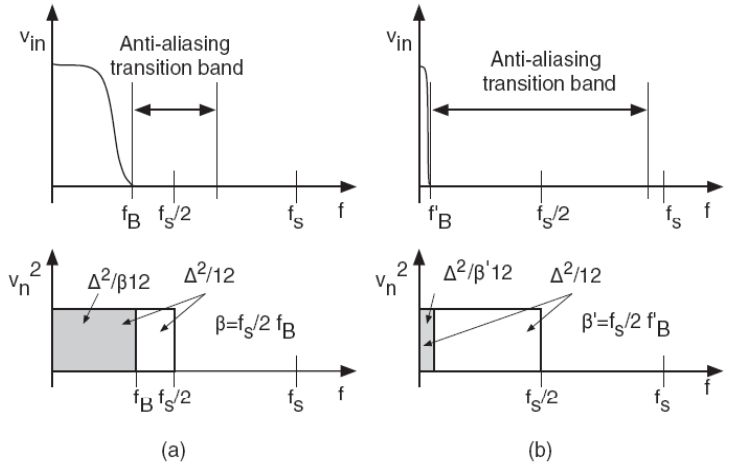


Figure 2.1. Comparing Nyquist-rate, (a), and oversampling, (b), strategies.

Different ADCs depending on needs

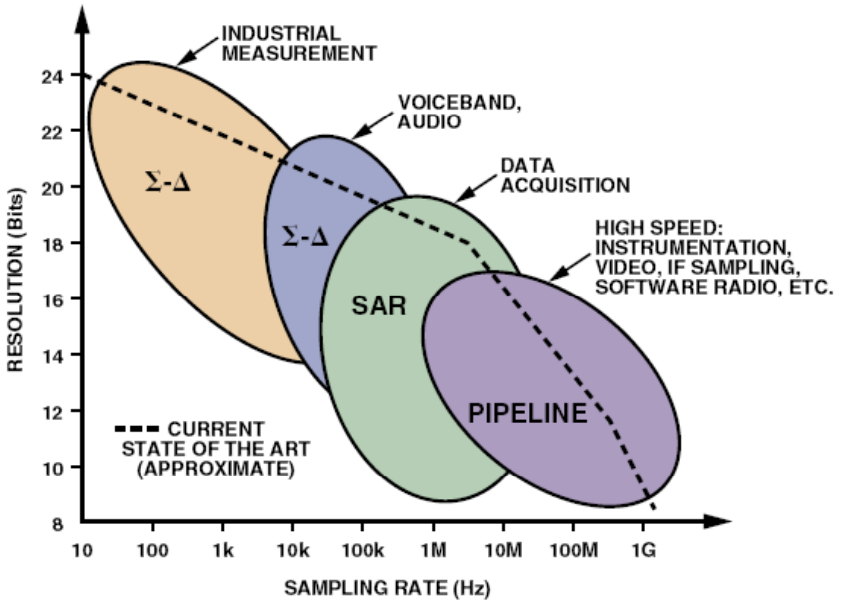


Figure 1. ADC architectures, applications, resolution, and sampling rates.

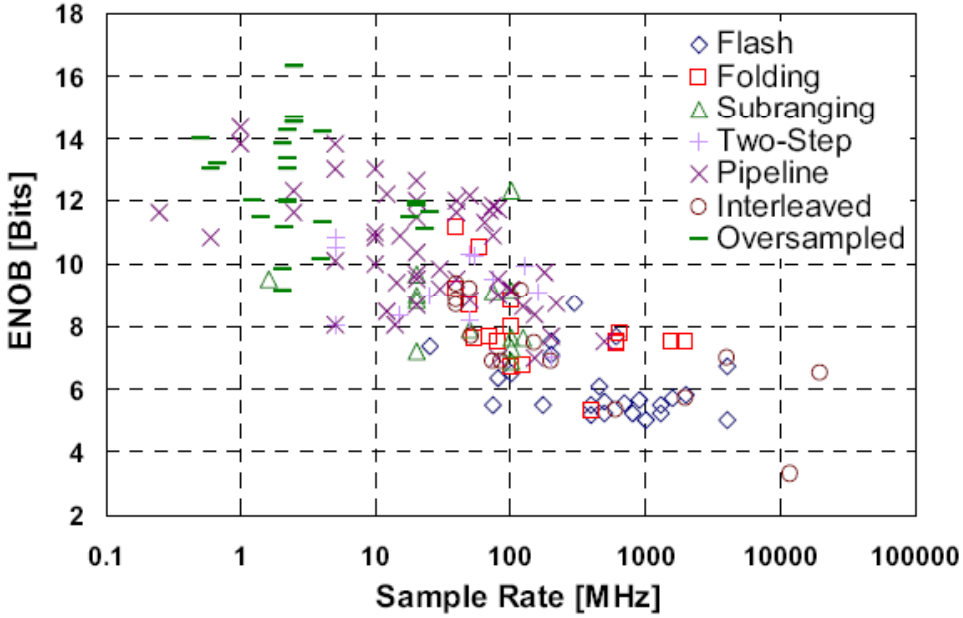


Fig. 2. ADC sample rate vs. ENOB from 1987 to 2005.

Which ADC Architecture Is Right for Your Application?

By Walt Kester [walt.kester@analog.com]

IEEE 2005 CUSTOM INTEGRATED CIRCUITS CONFERENCE

Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS

Y. Chiu [1], B. Nikolić [2], and P. R. Gray [2]

[1] Electrical and Computer Engineering, University of Illinois at Urbana-Champaign
[2] Electrical Engineering and Computer Sciences, University of California at Berkeley

ADC operational environment and influence on performance

- Supply voltage (ex. 14 bit requires 600 ppm/V)
- Temperature (ex. 14 bit requires 0.3 ppm / º C)

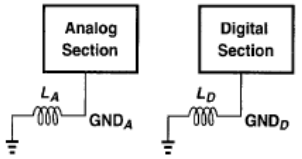


Figure 18.54 Analog and digital grounds.

- High-performance converters use separate pins for A and D supplies
- Connecting leads between supplies and pins should be short (noise, L).
- High frequency measurements need multi-layer PCB boards with separate ground and power planes.
- PCB traces leading clock signals must be short with a solid ground plane underneath.
- For low speed converters use a low output impedance generator so that internal fluctuations < 1 LSB are avoided.
- Manufacturers may provide evaluation boards, or their layout, as well as guidelines explaining evaluation procedures.
- PCB limits can totally mask the performance of a device

Converter specifications (chapter 2 in "Maloberti")

- General features: Many self-explanatory. Type of analog signals, resolution, dynamic range, absolute maximum ratings, ESD notice, pin function and pin configuration, warm-up time, drift.
- Static specifications: analog resolution, analog input range, offset, zero scale offset, common mode error, full scale error, bipolar zero offset, gain error, differential non-linearity error (DNL), monotonicity, hysteresis, missing code, integral non-linearity (INL), temperature range, thermal resistance, lead temperature, power dissipation
- Dynamic specifications: analog input bandwidth, input impedance, load regulation or output impedance, settling time, cross-talk, aperture uncertainty (jitter), D. to A. glitch impulse, glitch power, equivalent input referred noise, SNR, SINAD, SNDR, Dynamic range, Effective number of bits, harmonic distortion, spurious free dynamicrange, intermodulation distortion, two-tone Intermodulation distortion, multi-tone power ratio, noise power ratio, effective resolution bandwidth, Figure of Merit
- Digital and switching specifications:logic levels, encode or clock rate, clock timing, clock source, sleep mode

Static specifications (chapter 2 in “Maloberti”)

- **Static specifications**:
  analog resolution, analog input range, offset, zero scale offset, common mode error, full scale error, bipolar zero offset, gain error, differential non-linearity error (DNL), monotonicity, hysteresis, missing code, integral non-linearity (INL), temperature range, thermal resistance, lead temperature, power dissipation

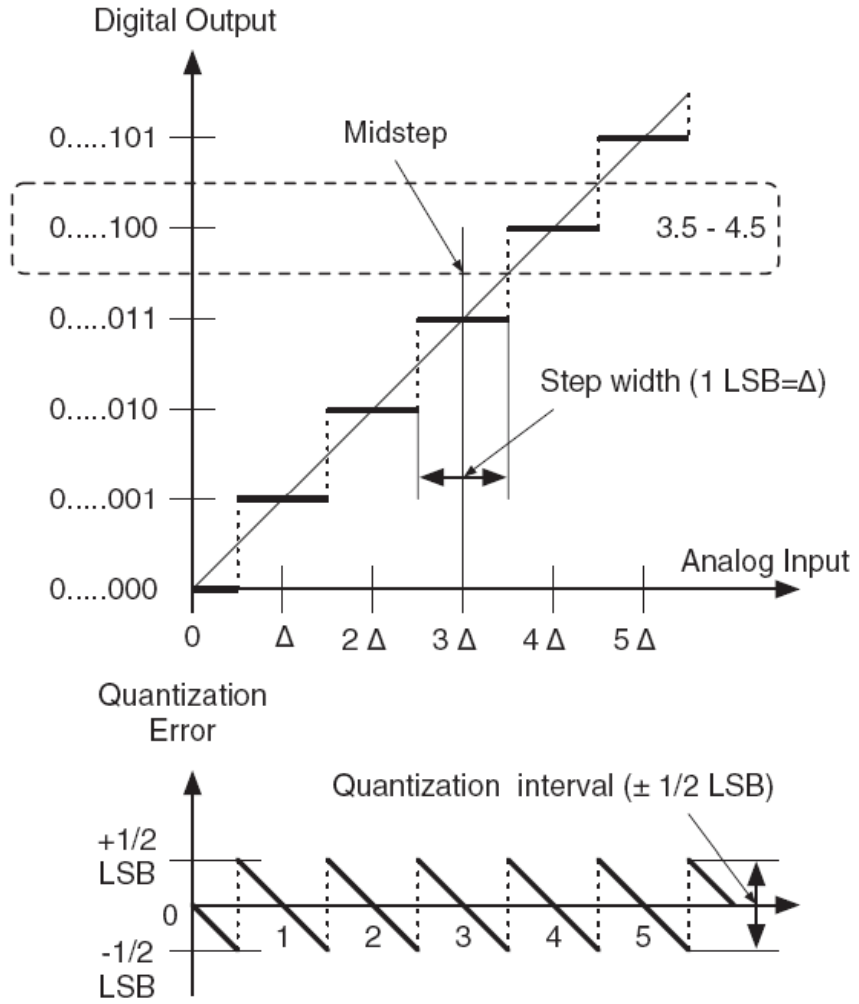


Figure 2.2. Ideal input-output transfer function of an A/D converter.

Static specifications (chapter 2 in “Maloberti”)

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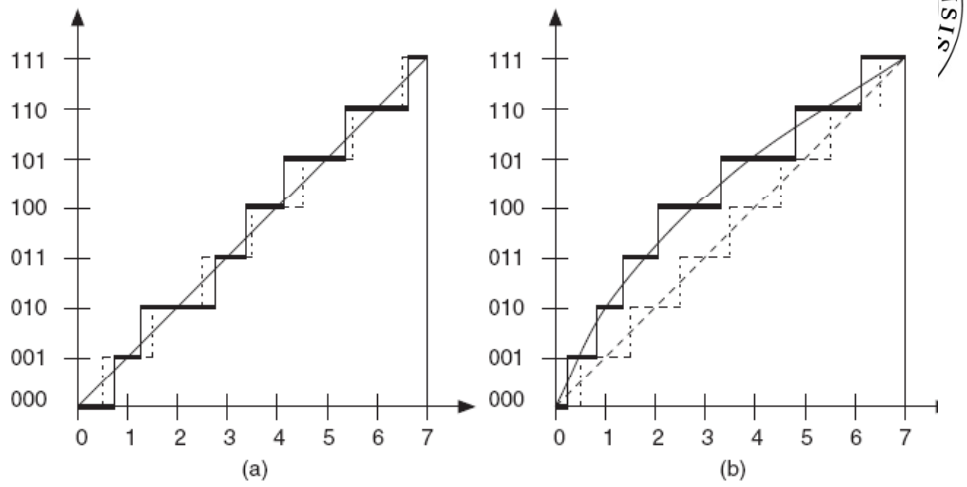

Figure 2.3. Input-output transfer characteristic of a real data converter.

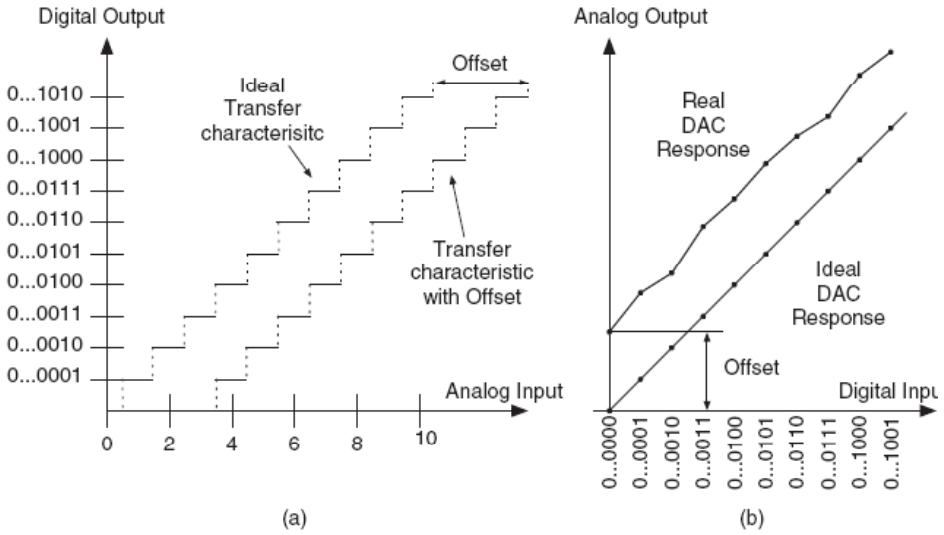

Figure 2.4. Offset error for an analog-to-digital (a) and a digital-to-analog (b) converter.

Static specifications (chapter 2 in “Maloberti”)

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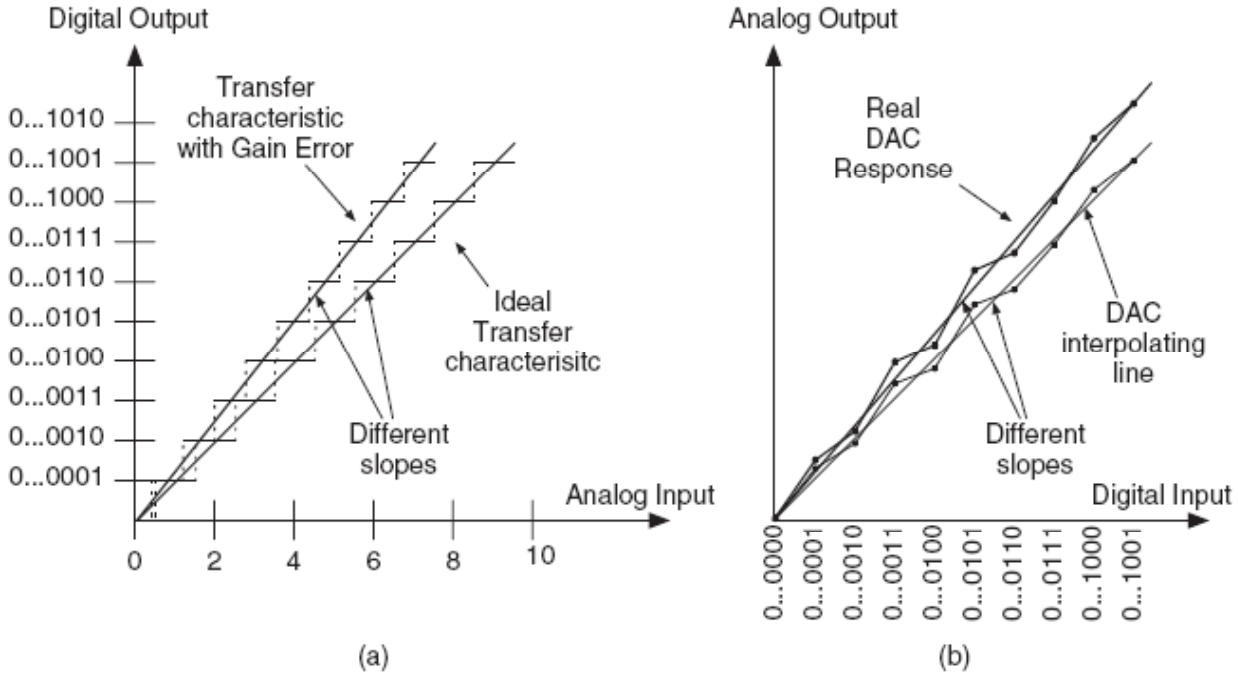

Figure 2.5. Gain error for an analog-to-digital (a) and a digital-to-analog (b) converter.

Static specifications (chapter 2 in “Maloberti”)

- Static specifications:
  analog resolution, analog input range, offset, zero scale offset, common mode error, full scale error, bipolar zero offset, gain error, differential non-linearity error (DNL), monotonicity, hysteresis, missing code, integral non-linearity (INL), temperature range, thermal resistance, lead temperature, power dissipation

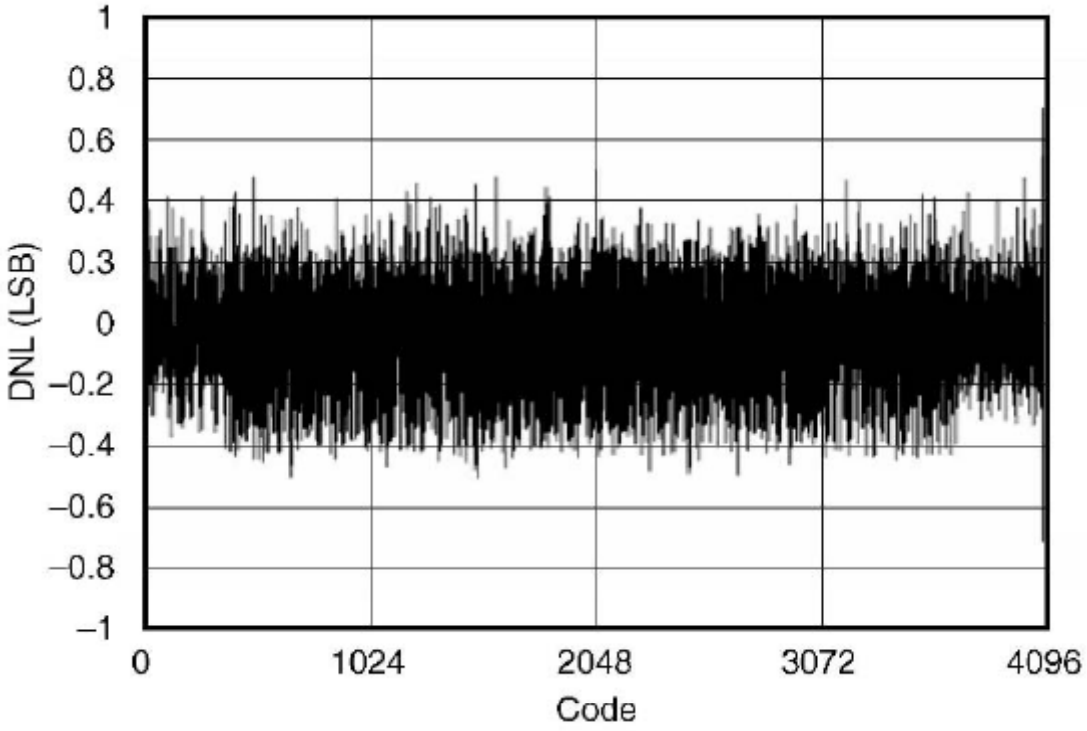

Figure 2.6. Differential non-linearity error (*DNL*) of a possible 12-bit ADC.

$$DNL(k) = \frac{\Delta_r(k) - \Delta}{\Delta}. \qquad (2.1)$$

Data Converter Specifications

ANALOG DEVICES

8-Bit, 250 MSPS, 1.8 V Dual Analog-to-Digital Converter (ADC)

AD9284

FEATURES

- Single 1.8 V supply operation
- SNR: 49.3 dBFS at 200 MHz input at 250 MSPS
- SFDR: 65 dBc at 200 MHz input at 250 MSPS
- Low power: 314 mW at 250 MSPS
- On-chip reference and track-and-hold
- 1.2 V p-p analog input range for each channel
- Differential input with 500 MHz bandwidth
- LVDS-compliant digital output
- DNL: ±0.2 LSB
- Serial port control options
  - Offset binary, Gray code, or twos complement data format
  - Optional clock duty cycle stabilizer
  - Built-in selectable digital test pattern generation
- Pin-programmable power-down function
- Available in 48-lead LFCSP

APPLICATIONS

- Communications
- Diversity radio systems
- I/Q demodulation systems
- Battery-powered instruments
- Handheld scope meters
- Low cost digital oscilloscopes
- OTS: video over fiber

GENERAL DESCRIPTION

The AD9284 is a dual 8-bit, monolithic sampling, analog-to-digital converter (ADC) that supports simultaneous operation and is optimized for low cost, low power, and ease of use. Each ADC operates at up to a 250 MSPS conversion rate with outstanding dynamic performance.

The ADC requires a single 1.8 V supply and an encode clock for full performance operation. No external reference components are required for many applications. The digital outputs are LVDS compatible.

The AD9284 is available in a Pb-free, 48-lead LFCSP that is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Integrated Dual 8-Bit, 250 MSPS ADC.
2. Single 1.8 V Supply Operation with LVDS Outputs.
3. Power-Down Option Controlled via a Pin-Programmable Setting.

FUNCTIONAL BLOCK DIAGRAM

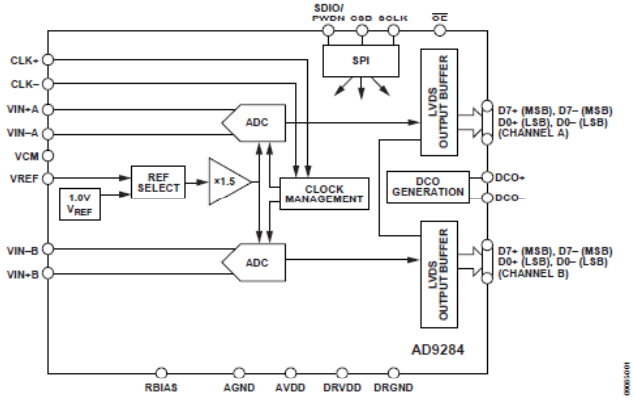

Figure 1.

Rev. 0
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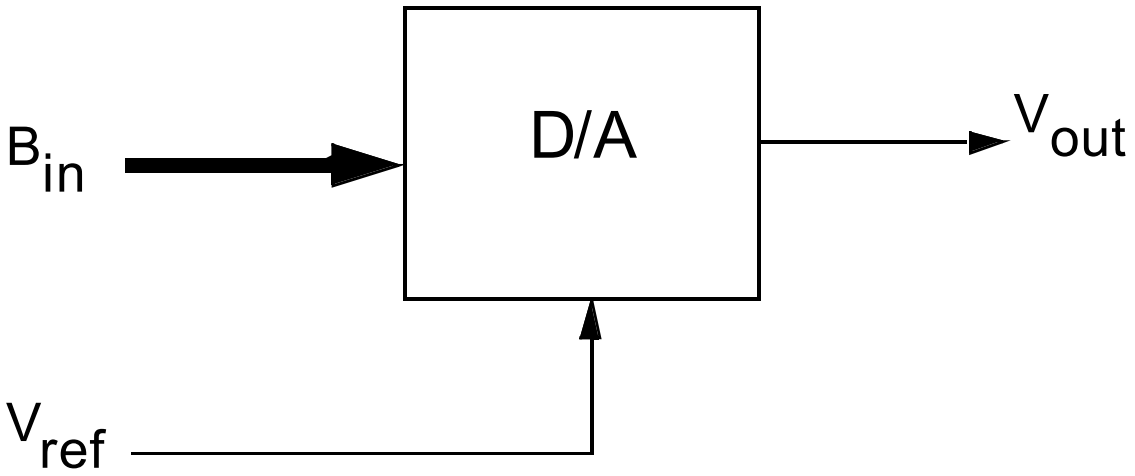
Ideal D/A converter



$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}$$

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N})$$

Example : 8-bit D/A converter

An ideal D/A converter has

$$V_{ref} = 5\ V$$

Find Vout when

$$B_{in} = 10110100$$

$$B_{in} = 2^{-1} + 2^{-3} + 2^{-4} + 2^{-6} = 0{,}703125$$

$$V_{out} = V_{ref} B_{in} = 3{,}516\ V$$

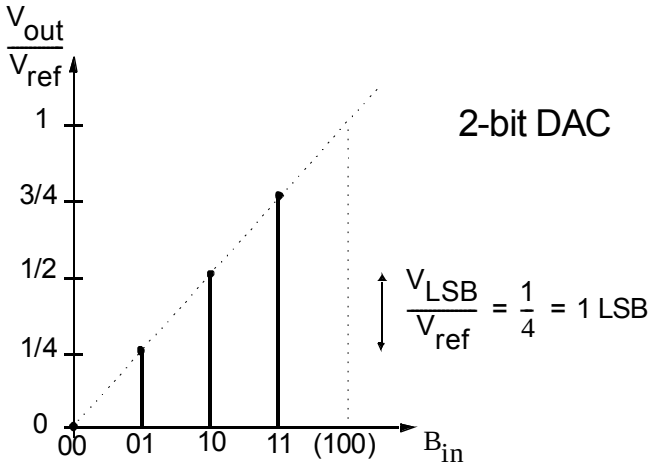
Find

$$V_{LSB}$$

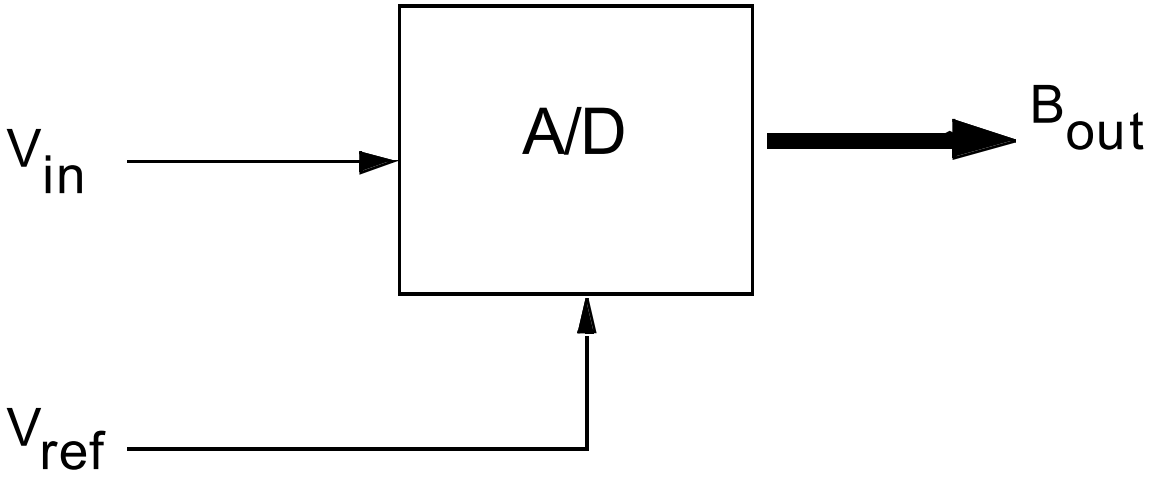
$$V_{LSB} = 5/256 = 19{,}5\ mV$$

$$V_{LSB} \equiv \frac{V_{ref}}{2^N}$$

$$1\ LSB = \frac{1}{2^N}$$



Ideal A/D converter (Fig. 11.3)

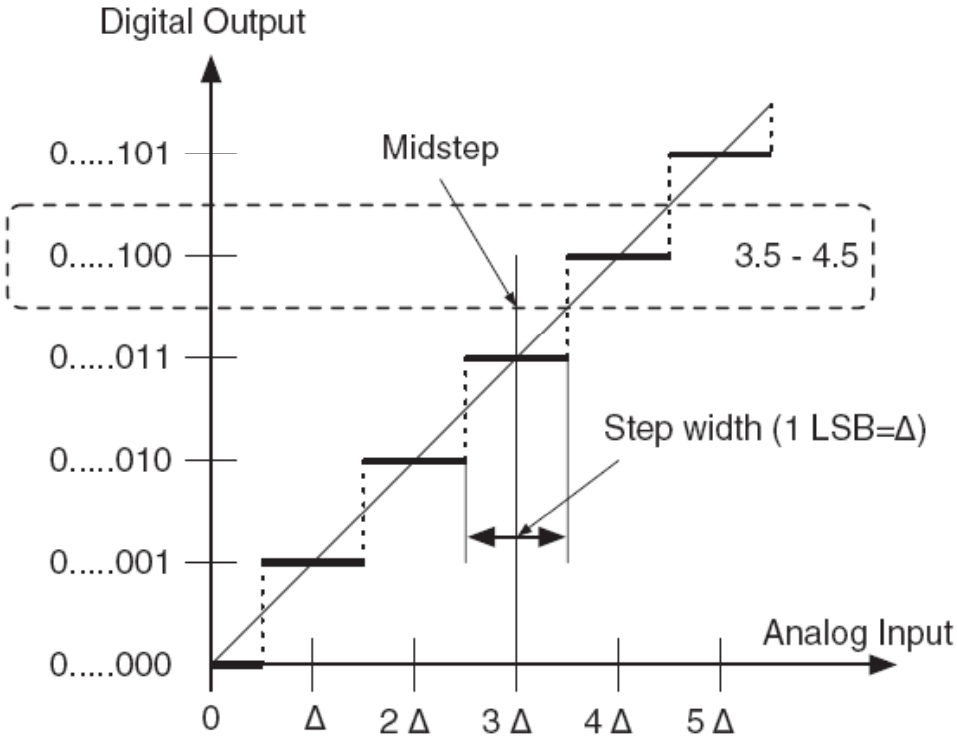


$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) = V_{in} \pm V_x$$

where

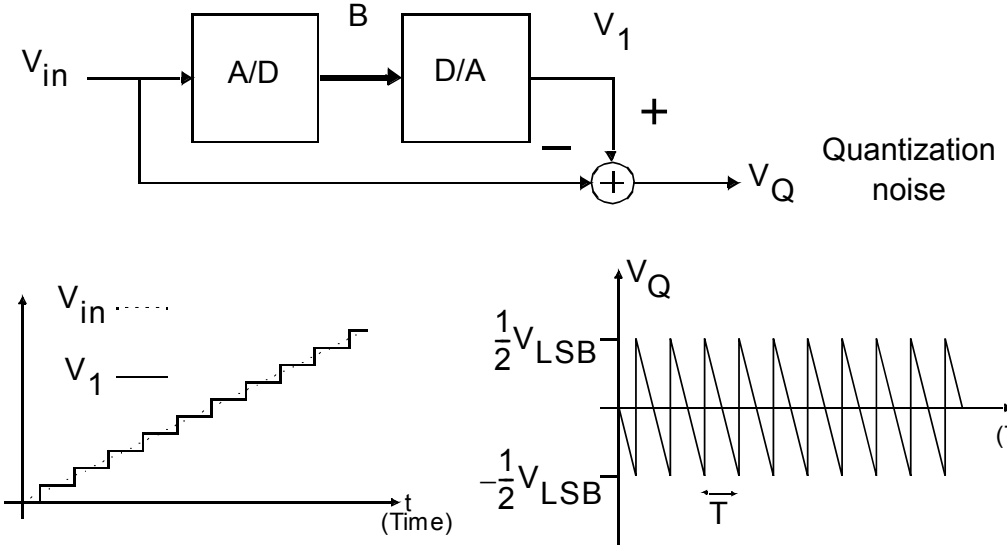
$$-\frac{1}{2}V_{LSB} \leq V_x < \frac{1}{2}V_{LSB}$$

Ideal transfer curve for a generic number of bits A/D converter (Fig. 2.2)



- A range of input values produce the same output value (QA range of input values produce the same output value (Quantization error)
- Different from the D/A case

Quantization noise (“J&M” + “M”)



$$V_Q = V_1 - V_{in}$$

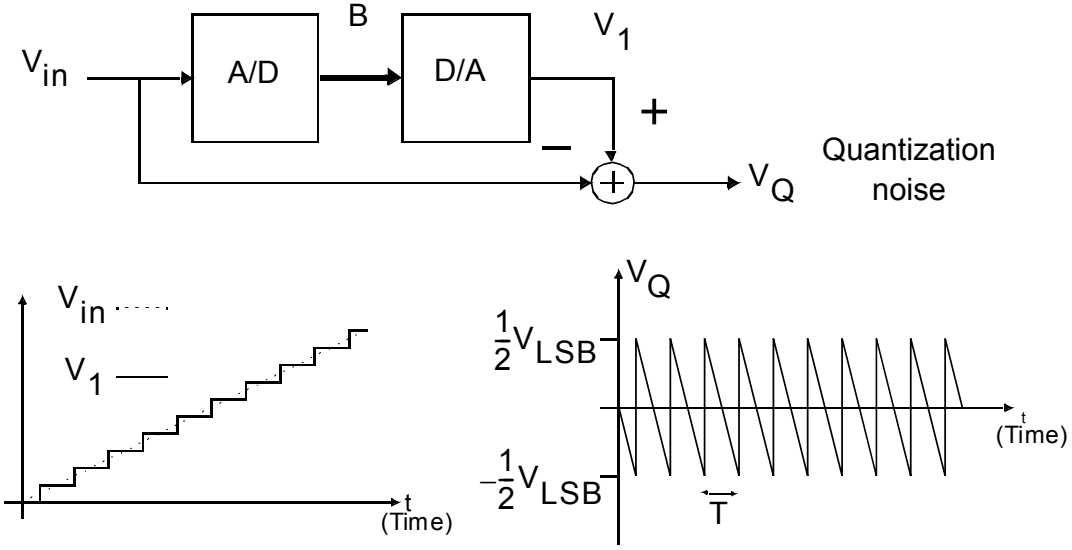
Quantization errors occur even in ideal A/D converters.

These errors may be modelled as equivalent to an additive noise source.

$V_1 = V_{in} + V_Q$

The above equation is exact because no approximations have been made. (The quantization noise modelling becomes aproximate once some assumptions are made about the statistical properties of V_Q.)

Quantization noise (“J&M” + “M”)



$$V_Q = V_1 - V_{in}$$

$V_Q = V_1 – V_{in}$

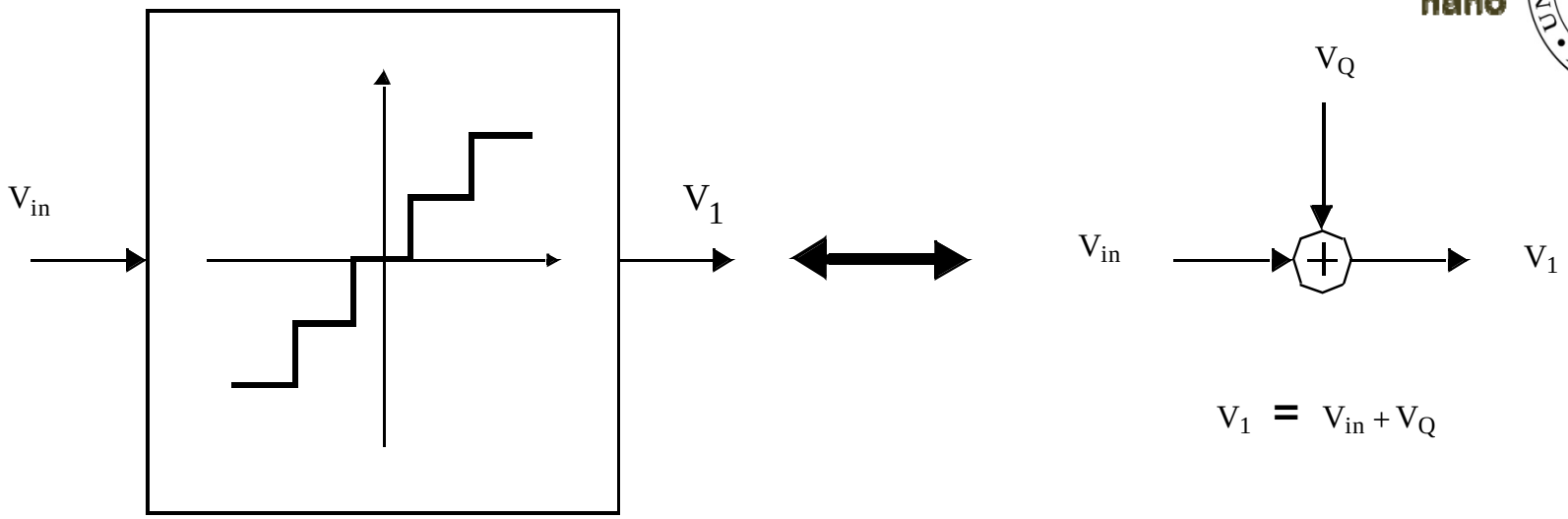
A/D and D/A are both n-bit data converters

The ramp input from the D/A appears as a staircase.

V_Q is limited to +/- $V_{LSB}/2$ The average of V_Q is zero, which is not the case for the rms value of the noise signal.

Rms value for noise voltage:
$V_{n(rms)} = [(1/T)\int^T_0 v^2_n(t)dt]^{1/2}$
, where T is a suitable averaging time interval (4.1) in ”J & M”

Quantization noise model



Quantizer

Model

•TThe model is exact as long as Vq is properly defined

•Vq is most often assumed to be white and uniformely distributed between +/- Vlsb/2

Quantiztion noise

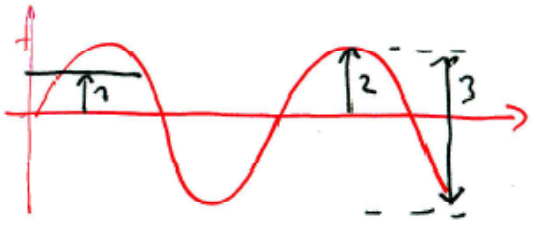
$$SNR = 20 \log\left(\frac{V_{in(rms)}}{V_{q(rms)}}\right)$$

$$= 20 \log\left(\frac{V_{ref}/2\sqrt{2}}{V_{LSB}/\sqrt{12}}\right)$$

, assuming V_{in} is a sinusoidal waveform between 0 and V_{ref}

$$\wedge \; V_{ref} = V_{LSB} \cdot 2^N$$

$$SNR = 2\log\left\{\frac{\frac{V_{ref}}{2\sqrt{2}}}{\frac{V_{ref}/2^N}{\sqrt{12}}}\right\} = 2\log\left\{\frac{\frac{V_{ref}}{\sqrt{2}\sqrt{2}}}{\frac{V_{ref}/2^N}{\sqrt{2}\sqrt{2}\sqrt{3}}}\right\} = 2\log\left\{\frac{\frac{1}{\sqrt{2}}}{\frac{1/2^N}{\sqrt{3}}}\right\} = 2\log\left\{\frac{\frac{1}{\sqrt{2}} \cdot \sqrt{2}\sqrt{3}}{\frac{1/2^N}{\sqrt{3}} \cdot \sqrt{2}\sqrt{3}}\right\}$$



$$= 20 \log \frac{\sqrt{3}}{\sqrt{2}} + 20 \log 2^N$$

$$\log(a-b) = \log a + \log b$$

$$\log_b (c^p) = p \log_b c$$

$$1.76 \text{ dB} + 6.02N$$

$$SNR = 6.02N + 1.76 \; [\text{dB}]$$

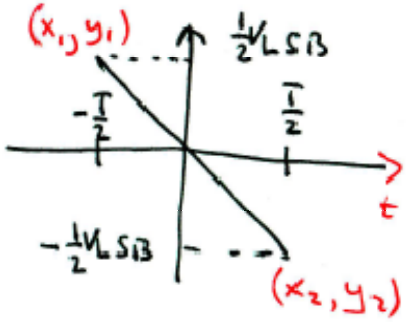
1) rms amplitude
2) peak amplitude
3) peak-to-peak ampl.

$$\text{Peak-to-peak} = 2\sqrt{2} \times \text{RMS}$$

$$\text{RMS} = \frac{\text{peak-to-peak}}{2\sqrt{2}}$$

Quantiztion noise

$$V_{n(rms)} = \sqrt{\frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} V_Q \, dt}$$



$$(y - y_1) = \frac{y_2 - y_1}{x_2 - x_1}(x - x_1)$$

$$y - \tfrac{1}{2}V_{LSB} = \frac{-\frac{1}{2}V_{LSB} - \left(+\frac{1}{2}V_{LSB}\right)}{\frac{T}{2} - \left(-\frac{T}{2}\right)}\left(t + \frac{T}{2}\right)$$

$$y - \tfrac{1}{2}V_{LSB} = \frac{-V_{LSB}}{T}\left(t + \frac{T}{2}\right)$$

$$y - \tfrac{1}{2}V_{LSB} = -\frac{V_{LSB}}{T}t - \frac{V_{LSB}\cdot T}{T2}$$

$$y = -\frac{V_{LSB}}{T}\cdot t$$

$$V_Q = -\frac{LSB}{T}\cdot t$$

$$V_{Q(rms)} = \sqrt{\frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} V_{LSB}^2\left(-\frac{t}{T}\right)^2 dt}$$

$$= \sqrt{\frac{V_{LSB}^2}{T^3}\left(\frac{t^3}{3}\Big|_{-\frac{T}{2}}^{\frac{T}{2}}\right)}$$

$$= \sqrt{\frac{V_{LSB}^2}{T^3}\left[\frac{\left(\frac{T}{2}\right)^3}{3} - \frac{\left(-\frac{T}{2}\right)^3}{3}\right]} = \sqrt{\frac{V_{LSB}^2}{T^3}\left(\frac{\frac{T^3}{8}}{3} + \frac{\frac{T^3}{8}}{3}\right)} = \sqrt{\frac{V_{LSB}^2}{T^3}\,\frac{\frac{2T^3}{8}}{3}\cdot 24} = \sqrt{\frac{V_{LSB}^2}{72}}$$

$$= V_{LSB}/\sqrt{12}$$

$$V_{Q\,rms} = \frac{V_{LSB}}{\sqrt{12}}$$

Quantization noise

- The rms-value of the quantization noise can be shown to be:

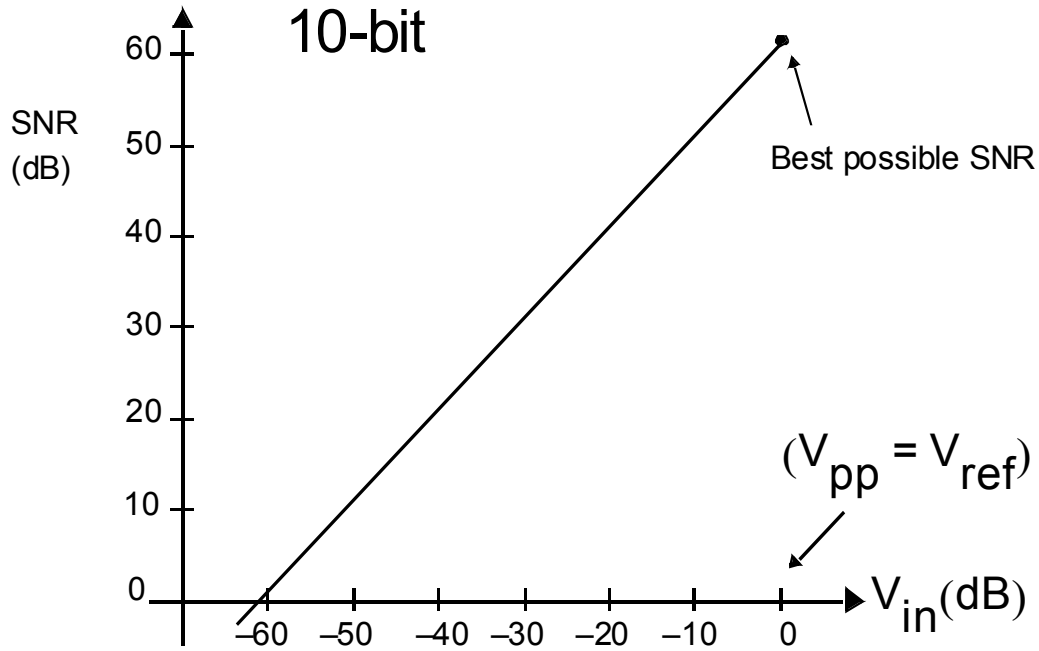
$$V_{Q(rms)} = \frac{V_{LSB}}{\sqrt{12}}$$

- Total noise power is independent of sampling frequency
- In the case of a sinusoidal input signal with p-p amplitude of $V_{ref}/2$

$$SNR = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/(2\sqrt{2})}{V_{LSB}/(\sqrt{12})}\right)$$

$$SNR = 6{,}02N + 1{,}76\ \text{dB}$$

Quantization noise



•Signal-to Noise ratio is highest for maximum input signal amplitude

Signed codes

Table 11.1 Some 4-bit signed digital representations

Number	Normalized number	Sign magnitude	1's complement	Offset binary	2's complement
+7	+7/8	0111	0111	1111	0111
+6	+6/8	0110	0110	1110	0110
+5	+5/8	0101	0101	1101	0101
+4	+4/8	0100	0100	1100	0100
+3	+3/8	0011	0011	1011	0011
+2	+2/8	0010	0010	1010	0010
+1	+1/8	0001	0001	1001	0001
+0	+0	0000	0000	1000	0000
(–0)	(–0)	(1000)	(1111)		
–1	–1/8	1001	1110	0111	1111
–2	–2/8	1010	1101	0110	1110
–3	–3/8	1011	1100	0101	1101
–4	–4/8	1100	1011	0100	1100
–5	–5/8	1101	1010	0011	1011
–6	–6/8	1110	1001	0010	1010
–7	–7/8	1111	1000	0001	1001
–8	–8/8			0000	1000

- Unipolar / bipolar
- Common signed digital repr.: sign magnitude, 1's complement, 2's compl.
- Sign. M.: 5:0101, -5:1101, two repr. Of 0, 2^N-1 numb.
- 1's compl.: Neg. Numbers are complement of all bits for equiv. Pos. Number: 5:0101, -5:1010
- Offset bin: 0000 to the most neg., and then counting up..

  +: closely related to unipolar through simple offset

2's complement

A3a2a1a0	Sign magnitude	2s complement
0111	+7	+7
0110	+6	+6
0101	+5	+5
0100	+4	+4
0011	+3	+3
0010	+2	+2
0001	+1	+1
0000	+0	+0
1000	-0	-8
1001	-1	-7
1010	-2	-6
1011	-3	-5
1100	-4	-4
1101	-5	-3
1110	-6	-2
1111	-7	-1

- 5_{10} : 0101 = $2^2 + 2^0$
- -5_{10} : (0101)' +1 = 1010 + 1 = 1011

- Addition of positive and negative numbers is straightforward, using addition, and requires little hardware
- 2's complement is most popular representation for signed numbers when arithmetic operations have to be performed

7_{10}-6_{10} via addition using two's complement of -6

- 0000 0000 0000 0000 0000 0000 0000 0000 $00111_2 = 7_{10}$
- 0000 0000 0000 0000 0000 0000 0000 0000 $00110_2 = 6_{10}$
- *Subtraction uses addition: The appropriate operand is negated before being added*
- *Negating a two's complement number: Simply invert every 0 and 1 and add one to the result.* Example:
- 0000 0000 0000 0000 0000 0000 0000 0110_2 becomes
- 1111 1111 1111 1111 1111 1111 1111 1001_2

\+ 1_2

= 1111 1111 1111 1111 1111 1111 1111 1010_2

0000 0000 0000 0000 0000 0000 0000 $0111_2 = 7_{10}$

\+ 1111 1111 1111 1111 1111 1111 1111 $1010_2 = -6_{10}$

= 0000 0000 0000 0000 0000 0000 0000 $0001_2 = 1_{10}$

performance limitations

- Resolution
- Offset and gain error
- Accuracy
- Integral nonlinearity (INL) error
- Differential nonlinearity (DNL) error
- Monotonicity
- Missing codes
- A/D conversion time and sampling rate
- D/A settling time and sampling rate
- Sampling time uncertainty
- Dynamic range
- NB!! Different meanings and definitions of performance parameters sometimes exist. → Be sure what's meant in a particular specification or scientific paper.. There are also more than those mentioned here.

Resolution

- Resolution usually refers to the number of bits in the input (D/A) or output (ADC) word, and is often different from the accuracy.
- Analog-Digital Conversion Handbook, Analog Devices, 3rd Edition, 1986: *An n-bit binary converter should be able to provide 2n distinct and different analog output values corresponding to the set of n binary words. A converter that satisfies this criterion is said to have a resolution of n bits.*

A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS

Terje Nortvedt Andersen, Bjørnar Hernes, *Member, IEEE*, Atle Briskemyr, Frode Telstø, Johnny Bjørnsen, *Member, IEEE*, Thomas E. Bonnerud, and Øystein Moldsvor

TABLE I
KEY DATA FOR THE ADC

Nominal sampling rate	110MS/s
Technology	0.18µm digital CMOS
Nominal supply voltage	1.8V
Resolution	12bit
Full scale analog input	$2V_{P-P}$
Area	$0.86mm^2$
Power consumption	97mW
DNL	±1.2 LSB
INL	-1.5/+1 LSB
SNR (f_{in}=10MHz)	67.1 dB
SNDR (f_{in}=10MHz)	64.2 dB
SFDR (f_{in}=10MHz)	69.4 dB
ENOB (f_{in}=10MHz)	10.4 bit

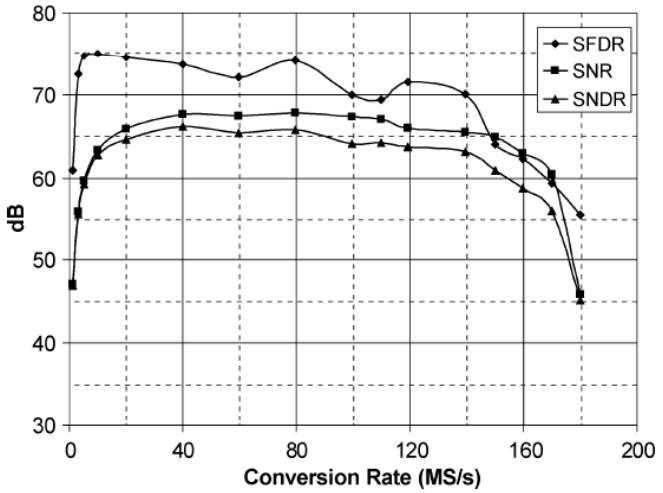


Fig. 8. SFDR, SNR, and SNDR versus conversion rate. The input frequency and signal swing is 10 MHz and $2V_{P-P}$, respectively.

Litterature

- Johns & Martin: ”Analog Integrated Circuit Design”
- Franco Maloberti: ”Data Converters”

Next week, 22/2:

- More on Nyquist Data Converters
- Messages are given on the INF4420 homepage.
- Questions: sa@ifi.uio.no , 22852703 / 90013264