Nyquist Digital to Analog Converters
Tuesday, February 22nd, 9:15 – 11:10

12-Bit, 4.0Gsps Wideband DAC

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February the 15th

- (The contents refer to
- "Maloberti")
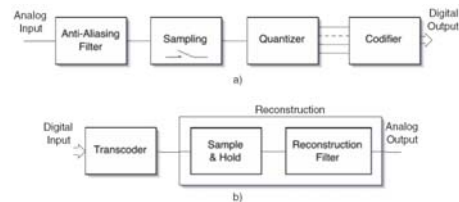
Figure 1.1. Block diagram of the basic functions of an A/D (a) and a D/A (b) converter.

26. februar 2011   2
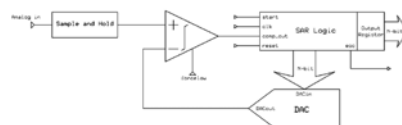
Ideal D/A converter

B_{in} → [D/A] → V_{out}
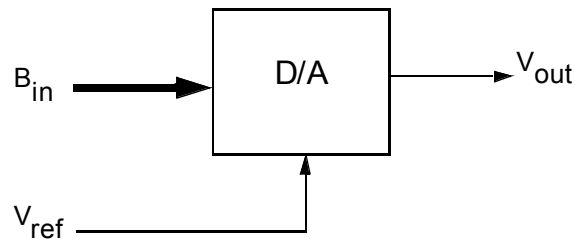
V_{ref} →

$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}$$

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N})$$

February the 22th

- **3.1 Introduction**
- 3.1.1 DAC applications
- 3.1.2 Voltage and current references
- **3.2 Types of converters**
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- 3.3.1 Resistive divider
- 3.3.2 X-Y selection
- 3.3.3 Settling of the output voltage
- 3.3.4 Segmented architectures
- 3.3.5 Effects of mismatch
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- 3.3.8 R-2R Resistor Ladder DAC
- 3.3.9 Deglitching

3.4 Capacitor based architectures
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3.5 Current source based architectures
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3.5.2 Unity current generator
3.5.3 Random mismatch with unary selection
3.5.4. Current sources selection
3.5.5 Current switching and segmentation
3.5.6 Switching of current sources
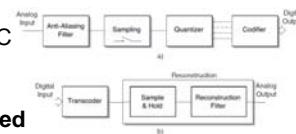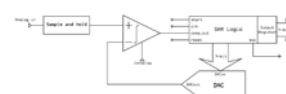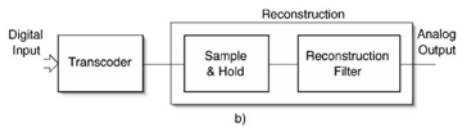**3.6 Other architectures**
(The contents refer to "Maloberti")

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Real reconstruction filters

$$H_{S\&H}(s) = \frac{1 - e^{-sT}}{s\tau}, \qquad (1.39)$$

where τ is a suitable gain factor whose dimension is time for making $H_{S\&H}$ dimensionless.

Equation (1.39) on the $j\omega$ axis becomes

$$H_{S\&H}(j\omega) = j\frac{T}{\tau}e^{-j\omega T/2}\frac{sin(\omega T/2)}{\omega T/2}, \qquad (1.40)$$

showing a phase shift proportional to ω and an amplitude attenuation proportional to the $sinc\ (=sin(x)/x)$ function.
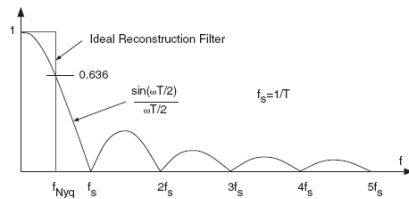
Figure 1.27. Amplitude response of the ideal and real sample-and-hold.

- A real reconstruction filter is an approximation of the ideal reconstruction response, given by eq. 1.39.
- Many commercial DACs provide output in sampled data form (no reconstruction) A reconstruction filter removes frequencies higher than the Nyquist limit. (Still harmonics of low frequency signals and the intermodulation products coming from multi-tone inputs produce spurs inside the first Nyquist zone.)
- Other DACs have an output providing a continous time signal with a BW within the first Nyquist zone.
- For example, both the input and the output for audio equipment is sampled at 44.1 kHz. Both audio filters block as much as possible above 22 kHz and pass as much as possible below 20 kHz. Typically both filters are active op-amp filters, with exactly the same selection of resistors and capacitors.

Matching of passive components (R, C) within 0.1 to 0.02 % possible
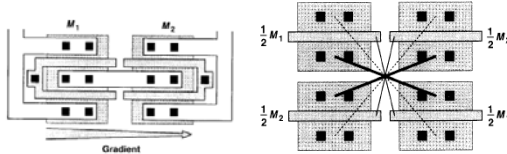
- Gain or attenuation of references
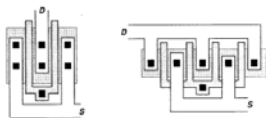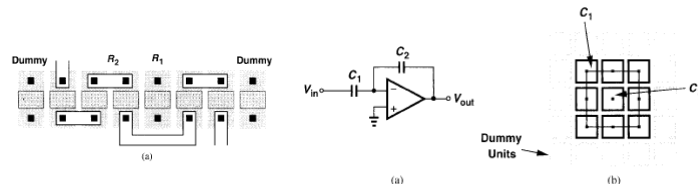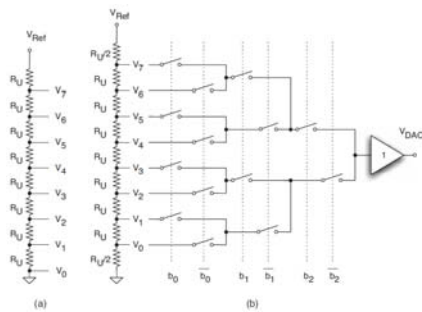- Careful layout (inter digitized , common centroid, dummy elements, equalization of resistive metal contacts) leads to matching accuracies within 0.02 % to 0.1 % without trimming or digital correction (60 dB to 70 dB resolution)

3

DACs, CMOS switches and OTAs

- A MOS transistor becomes an off-switch if its driving voltage is in the subthreshold region, and low resistance (on-switch) if its driving voltage well exceeds the threshold and V_{DS} is small.
- Design of switches and their control is an important part of the data converter design because it is important to obtain low on-resistance, high speed of switching and minimum side effects (clock feedthrough, charge injection).
- OTA performance crucial for meeting DAC specifications

(A few) applications (ch. 3.1.1)
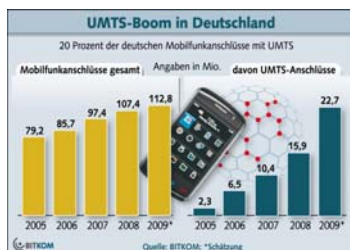
- High speed DACs for video signals from a computer or a DVD.
- HDTV: (plasma) requires above 11 bits. 12-bits and 150 MSPS often required
- UMTS, CDMA2000, GSM/EDGE; 200 MSPS 12 – 16 bit can be necessary.
- DACs may replace potentiometers in analogue signal processors.
- Audio; 16-bit (or more), 44 kSpS

Voltage and current references (ch. 3.1.2)
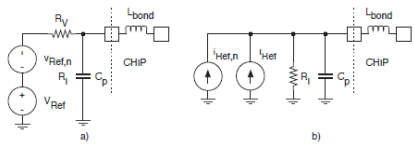
Figure 3.2. Equivalent model of external references: (a) voltage and (b) current.

Remember

The noise of reference generators must be lower than the expected quantization noise floor. The request becomes very challenging for resolutions above 14-bit.

- The dynamic range is established by the voltage (or current) reference which can be generated inside the chip or via an external pin.
- High accuracy is needed as errors affect the overall performance.
- Constant, independent of load changes, temperature, supply voltage, time
- Static errors may lead to gain errors.
- Dynamic errors are worse, and may affect SNR and speed.

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3 main types of converters

$$V_{Out} = V_{Ref} \frac{C_1}{C_1 + C_2}. \qquad (3.18)$$

- Resistor based architectures
- Capacitor based architectures
- Current source based architectures

Resistor based architectures (ch. 3.3)

- **Resistive divider.**
- **The digital potentiometer**
- **R-2R resistive ladder**
- $\Omega/\square$ - $k\Omega/\square$
- Matching errors cause gain errors and sometimes harmonic distortion
- When ratio between resistors is an integer number, use unity elements to construct the various elements by series connections.
- Dummy structures for improved matching

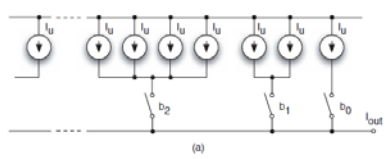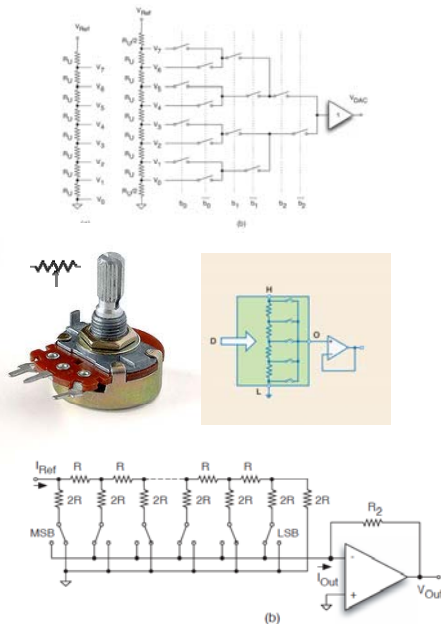$$R = \rho_\square (L/W)_{eff} + 2 \cdot R_{cont}.$$

Resistor divider (ch. 3.3.1)

- A resistive string connected accross the positive and negative reference obtain multiple voltages whose digitally controlled selection realizes a very simple DAC.
- Fig. 3.4 a); 3-bit divider made of 2^3 equal resistors.
- The selected voltage (simples method shown in Fig. 3 b))is used as the input of a buffer (high input impedance, low output impedance)
- Switch on resistances and the parasitic capacitances can impede the fast operation of a DAC.
- Fig. 3.5 : typical architecture. Power on reset for zero outputvoltage at power-on. Serial interface may be used for input data.

Figure 3.3. (a) resistance with L/W=6. (b) Two matched resistances with ratio 2.

Figure 3.5. Typical architecture of a resistive divider DAC.
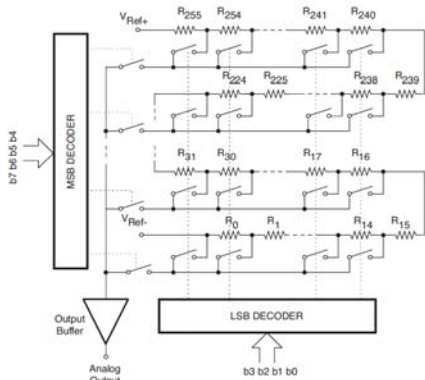
X-Y Selection (ch. 3.3.2)

Figure 3.6. Resistive DAC with X-Y addressing scheme.

- Fig. 3.6: 256 unity resistances divided into 16 lines.
- Avoids the excessive growth of switches with number of bits as the resistive divider architecture (needing 510 switches and 256 logic signals driving the switches for an 8-bit DAC).
- Decoding signals are $2 \cdot 2^{n/2}$ instead of 2^n.
- (8 bit: 32 instead of 256.)
- The layout is compact and minimizes the grading error
- The time constant of the RC network between resistive divider and buffer is doubled (2 switches instead of one).

Settling of the output voltage (ch. 3.3.3)
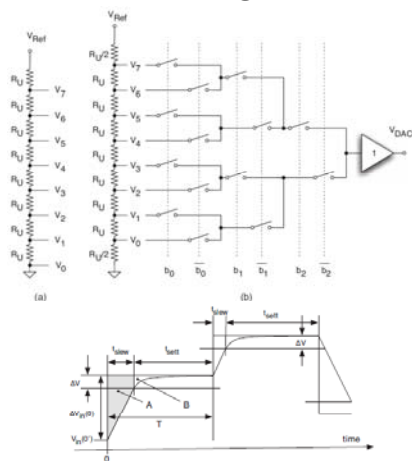
Figure 3.8. Response of a unity gain buffer with finite slew-rate and bandwidth.

Observation
A code dependent settling of the output voltage causes distortion. High *SFDR* requires low resistances at every node. The variation of the settling time must be much smaller than the hold period.

- The RC network and the buffer determine the time from a change in input code to the step change on the output has settled.
- The response is fastest if the beginning or end of the resistive string are selected and slower in the middle range.
- A reconstruction filter filter out spurs at frequencies higher than the Nyquist limit.
- Harmonics of low frequency signals and intermodulation products produce spurs inside the first Nyquist zone. Thus, a spur free output spectrum requires a settling time well below the D/A conversion period (→ low unity resistance).
- The buffer must also be fast enough (limited by SR and gain bandwidth product).

Segmented architectures (ch. 3.3.4)

Figure 3.10. (a) Cascade of two DAC's with decoupling buffers. (b) Volt-metric interconnection of the LSB DAC.

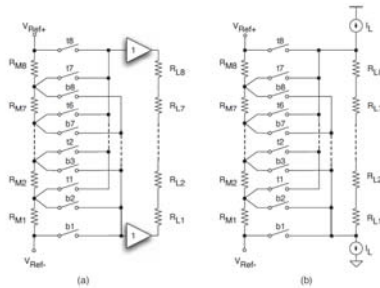- Obtains a higher resolution by combining the operation of two or more DACs together.
- **Fig. 3.10 a)**: R_{M1}-R_{M8} obtain a 3 bit coarse division, and R_{Li1} – R_{Li8}, i=1…8.
- Switches select one of the coarse intervals.
- The offset of the buffers must match below one LSB.
- The input impedance of the input buffer needs to be high and the output reistance must be much less than the total resistance of the LSB divider.
- **Fig. 3.10 b):** Two current generators inject and drain the same current (setting the current in the connections between the two DACs to zero.)

Effect of the mismatch (ch. 3.3.5)

$$R_i = R_u(1 + \epsilon_a) \cdot (1 + \epsilon_{r,i}), \qquad (3.9)$$

The k-th resistor is

$$R_k = R_0(1 + k \cdot \alpha \Delta X); \quad k = 0, \cdots, 2^n - 1 \qquad (3.12)$$

and the output at the tap k becomes

$$V_{out}(k) = V_{Ref} \frac{k + \alpha \Delta X \cdot k(k+1)/2}{2^n - 1 + \alpha \Delta X \cdot (2^n - 1)2^n/2} \qquad (3.13)$$

which is parabolic with initial value 0 and final value V_{Ref}. Recall that the INL is $V_{out}(k) - \bar{V}_{out}(k)$. It is plotted in Fig. 3.11 for an 8-bit DAC with $\alpha \Delta X = \pm 10^{-4}$ (curves (a) and (b)). Notice that the maximum value of the INL
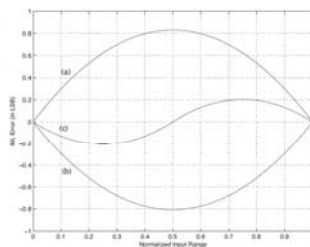
Figure 3.11. INL caused by a gradient in the specific resistance for a linear and a folded (curve (c) resistive string.

- Global error and local fluctuations of parameters
- The error depends on accumulation of mismatches and is zero at the two ends of the string.
- Problematic when errors are correlated and accumulate to a large INL.
- Fig.3.11: 8-bit DAC with $\alpha \Delta X$ = +/-10^{-4}
- (ΔX is the spacing between unity elements.) (curves a) and b)) Max INL±0.8 LSB.
- Fig. 3.11 c) has a resistive divider folded around it's midpoint, where the INL becomes zero. The max INL is reduced to ¼.
- Better results are obtained with multiple folding and suitably designed layouts.

Trimming and calibration (ch. 3.3.6)
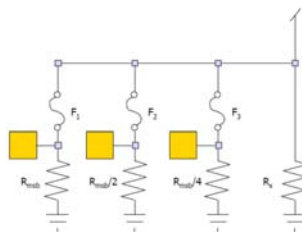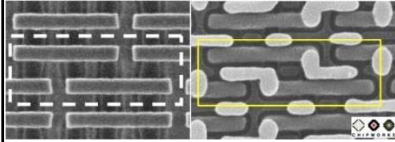
- Systematic variations (described in the 1st order by a gradient) and random errors in resistor values. (Picture left from http://scsong.wordpress.com/2009/10/13/intels-32-nm-clarkdale-shows-many-changes/)
- Monte Carlo simulations to see variance.
- Local fluctuations are unpredictible and cannot be (fully) compensated for with layout strategies.
- Effects of systematic errors cannot be completely cancelled, so that the global accuracy can end up being inadequate for the application at hand.
- Possible solution: Trimming (laser adjustment) or electronic calibration of (thin film) resistors.
- Or fuses and anti-fuses. (Fig. From www.eng.yale.edu/elab/eeng427/lectures/EENG427l06alayout.pdf)

R-2R Resistor Ladder DAC (ch. 3.3.8)
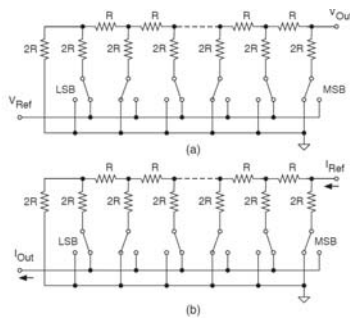
(a) Voltage mode R-2R ladder network. (b) R-2R current mode ladder networks.

- Reduces the number of resistors from 2^n to 3n.
- Ex. 8 bit: 24 resistors instead of 256
- Combines a set of signals that are related in a binary weighted fashion
- The output variable could be a voltage or a current.
- Output from R-2R in the voltage mode:

$$V_{Out} = \frac{V_{Ref}}{2} b_{n-1} + \frac{V_{Ref}}{4} b_{n-2} + \cdots + \frac{V_{Ref}}{2^{n-1}} b_1 + \frac{V_{Ref}}{2^n} b_0, \quad (3.14)$$

which is the DAC conversion of a digital input $\{b_{n-1}, b_{n-2}, \cdots, b_1, b_0\}$.

- The "Kelvin divider" is intrinsically monotonic – not the R-2R.

R-2R Resistor Ladder DAC

$R-2R$ - based structure

$V_3 = \dfrac{V_2}{2}$

$U = RI$
$I = \dfrac{v}{R}$

$I_3 = \dfrac{\frac{V_2}{2}}{2R'} = \dfrac{\frac{1}{2}\cdot\frac{1}{2}\cdot V_{ref}}{2R} = \dfrac{V_{ref}}{8R}$

and so on..

Resistors of size $2R$ are made from size R resistors to improve matching.

$R_4' = 2R$

$R_4 = \dfrac{2R\cdot 2R}{2R+2R} = \dfrac{4R^2}{4R} = R$

$R_3' = R + R_4 = R + R = 2R$

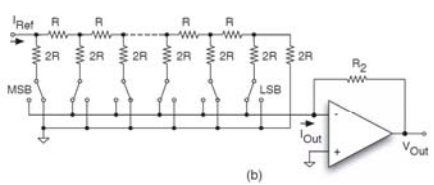$R_3 = 2R \| R_3' = \dfrac{2R\cdot 2R}{4R} = R$

$R_2' = R + R_3 = R + R = 2R$

$R_2 = 2R \| R_2' = R$

$R_1' = R + R_2 = R + R = 2R$

$R_1 = 2R \| R_1' = R$

$R_i' = 2R$ for all i

Therefore:

$I_1 = \dfrac{V_{ref}}{2R}$

From ②:

The voltage at node ② is half of the voltage at ①:

$I_2 = \dfrac{V_2}{2R} = \dfrac{\frac{1}{2}V_{ref}}{2R} = \dfrac{V_{ref}}{4}$
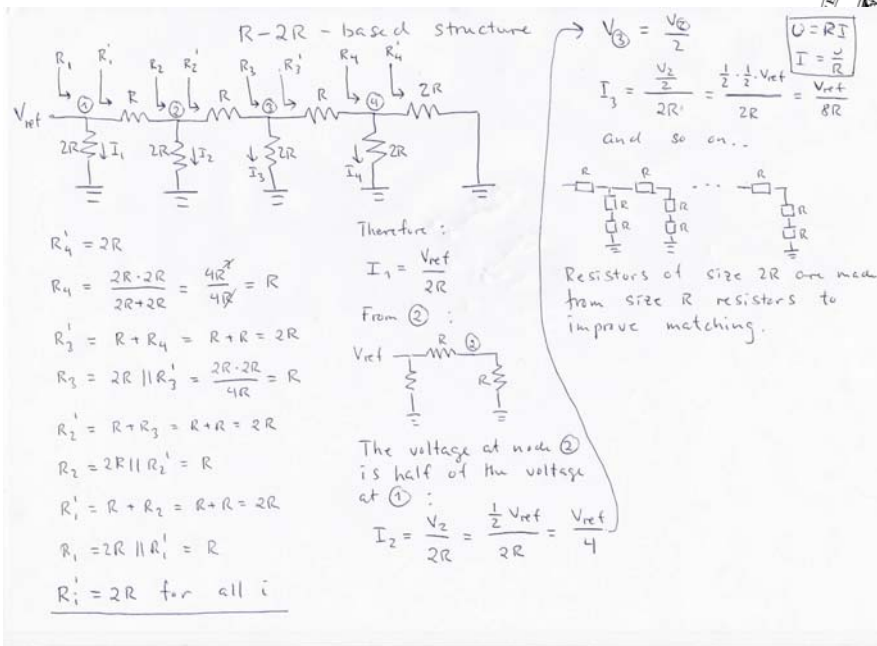
Current-mode R-2R (ch. 3.3.8)

$I_{Out} = \dfrac{I_{Ref}}{2}b_{n-1} + \dfrac{I_{Ref}}{4}b_{n-2} + \cdots + \dfrac{I_{Ref}}{2^{n-1}}b_1 + \dfrac{I_{Ref}}{2^n}b_0 \qquad (3.15)$
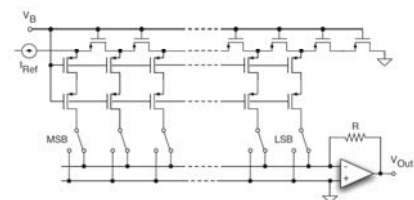
- The current-mode R-2R ladder network is converted to a voltage with an operational amplifier.
- Only two resistance values → good matching
- Impedance at virtual ground is code dependent → code dependent amplification of the op-amp offset and its low frequency noise.
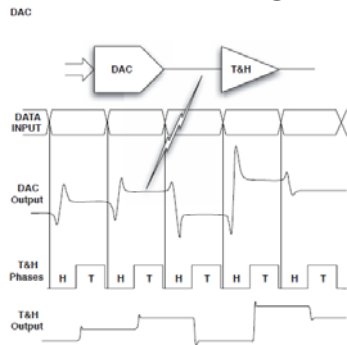- For medium accuracy the resistors may be replaced by MOS transistors, saving area.

Figure 3.21. R-2R architecture with MOS transistors replacing the resistors.

Deglitching (ch. 3.3.9)

Figure 3.25.   Deglitch circuit and possible voltages.

decimal	Binary b1b2b3	Thermometer code d1d2d3d4d5d6d7
0	000	0000000
1	001	0000001
2	010	0000011
3	011	0000111
4	100	0001111
5	101	0011111
6	110	0111111
7	111	1111111

- Ideally a DAC should change from one value to its new one
- Non-synchronous switching in the R-2R network produces glitches that can cause non-linearity, harmonic distortion and wasted energy. (main source of glitches)
- Deglitching may be done by T/H (=S/H) after the DAC.
- Modify some or all of the digital word from binary to thermometer code (most popular)
- Exact matching in time (difficult)
- Reducing the bandwidth by placing C accross Rfeedback.

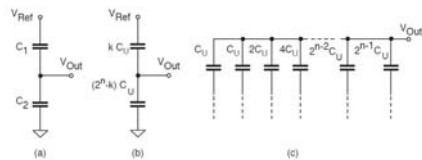# Capacitor based architectures (ch. 3.4)

Figure 3.26. (a) and (b) Simple capacitor divider. (c) Array of binary weighted capacitors.

$$V_{Out} = V_{Ref}\frac{C_1}{C_1 + C_2}. \qquad (3.18)$$

Figure 3.27. (a) MIM capacitance. (b) MMCC capacitance using three metal levels.

- The series of two capacitors, initially discharged between V_{ref} and ground yields V_{Out} given by eq. 3.18.
- The capacitors used are multiples of a unity element.
- Capacitors made from poly-oxide-poly or Metal-Insulator-Metal, MIM.
- Fingers of metal and vias; MMCC

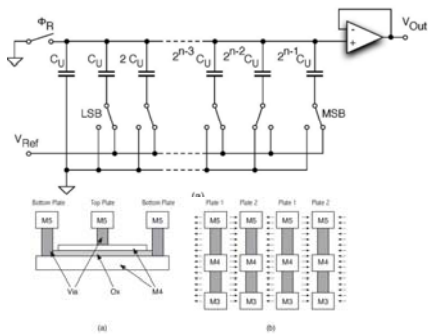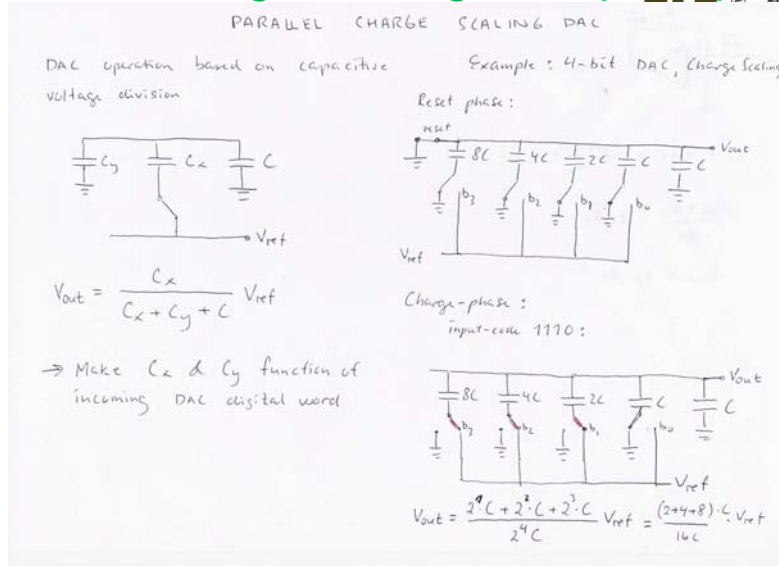# Parallel charge sharing DAC principle

Hybrid Capacitive-Resistive DACs (ch. 3.4.4)
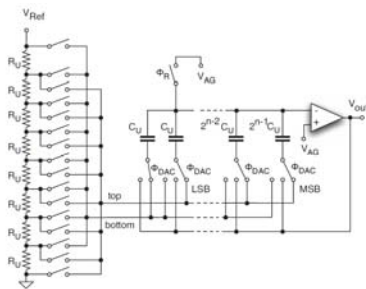
Figure 3.31. Hybrid architecture made by a Kelvin divider followed by a flip-around MDAC.

- Resistive and Capacitive DACs may be combined to give hybrid solutions.
- Resistive DAC for coarse conversion and capacitive DAC for the fine conversion.

Keep in Mind

Any capacitor-based architecture requires a reset phase to make sure that the array is initially discharged. Since the output voltage is not valid during the reset, a track and hold sustains the output.
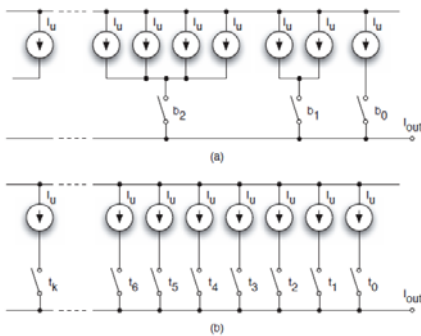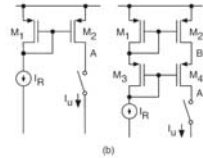
Current source based architectures (ch. 3.5)

Figure 3.32. (a) Binary weighted control. (b) Unary weighted control.

An *n-bit* current steering DAC switches *k* out of $2^n - 1$ unity current generators toward the output node under the control of the *n-bit* digital input,

mirror. (b) Simple and cascode MOS current

- Binary weighted current sources
- Output current may be dumped through a resistor
- Simple or cascode current mirrors may be used for unity current sources
- Mismatch in the saturation current, I_D, is a source of error

$$I_D = \beta \left(V_{gs} - V_{th} \right)^2 \qquad (3.29)$$

- $\Delta I/I$ halves if the gate area increases by a factor 4.

Current sources selection (1/2) (ch. 3.5.4)
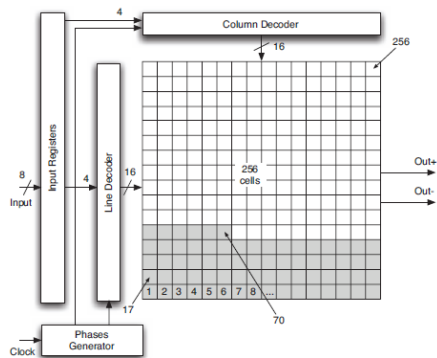

Figure 3.38. 8-bit DAC with thermometric selection of current cells.

- The unity current sources are often arranged in a two-dimensional array whose optimum shape is a square with $2^{n/2}$ lines and columns if the number of bits n is even.
- The simplest thermometric selection is sequential by lines and columns starting from one corner of the array. Fig 3.38 shows the block diag. Of a possible 8-bit DAC with 70 selected cells corresponding to the input code 01000110. A possible grading error in x and y directions causes INL.
- Using a more complex selection technique reduces the INL. …

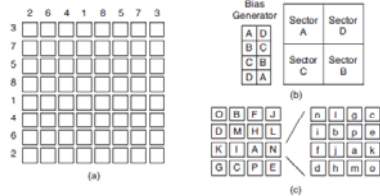# Current sources selection ($2/2$) (ch. 3.5.4)

Figure 3.39. (a) Line and column shuffling. (b) Use of multiple current references for minimizing the threshold mismatch. (c) Random walk selection of unity cells.

- Using a more complex selection technique reduces the INL. …; shuffling lines and columns to randomize the mismatches and keep the accumulated error low (Figure 3.39 a).

- The *Q^2 Random Walk* method has given excellent linearity for 12-bit resolution with a reasonable silicon area.

Thermometer-code Current-Mode D/A-Converter (12.3)

- Thermometer-code decoder in both row and column, for inherent monotonicity and good DNL

- Current is switched to the output when both row and column lines for a cell are high

- Cascode current source used for improved current matching

- Suited for high speed, with output fed directly into a resistor (50 or 75 Ohms), instead of an output opamp.

- The delay to all switches must be equal (suppress glitching)

- Important that the edges of d_i and d_i' are synchronized

- (From "Johns & Martin")
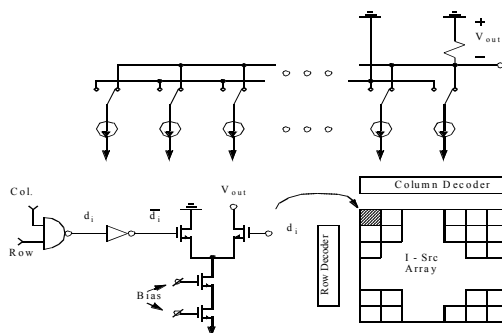
A few published DACs

Publication year	SFDR @Nyquist [dB]	ENOB @ Nyquist	Nyquist update rate, [Ms/s]	Power consumpt. [mW]	Area [mm²]	Supply voltage [V]	Technology [nm]	other	Reference
2009	>60dB	9.7	1000	188			65	Current steering	Lin et al., ISSCC '09
2008	80	12.9	11	119	0.8	1.8	180	"current steering"	Radulov, APPCAS '08
2007	59	9.5	200 @3.3 V	56	2.25	3.3	180	"current steering"	Mercer, JSCC, Aug.'07
2004	40	6	250	23	0.14	1.8	180	"binary weighted"	Deveugele, JSCC, July '04
2001	61	9.84	1000	110	0.35	3.0	350	"current steering"	Van den Bosch, JSCC, Mar.'01
1988	95	15.45	0.044	15	5	2.5-5	2000		Schouwenaars, JSCC, Dec. '88

Litterature

- Johns & Martin: "Analog Integrated Circuit Design"
- Franco Maloberti: "Data Converters"

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Next week, 1/3:

- More on Nyquist Analog to Digital Converters (ch. 4 in "Maloberti"

- Messages are given on the INF4420 homepage.

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