

Nyquist Analog to Digital Converters

Tuesday, March 1st, 9:15 – 11:00

Snorre Aunet (sa@ifi.uio.no)
Nanoelectronics group
Department of Informatics
University of Oslo

February the 22th

- **3.1 Introduction**
- 3.1.1 DAC applications
- 3.1.2 Voltage and current references
- **3.2 Types of converters**
- **3.3 Resistor based architectures**
- 3.3.1 Resistive divider
- 3.3.2 X-Y selection
- 3.3.3 Settling of the output voltage
- 3.3.4 Segmented architectures
- 3.3.5 Effects of mismatch
- 3.3.6 Trimming and calibration
- 3.3.7 Digital Potentiometer
- 3.3.8 R-2R Resistor Ladder DAC
- 3.3.9 Deglitching

3.4 Capacitor based architectures

- 3.4.1 Capacitive divider DAC
- 3.4.2 Capacitive MDAC
- 3.4.3 "Flip around" MDAC
- 3.4.4 Hybrid capacitive resistive DACs

3.5 Current source based architectures

- 3.5.1 Basic operation
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- 3.5.4. Current sources selection
- 3.5.5 Current switching and segmentation
- 3.5.6 Switching of current sources

3.6 Other architectures (The contents refer to "Maloberti")

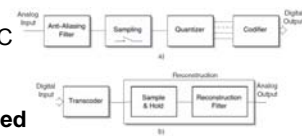
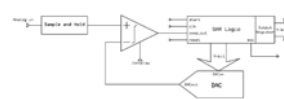


Figure 1.1. Block diagram of the basic functions of an AD (a) and a DA (b) converter.



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- Contents of Chapter 4:
- 4.1 Introduction
- 4.2 Timing accuracy
- 4.3 Full flash converters
- 4.4 Sub-ranging and two-step converters
- 4.5 Folding and interpolation
- 4.6 Time interleaved converters
- 4.7 Successive approximation converter
- 4.8 Pipeline converters
- 4.9 Other architectures

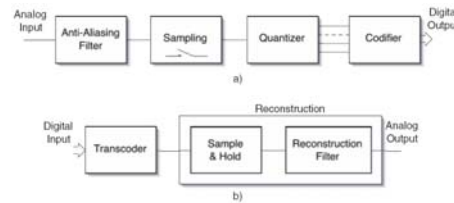
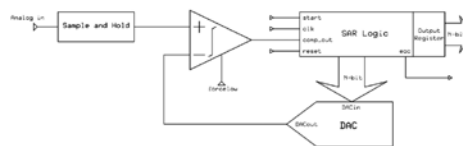


Figure 1.1. Block diagram of the basic functions of an A/D (a) and a D/A (b) converter.



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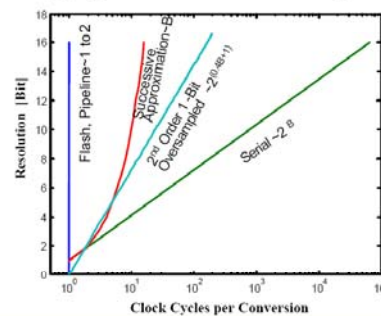
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ADCs and throughput (1 of 2)



- Depending on the bandwidth of the input signal, ADCs may use one or multiple clock cycles per conversion.

Throughput Rate Comparison



ADCs and throughput (2 of 2)



- Depending on the bandwidth of the input signal, ADCs may use one or multiple clock cycles per conversion.

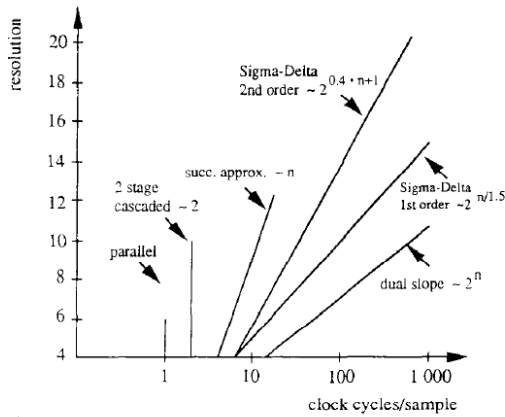


Fig. 1: Resolution vs. clock cycles/sample for different ADC algorithms

Full Flash Converters

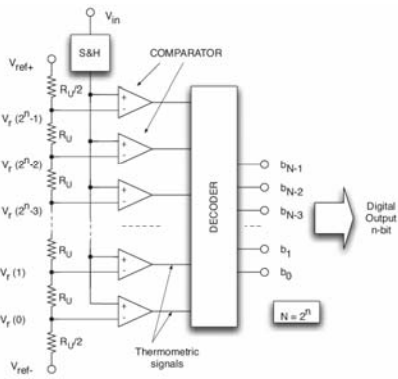


Figure 4.4. Basic block diagram of the full-flash converter.

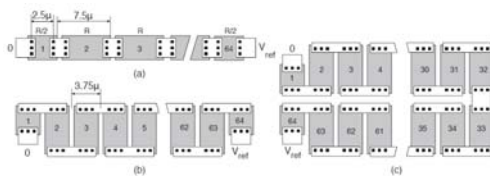
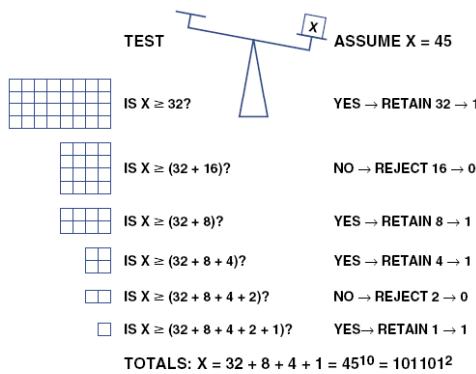


Figure 4.5. Resistive divided layout using different layout strategies.

- Compare input with all transition points between adjacent quantization intervals - "brute force"
- Quick – 1 CP, "flash".
- n bit: $2^n - 1$ reference voltages and comparators.
- "1" output up to a certain level, "0" over: thermometer code.
- ROM decoder.
- Quantization step $\Delta = (V_{ref+} - V_{ref-}) / 2^n - 1$, with first and last step equal to $\Delta/2$.

Successive approx ADC algorithm



- If we have weights of 1 kg, 2 kg, 4 kg, 8 kg, 16 kg, 32 kg and will find the weight of an unknown X assumed to be 45 kg.

$$101101_2$$

$$= 1 \cdot 32 + 0 \cdot 16 + 1 \cdot 8 + 1 \cdot 4 + 0 \cdot 2 + 1 \cdot 1$$

$$= 45_{10}$$

Figure 4. Successive-approximation ADC algorithm using balance scale and binary weights.

Which ADC Architecture Is Right for Your Application?

By Walt Kester [walt.kester@analog.com]

Successive approximation converter

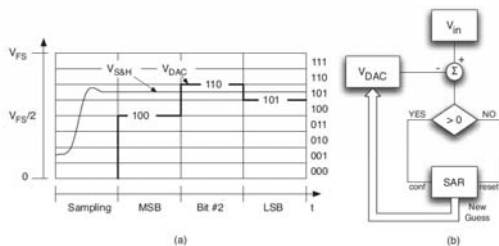


Figure 4.28. Timing (a) and flow diagram (b) of the successive approximation technique.

- Multiple clock periods
- Exploits knowledge of previously determined bits to find next significant bit.
- Low complexity and low power consumption
- For a given dynamic range $0 - V_{FS}$ the MSB distinguishes between input signals below or above $V_{FS} / 2$. Comparing the input with $V_{FS} / 2$ obtains the first bit as seen in Fig. 4.28 a)
- Fig. 4.29 shows a typical block diagram.

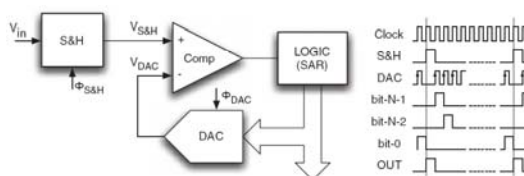


Figure 4.29. Basic circuit diagram of the successive approximation algorithm.

Successive approximation converter

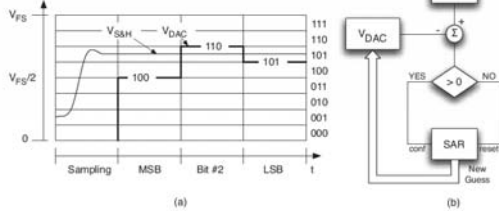


Figure 4.28. Timing (a) and flow diagram (b) of the successive approximation technique.

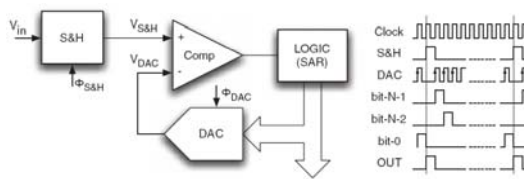


Figure 4.29. Basic circuit diagram of the successive approximation algorithm.

- For a given dynamic range 0 to V_{FS} the MSB distinguishes between input signals below or above $V_{FS} / 2$. Comparing the input with $V_{FS} / 2$ obtains the first bit as seen in Fig. 4.28 a)
- The knowledge of the MSB restricts the search for the next bit to either the upper or lower half of the 0 to V_{FS} interval. Threshold for second bit is $V_{FS} / 2$ or $3V_{FS} / 4$ (the case here).
- After this the next bit is chosen and next bit can be estimated .
- The timing diagram (upper left) describes the case for three bits.
- Voltages for comparisons are generated by a DAC under control of the SAR register.

Successive approximation converter

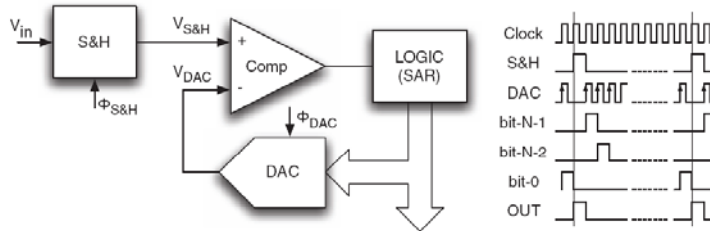
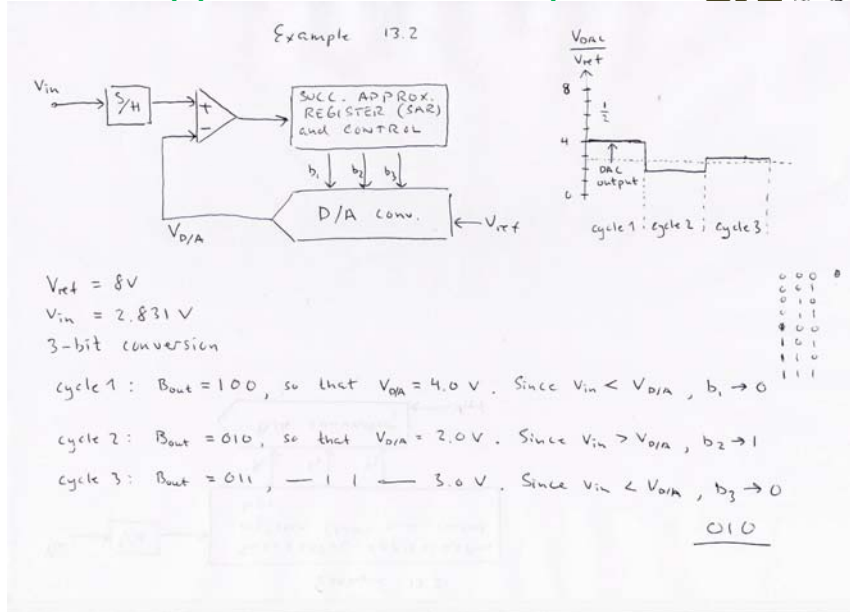


Figure 4.29. Basic circuit diagram of the successive approximation algorithm.

- Timing diagram: S/H samples the input during the 1st clock period and holds it for N successive clock intervals.
- The DAC is controlled by the SAR algorithm (Fig. 4.28 b))
- Initially the SAR sets MSB to 1 as a prediction, though this may be changed to 0.
- The process continues until all n bits have been determined.
- As the start of the next conversion (while the S&H is sampling the next input, the SAR provides the n-bit output and resets the registers.
- The name of the algorithm comes from the fact that the voltage from the DAC is an improving approximation of the sampled input voltage.

Succ. Approx ADC, example 13.2 in J&M



Sub-ranging and Two-step converters

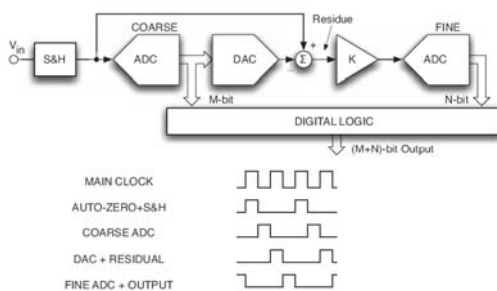


Figure 4.10. Block diagram of sub-ranging ($K=1$) and two-step architectures ($K>1$).

- Sub-ranging and two-step ADCs have better speed-accuracy tradeoff than full flash for $n>8$.
- 2 (or 3) clock periods per conversion, but smaller number of comparators and thus benefiting silicon area, power consumption and capacitive loading of the S/H.
- The DAC converts the M MSBs back to an analog signal that is subtracted from the held input that is converted to digital by the 2nd N-bit flash that yields the LSBs.
- Digital Logic combine coarse and fine bits to obtain the $n = (M+N)$ bit output.
- Sub-ranging ADCs does not have the amplification by K (two-step has).

Sub-ranging and Two-step converters

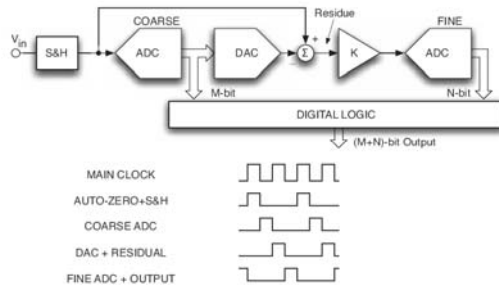


Figure 4.10. Block diagram of sub-ranging ($K=1$) and two-step architectures ($K>1$).

- Fig. 4.10 shows the timing diagram.
- Four logic signals (below main clock signal) are derived from the main clock.
- Assuming half a clock period is used to provide each function or group of functions means that 2 clock periods are enough for 1 conversion.
- For an 8 bit conversion: $M = N = 4 \rightarrow 2(16-1) = 30$ comparators are needed, instead of 255 for an 8-bit flash ADC.
- The spared area and power are much more than what is needed for the DAC and residue generator.
- S/H is only loaded by 2^M comp.

Folding and interpolation

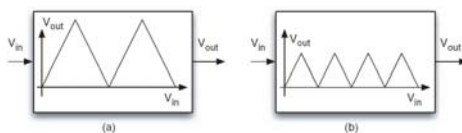


Figure 4.17. Non-linear blocks that obtain input folding.

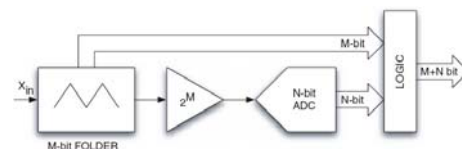


Figure 4.18. Basic architecture of a folding converter.

- Splits the input range into a number of sectors
- Single folding bends the input around $\frac{1}{2} V_{FS}$ and gives rise to 2 sectors (1-bit) with peak amplitude $\frac{1}{2} V_{FS}$.
- Folding 2 times leads to 4 sectors (2-bit) with peak amplitude $\frac{1}{4} V_{FS}$.
- M bit folding needs $2^{n-M}-1$ comparators to complete an n-bit conversion.
- Knowledge of which segment the input is in determines the MSBs, which are combined with LSBs for M+N-bit output.

Folding and interpolation

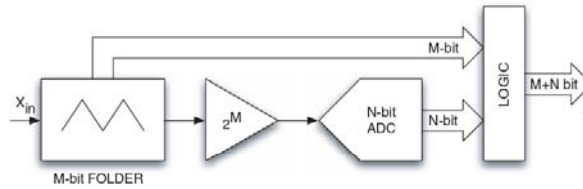
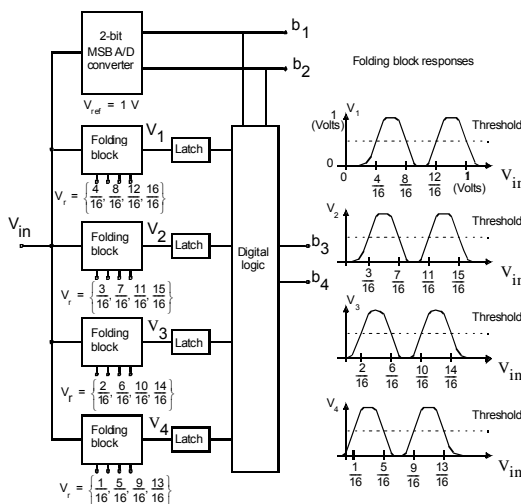


Figure 4.18. Basic architecture of a folding converter.

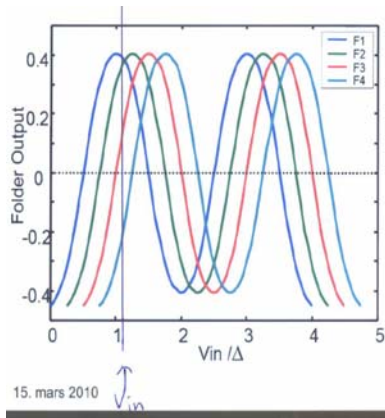
- Fig. 4.18 is a conceptual block diagram: The M-bit folder produces the analog folded output and the M-bit code which identifies which segment the output is in. The gain stage augments the dynamic range to become V_{FS} . The N-bit ADC determines the LSBs that are combined with the MSBs to give the overall output of $n = (N+M)$ bits.
- The folding circuit is normally used for high conversion rates and medium-high resolutions.

Folding A/D Converters (13.7)



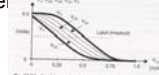
- The number of latches is reduced compared to the interpolating ADC, and even more from FLASH
- The figure shows a 4 bit converter with folding rate of 4
- A group of LSBs are found separately from a group of MSBs.
- The MSB converter determines whether the input signal, V_{in} , is in one of four voltage regions (between 0 and $\frac{1}{4}$, $\frac{1}{4}$ and $\frac{1}{2}$, $\frac{1}{2}$ and $\frac{3}{4}$, or $\frac{3}{4}$ and 1)
- V_1 to V_4 produce a thermometer code for each of the four MSB regions

Similar to folding block responses on previous slide



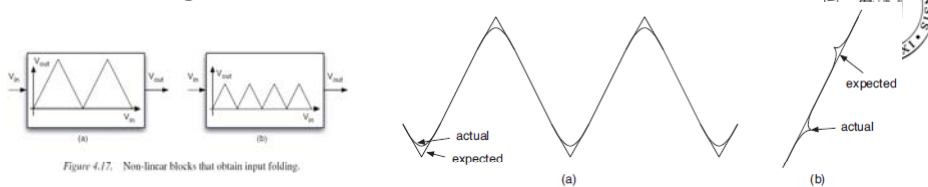
- Bipolar folder outputs
- Ex: Input 1.05:
- F1 > threshold=0 -> "1"
- F2 > threshold=0 -> "1"
- F3 > threshold=0 -> "1"
- F4 < threshold=0 -> "0"
- Thermometer code produced for each of the four MSB regions (between 0 and 1/4, 1/4 and 1/2, 1/2 and 3/4, or 3/4 and 1 for previous slide)
- (in certain respects related to inter 3.24)

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Folding – problems with unsharp edges



- Sharp edges are desired, but hard to obtain.
- Linearity is good in the regions midway between the folding points and becomes bad as the input approaches the segment borders.
- This may give rise to an INL which sometimes can make the method impractical. There is a solution..

2 folders to avoid non-linear regions



Figure 4.19. (a) Real folding response and (b) its unfolded version.

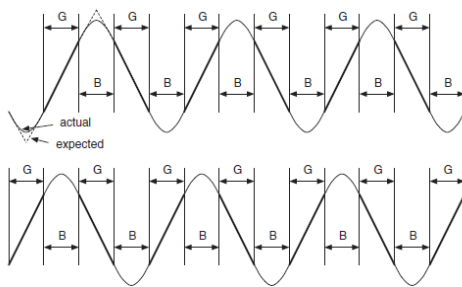


Figure 4.20. The use of double folding avoids non-linear regions.

- Bad regions may be discarded and only good ones used.
- 2 folders and transfer characteristics shifted by a quarter of the folding period.
- → One folder is always in the linear region.
- The combining logic (MSBs + LSBs) must take into account the sign of the slope in the used segment and decide which folder provides the best linear response.

Interpolation

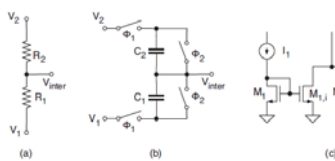
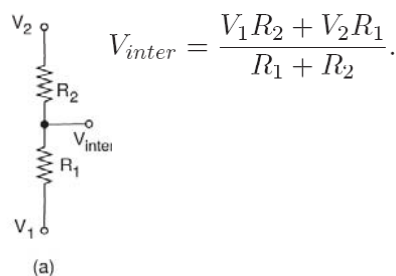


Figure 4.21. Simple circuits that achieve interpolation.



- Interpolation provides an electrical value that is intermediate between two other electrical quantities.
- Voltage inputs: resistive or capacitive dividers
- Current inputs: schemes based on current mirrors.

Interpolation in Flash ADCs (ch. 4.5.4)

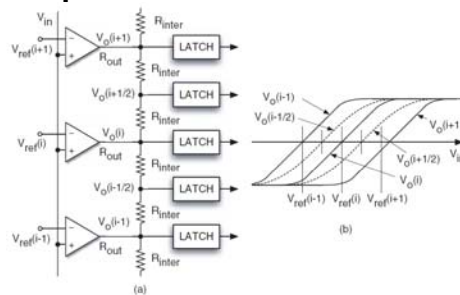


Figure 4.22. a) Use of interpolation in flash converters. b) Outputs and interpolated responses.

- Reduces the number of preamplifiers by generating the median of adjacent pre-amplifier outputs. This interpolated voltage is then used by intermediate latches.
- Equal slopes at the zero crossing equalize the speed and the metastability error of the latches.
- The number of pre-amps (and reference voltages diminish by a factor of 2, reducing the capacitive load on the S/H. (may be extended to 4 or 8 resistors between neighbouring pre-amplifiers.
- → less power consumption or higher speed.

Time-Interleaved Converters (ch. 4.5.4)

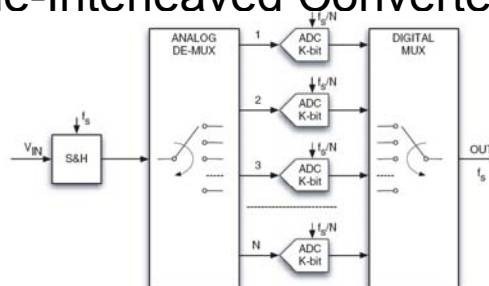


Figure 4.27. Time-interleaved architecture.

- Converters working in parallel for simultaneous quantization of input samples.
- A suitable combination of the results makes the operation equivalent to a single converter whose speed has been increased by a factor equal to the number of parallel elements.
- An alternative solution that relaxes the demanding specification associated with one full speed S/H employs one S/H in each path.
- Problems: gain mismatch between channels transformed into dynamic errors.

Time-Interleaved – best compromise between complexity and sampling rate – may be used for different architectures [Elbjornsson '05]

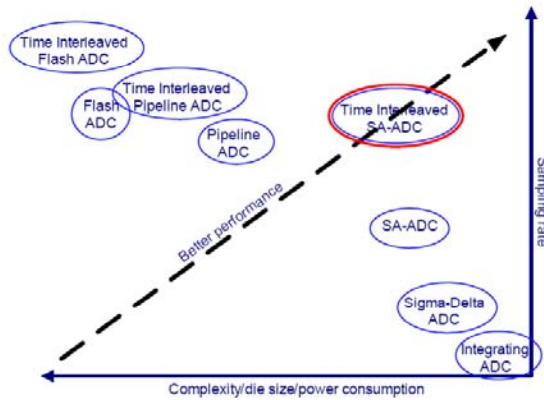


Figure 7 Comparison between ADC architectures. The time interleaved successive approximation ADC gives the best compromise between complexity and sampling rate.

Pipeline Converters (ch. 4.8)

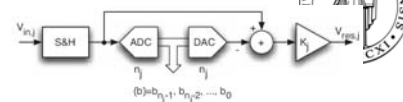
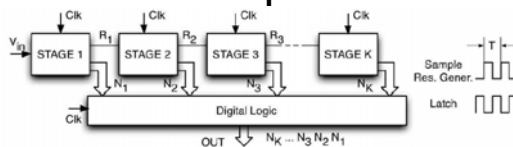


Figure 4.36. Block diagram of a pipeline stage.

Figure 4.34. Pipeline architecture.

S&H	S&H n	S&H n+1	S&H n+2				
Stage 1	b_9-b_8 n-1	b_9-b_8 n	b_9-b_8 n+1	b_9-b_8 n+2			
Stage 2		b_9-b_8 n-1	b_7-b_6 n	b_7-b_6 n+1	b_7-b_6 n+2		
Stage 3			b_5-b_4 n-1	b_5-b_4 n	b_5-b_4 n+1	b_5-b_4 n+2	
Stage 4				b_3-b_2 n-1	b_3-b_2 n	b_3-b_2 n+1	b_3-b_2 n+2
Stage 5					b_1-b_0 n-1	b_1-b_0 n	b_1-b_0 n+1
Digital					OUT n-1	OUT n	
	n	n+1	n+2	n+3	n+4	n+5	n+6

Figure 4.35. Timing control of a 2-bit per stage 10-bit pipeline.

Two-step expanded to a multi-step algorithm and implemented as a pipeline architecture.

- May generate multiple bits / stage.
- Total resolution is given by the sum of the bits at each stage.
- Fig. 4.36: generic pipeline stage.

Pipelined ADC -example

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 7, JULY 2005

A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18- μm Digital CMOS

Terje Nortvedt Andersen, Bjørnar Hernes, Member, IEEE, Ate Briskemyr, Frode Telsto, Johnny Bjørnsen, Member, IEEE, Thomas E. Bonnerud, and Øystein Moldsvor

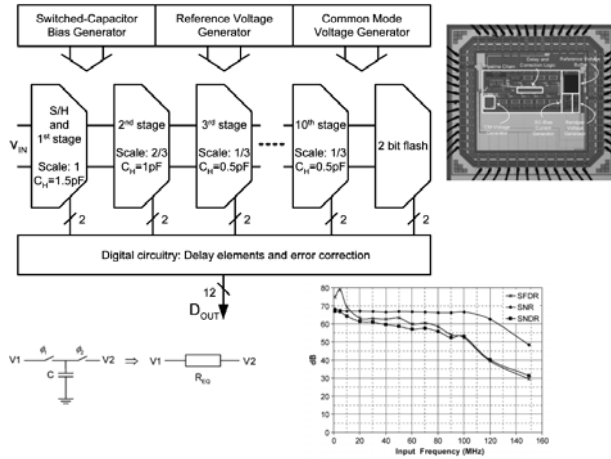


Fig. 9. SFDR, SNR, and SNDR versus input frequency. The conversion rate and signal swing are 110 MS/s and $2^3 V_{DD}$, respectively.

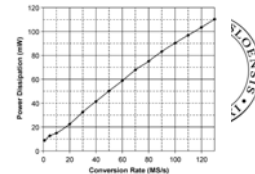


Fig. 7. Power dissipation versus conversion rate. The input frequency and signal swing is 10 MHz and $2^3 V_{DD}$, respectively.

Nominal sampling rate	110 MS/s
Technology	0.18 μm digital CMOS
Nominal supply voltage	1.5V
Resolution	12 bit
Full scale analog input	$2^3 V_{DD}$
Area	0.86 mm ²
Power consumption	97 mW
DNL	± 1.2 LSB
INL	-1.5 ± 1 LSB
SNR ($f_{in}=10$ MHz)	67.1 dB
SFDR ($f_{in}=10$ MHz)	64.2 dB
SFDR ($f_{in}=10$ MHz)	69.4 dB
ENOB ($f_{in}=10$ MHz)	10.4 bit

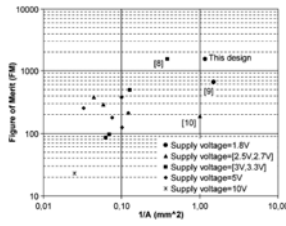


Fig. 12. Figure of Merit (FOM) versus $1/A$ for 12-bit ADCs. f_{clk} is given in MS/s, A is given in mm² and P_{DTP} is given in mW.

Integrating converters (ch. 4.9.2)

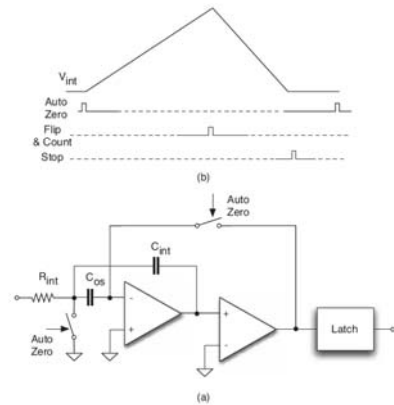
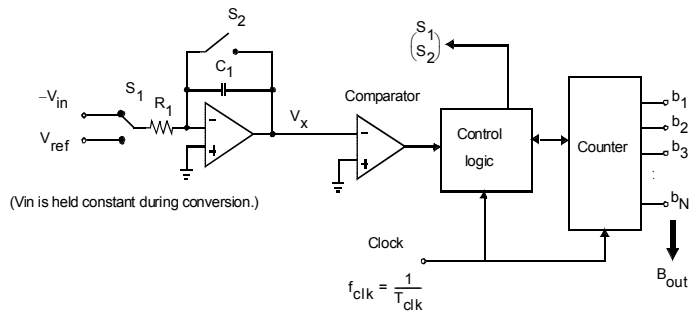


Figure 4.50. Waveforms of a two-slope ADC (a) and (b) offset cancelled scheme.

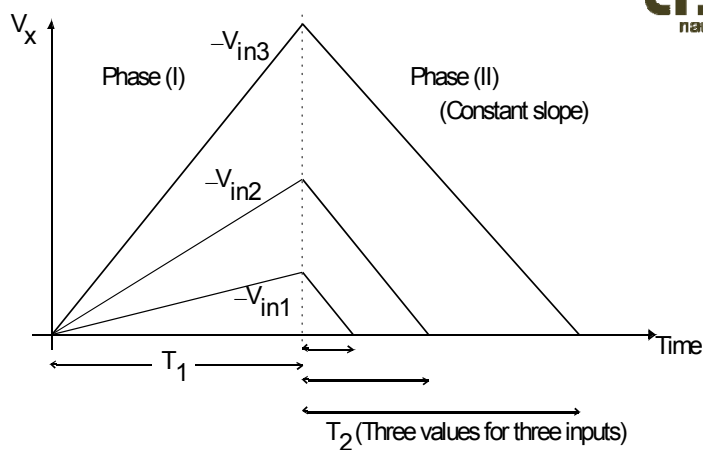
- Input signal determines the slope of the output from the integrator.
- When it's shifted, the slope becomes fixed, and the time it takes to return is measured by a counter, and translated to a digital output.

Integrating Converters (13.1)



- $V_x(t) = V_{in} t / RC$ (V_x ramp derivative depending on V_{in})
- High linearity and low offset/gain error
- Small amount of circuitry
- Low conversion speed
 - $2^{N+1} * 1/T_{clk}$ (Worst case)

Integrating Converters



- The digital output is given by the count at the end of T_2
- The digital output value is independent of the time-constant RC

COMPARATOR OFFSET

V_{ref+}
 V_{ref-}
 V_{LSB}
 V_{ref-}

V_{in}
 S/H
 R_n
 R_{n-1}
 R_{n-2}
 \dots
 R_1
 V_{ref-}

b_{n-1}
 b_{n-2}
 \dots
 b_0
 $N = 2^n$

$V_{LSB} = \frac{V_{FS}}{2^n}$

Input offset voltage: voltage required to drive the output voltage to zero

Comp. offset is added to the diff. input and modifies the threshold transition. Offset in a flash architecture alter the i th quantization interval Δ :

$$\Delta_i = V_{thr,i} - V_{thr,i-1} = \Delta - Vos,i + Vos,i-1$$

To ensure no missing codes or monotonicity for a given yield, the max. value of the offset must be lower than $\frac{1}{2}$ LSB divided by the number of sigma required to obtain that yield.

Ex:

NORMAL DISTRIBUTION

99.6% within $\pm 3\sigma$

COMPARATOR OFFSET

Example: 8-bit FLASH, 1V FS, 99.9% yield:

$$V_{LSB} = \frac{1V}{2^8} = 3.90625 \text{ mV}$$

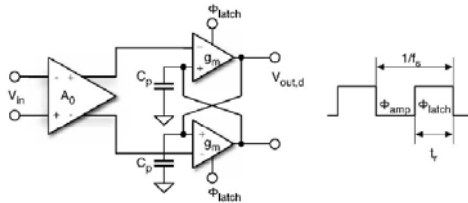
$$\frac{1}{2} V_{LSB} = 0.001953125 \text{ V} = 1.953125 \text{ mV}$$

To ensure 99.9% yield, the corresponding sigma with a normal distribution of errors is $\sigma = 3.3$

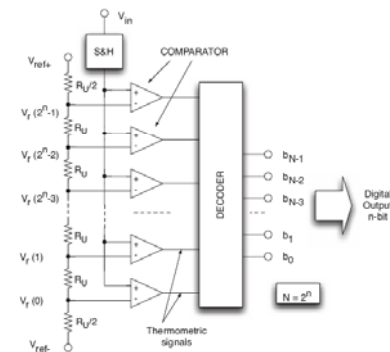
$$\frac{1}{2} V_{LSB} : 3.3 \Rightarrow 1.953125 \text{ mV} / 3.3 = 0.592 \text{ mV}$$

The offset is mainly caused by the pre-amplifier of the comparator \Rightarrow Design the 1st stage and optimize the layout for minimum threshold, transcend. param. μ_{ox} and W/L mismatches in the input diff. pair and active loads $\Delta V_{th} = \frac{A_{VS}}{\sqrt{W/L}}$.

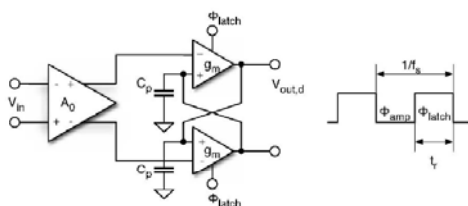
Metastability – probability of undefined comparator output



- A sampled-data comparator is typically realized using a pre-amplifier and a latch.
- Φ_{amp} , Φ_{latch} (latch logic level)
- If $V_{in,d}$ is too small, the comparator may be undefined at the end of the latch phase giving an **error** in the **output** code and possibly causing a code **bubble** error in the **thermometric** output of some converter architectures (or other circuits making use of comparators).



Metastability – probability of undefined comparator output



- V_0 : voltage swing for valid logic levels
- $t_r = \Phi_{latch} \rightarrow$ Probability of a metastability error increases with the sampling frequency and at high frequencies becomes equal to 1 (since more than 1 is not a valid result. If P_E is according to eq. 4.11 > 1 , the result means P_E is 1.)
- P_E is inversely proportional to the input amplitude $V_{in,d}$.

The differential latch of Fig. 4.3 is the positive loop of two transconductors whose regenerative time constant, τ_L , is

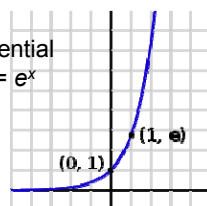
$$\tau_L \approx \frac{C_p}{g_m} \quad (4.10)$$

The metastability error probability can be approximated by

$$P_E = \frac{V_0}{V_{in,d}} e^{-t_r/\tau_L} \quad (4.11)$$

where V_0 is the voltage swing required for valid logic levels and t_r is the period of the latch phase.

The exponential function $y = e^x$

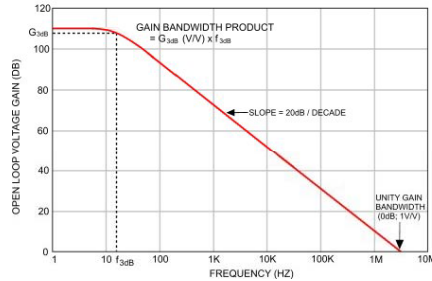


Approximate Evaluation of max frequency of operation for ADCs (1/2)

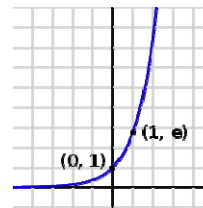


- f_{Tech} : Technology unity gain frequency
- f_T : unity gain frequency of OTA or op-amp
- $f_T = f_{Tech} / \alpha$, where α is at least 2-4 (ultimately depending on accuracy).
- $f_{CK} = f_T / \gamma$, where γ is a suitable margin between the op-amps f_T and the clock frequency, f_{CK} , as some time for settling is needed. ($f_{CK} < f_T$)
- In order to estimate γ , suppose that the input V_{in} is a step at $t = 0$.
- A single pole band-limitation gives rise to an output $V_{out}(t)$ (approaching V_{in}) given by:

$$V_{out}(t) = V_{in}(1 - e^{-t/\tau}) \quad (4.1)$$



$$A_{OL} = V_{out}/(V^+ - V^-)$$



The exponential function $y = e^x$

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Approximate Evaluation of max frequency of operation for ADCs (2/2)



- f_{Tech} : Technology unity gain frequency
 - f_T : unity gain frequency of OTA or op-amp
 - $f_T = f_{Tech} / \alpha$, where α is at least 2-4 (ultimately depending on accuracy).
 - $f_{CK} = f_T / \gamma$, where γ is a suitable margin between the op-amps f_T and the clock frequency, f_{CK} , as some time for settling is needed. ($f_{CK} < f_T$)
 - In order to estimate γ , suppose that the input V_{in} is a step at $t = 0$.
 - A single pole band-limitation gives rise to an output $V_{out}(t)$ (approaching V_{in}) given by:
- Since an n-bit ADC needs an accuracy better than $2^{-(n+1)}$, the settling time must be

$$t_{sett} > \tau \cdot (n + 1) \ln(2)$$

$$f_{CK} < \frac{\pi \beta f_T}{(n + 1) \ln(2)} \quad (4.3)$$

$$\gamma = \frac{f_T}{f_{CK}} > \frac{(n + 1) \ln(2)}{\pi \beta} \quad (4.4)$$

- Since the time allowed for settling is half clock frequency.

$$V_{out}(t) = V_{in}(1 - e^{-t/\tau}) \quad (4.1)$$

$$\tau = \frac{1}{2\pi\beta f_T} \quad (4.2)$$

β - feedback factor - how much of the output is fed back to the negative input

The foresen order of the anti-aliasing filter sets a given margin λ , which is the ratio between sampling rate and signal band. Moreover, since the conversion algorithm can use multiple clock periods (say k), the conversion rate is therefore given by $f_{CK}/(\lambda k)$.

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Litterature



- Johns & Martin: "Analog Integrated Circuit Design"
- Franco Maloberti: "Data Converters"
- http://inst.eecs.berkeley.edu/~ee247/fa04/fa04/lectures/L19_f04.pdf

SYSTEM ARCHITECTURE AND KEY COMPONENTS FOR AN 8 BIT/1 GH
GaAs MESFET ADC

J. Sauerer, R. Hagelauer, F. Oehler, G. Rohmer, U. Schlag, D. Seitzer +
T. Grave, W. Kellner ++

+ FHG IIS, Wetterkreuz 13, D-8520 Erlangen, Germany
++ Siemens Research Laboratories, Otto-Hahn-Ring 6, D-8000 Munich, Germany

Which ADC Architecture Is Right for Your Application?

By Walt Kester [walt.kester@analog.com]

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Next week, 01/03:



- Next week: To be defined..
- Messages are given on the INF4420 homepage.
- Questions: sa@ifi.uio.no , 22852703 / 90013264