

# Switched Capacitor Circuits

Tuesday, March 8th, 9:15 – 11:00

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## March the 1st

- Contents of Chapter 4:
- 4.1 Introduction
- 4.2 Timing accuracy
- 4.3 Full flash converters
- 4.4 Sub-ranging and two-step converters
- 4.5 Folding and interpolation
- 4.6 Time interleaved converters
- 4.7 Successive approximation converter
- 4.8 Pipeline converters
- 4.9 Other architectures

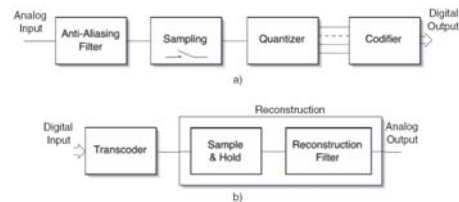
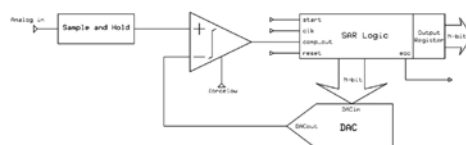


Figure 1.1. Block diagram of the basic functions of an A/D (a) and a D/A (b) converter.



7. mars 2011

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## March the 8th –Switched Capacitor Circuits



- Intro to SC-circuits
- 12.3 Switched Capacitor Amplifiers
- 12.3.1 Unity-Gain Sampler / Buffer
- 12.3.2 Noninverting amplifier
- 12.4 Switched-Capacitor Integrator
- Examples, incl. Oversampling converters.
- Report Writing

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## Folding and interpolation

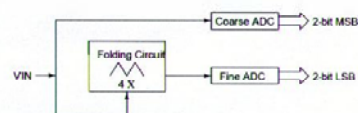


Fig. 1 Block diagram of 4 × folding ADC

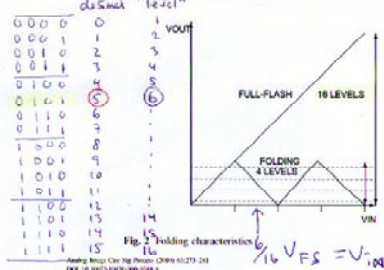


Fig. 2 Folding characteristics

Source: IEEE, Circuits and Systems, 2009, 51:273-281

DOI: 10.1109/TCAS.2009.5091088

A threshold inverter quantization based folding and interpolation ADC in 0.18 μm CMOS

Robert Najarian - Roy Palit

- Fig. 2 illustrates the operation of the folding circuit.
- The coarse quantizer determines where the input lies for the folding amplifier.
- Total resolution:  $N_{MSB} + N_{LSB}$
- If the input is in the lower  $1/4$  of  $V_{FS}$ , the two MSBs,  $b_3b_2=00$ .
- If the input is in the range  $1/4 V_{FS}$  to  $2/4 V_{FS}$ , the two MSBs,  $b_3b_2=01$ .
- If the input is in the range  $2/4 V_{FS}$  to  $3/4 V_{FS}$ , the two MSBs,  $b_3b_2=10$ .
- If the input is in the range  $3/4 V_{FS}$  to  $4/4 V_{FS}$ , the two MSBs,  $b_3b_2=11$ .
- If the output from the folding circuit is above the lowermost folding level ("11"), but below the 2nd fl, the two LSBs are  $b_1b_0=00$ .
- If the output from the folding circuit is above the 2nd fl, but below the 3rd fl, the two LSBs are  $b_1b_0=01$ .
- If the output from the folding circuit is above the 3rd, but below the 4th fl, the two LSBs are  $b_1b_0=10$ .
- If the output from the folding circuit is above the 4th fl the two LSBs are  $b_1b_0=11$ .
- Example 1:  $V_{in} = 6/16 V_{FS}$ ;  $b_3b_2=01$ , Output from the folding circuit between 2nd and 3rd fl;  $b_1b_0=01$ .
- $0101 = 0 \cdot 8 + 1 \cdot 4 + 0 \cdot 2 + 1 \cdot 1 = 5$

# Switched Capacitor Circuits



- Sensing / sampling the input only at periodic instants of time, processing the each sample and producing a valid output at the end of each period; "discrete-time" or "sampled-data" systems.
- Simple building blocks like samplers, amplifiers and integrators provide the foundation for more advanced circuits and topics.
- Filters, comparators, (oversampling) ADCs and DACs.
- Well suited for CMOS implementation, due to good switches (low  $R_{on}$ , no offset) and high input impedance amplifiers.

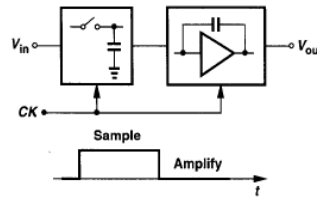


Figure 12.7 General view of switched-capacitor amplifier.

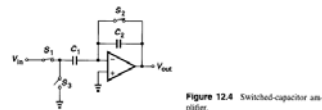
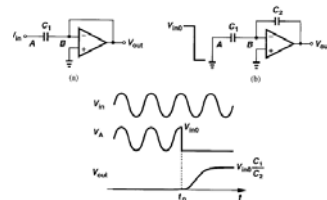


Figure 12.4 Switched-capacitor amplifier.



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## Properties of SC circuits



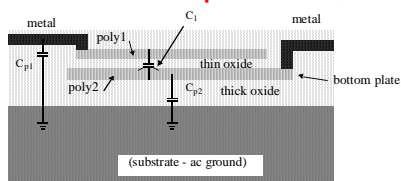
- Popular due to accurate frequency response, good linearity and dynamic range
- Easily analyzed with z-transform
- Typically require aliasing and smoothing filters
- Accuracy is obtained since filter coefficients are determined from capacitance ratios, and relative matching is good in CMOS
- The overall frequency response remains a function of the clock, and the frequency may be set very precisely through the use of a crystal oscillator
- SC-techniques may be used to realize other signal processing blocks like for example gain stages, voltage-controlled oscillators and modulators

Basic building blocks in SC circuits; Opamps, capacitors, switches, clock generators

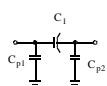


- **DC gain** typically in the order of 40 to 80 dB (100 – 10000x)
- **Unity gain** frequency should be > 5 x clock speed (rule of thumb)
- **Phase margin** > 70 degrees (according to "Johns & Martin")
- Unity-gain and phase margin highly dependent on the load capacitance, in SC-circuits. In single stage opamps a doubling of the load capacitance halves the unity gain frequency and improve the phase margin
- The finite **slew rate** may limit the upper clock speed.
- Nonzero **DC offset** can result in a high output dc offset, depending on the topology chosen, especially if correlated double sampling is not used

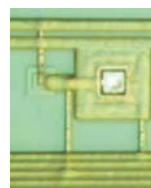
Basic building blocks in SC circuits; Opamps, capacitors, switches, clock generators



cross-section view

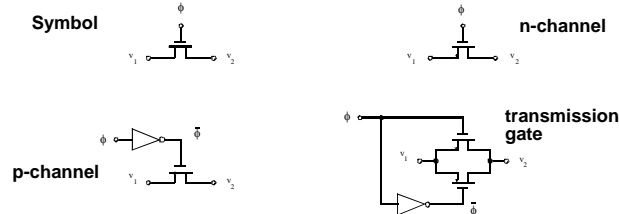


equivalent circuit



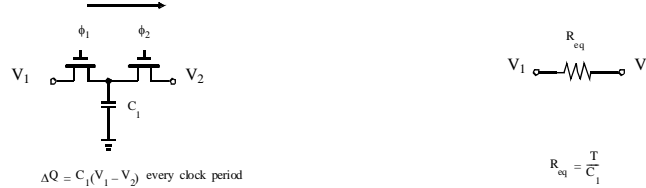
- Typically constructed between two polysilicon layers
- Parasitics; Cp1, Cp2.
- Parasitic Cp2 may be as large as 20 % of the desired, C1
- Cp1 typically 1- 5 % of C1. Therefore, the equivalent model contain 3 capacitors

## Basic building blocks in SC circuits; Opamps, capacitors, switches, clock generators



- Desired: very **high off-resistance** (to avoid leakage), relatively **low on-resistance** (for fast settling), no offset
- Phi, the **clock signal**, switches between the **power supply levels**
- Convention: Phi is high means that the switch is on (shorted)
- Transmission gate switches may increase the signal range
- Some nonideal effects: nonlinear capacitance on each side of the switch, charge injection, capacitive coupling to each side

## SC Resistor Equivalent (1/2)



$$Q_x = C_x V_x$$

$C_1$  is first charged to  $V_1$  and then charged to  $V_2$  during one clock cycle

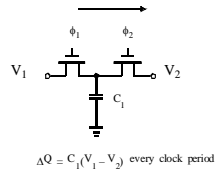
$$\Delta Q_1 = C_1(V_1 - V_2)$$

The average current is then given by the change in charge during one cycle

$$I_{avg} = \frac{C_1(V_1 - V_2)}{T}$$

Where  $T$  is the clock period (1/fs)

## SC Resistor Equivalent (2/2)



$$\Delta Q = C_1(V_1 - V_2) \text{ every clock period}$$



$$R_{eq} = \frac{T}{C_1}$$

The current through an equivalent resistor is given by:

Combining the previous equation with  $I_{avg}$ :

$$I_{eq} = \frac{V_1 - V_2}{R_{eq}}$$

The resistor equivalence is valid when  $f_s$  is much larger than the signal frequency. In the case of higher signal frequencies, z-domain analysis is required :

$$R_{eq} = \frac{T}{C_1} = \frac{1}{C_1 f_s}$$

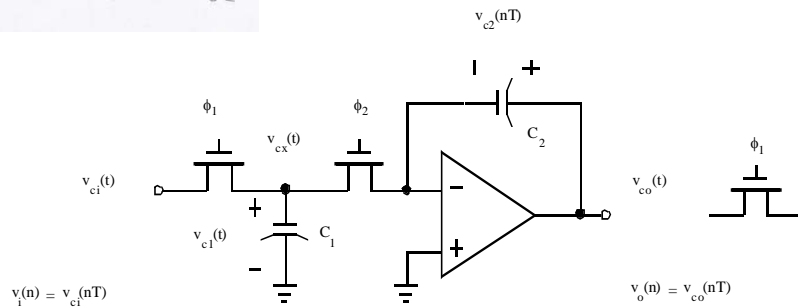
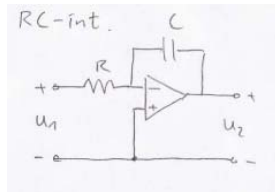
## Example of resistor implementation



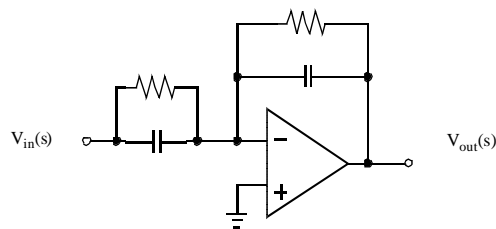
- What is the resistance of a 5 pF capacitance sampled at a clock frequency of 100 kHz?
- Note the large resistance that can be implemented. Implemented in CMOS it would take a large area for a plain resistor of the same resistance

$$R_{eq} = \frac{1}{(5 \times 10^{-12})(100 \times 10^3)} = 2M\Omega$$

## An inverting integrator



## First-Order Filters



- Select a known Active-RC circuit
- Replace resistors by SC-equivalents
- Analyze using discrete-time methods

# Unity-Gain Sampler/Buffer

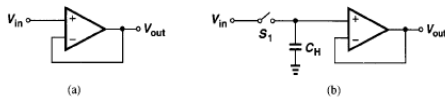


Figure 12.29 (a) Unity-gain buffer, (b) sampling circuit followed by unity-gain buffer.

- A unity gain amplifier can be realized with no resistors and capacitors in the feedback, but still requires a sampling circuit (Fig. 12.29 b))
- The input-dependent charge injected by  $S_1$  onto  $C_H$  limits the accuracy.
- We'll see a **SC-implementation that does not have significant problems with charge injection**, if proper clocking is used (Fig. 12.30).
- Three switches control the operation.

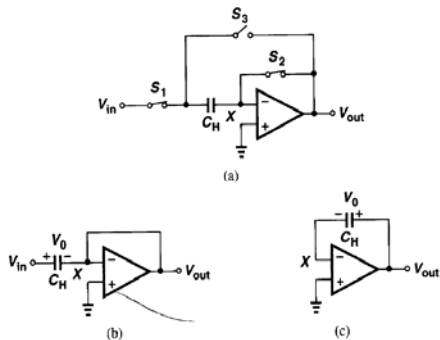


Figure 12.30 (a) Unity-gain sampler, (b) circuit of (a) in sampling mode, (c) circuit of (a) in amplification mode.

## Unity-Gain Sampler/ buffer in sampling and amplification mode

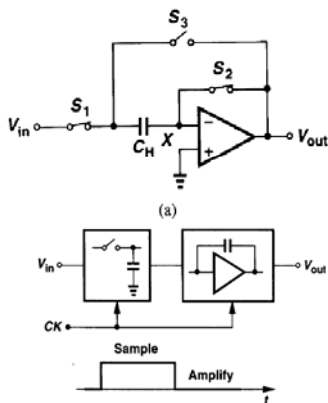


Figure 12.7 General view of switched-capacitor amplifier.

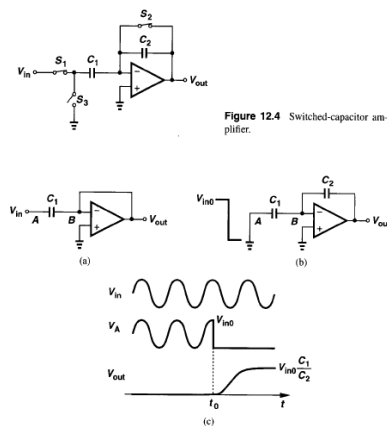


Figure 12.5 Circuit of Fig. 12.4 in (a) sampling mode, (b) amplification mode.

- Sample:  $S_1$  and  $S_2$  are on,  $S_3$  off. For a high gain opamp,  $V_B = V_{out} \approx 0$  and the voltage across  $C_1$  equal to  $V_{in}$ .
- Amplify:  $S_3$  on,  $S_1$  and  $S_2$  are off.  $A$  to ground. Since  $V_A$  changes from  $V_{in}$  to 0,  $V_{out}$  changes to  $V_{in0} C_1 / C_2$ .



### Continuous time implementation vs the SC implementation

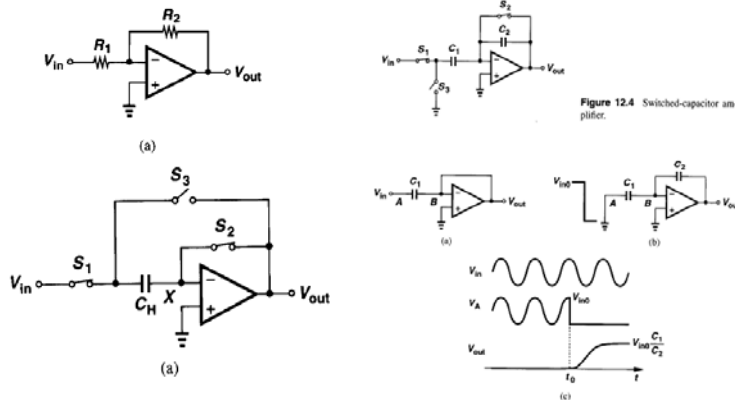


Figure 12.5 Circuit of Fig. 12.4 in (a) sampling mode, (b) amplification mode.

- The SC implementation **samples** the input, setting the **output to zero** and provides **amplification** of the input in the **next** period, while **ignoring the input voltage**. The circuit configuration changes from one phase to another, raising stability concerns.
- When  $V_{out}$  have settled, the current through  $C_2$  approaches zero, while  $R_2$  continuously loads the amplifier.

### Unity-Gain Sampler/Amplifier ; turning $S_2$ off slightly before $S_1$ , to avoid problems with charge injection

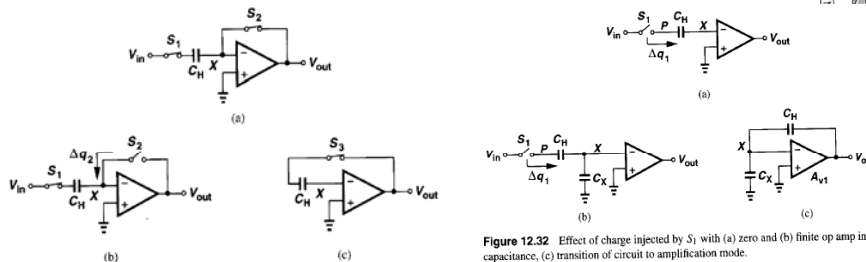


Figure 12.31 Operation of the unity-gain sampler in slow motion.

Figure 12.32 Effect of charge injected by  $S_1$  with (a) zero and (b) finite op amp input capacitance, (c) transition of circuit to amplification mode.

- Fig. 12.31 shows "slow motion";  $S_2$  injects  $\Delta q_2$  onto  $C_H$ , producing an error  $\Delta q_2 / C_H$ , which is quite independent (The body effect makes  $V_{TH}$  a function of  $V_{in}$ ) of the input level since node X is at virtual ground. **Only an offset** (rather than gain error or nonlinearity is produced)
- $\Delta q = WLC_{ox} V_{eff} = WLC_{ox} (V_{GS} - V_{TH}) = WLC_{ox} (V_{CK} - V_X - V_{TH})$
- Suppose  $V_{in}=0$  and  $S_1$  injects  $\Delta q_1$  onto P.  $C_X$  is the total capacitance from X to ground. The **total charge at X cannot change after  $S_2$  turned off** (no dc path in or out). The same holds true after  $C_H$  is placed around the opamp. The output voltage is **not influenced by charge injection due to  $S_1$** .
- After the feedback circuit has settled, the charge on  $C_H$  equals  $V_0 C_H$ , unaffected by  $S_3$  ( $S_3$  introducing no error).

Unity-Gain Sampler/Amplifier and generation of proper clock edges ensuring that  $S_1$  turns off after  $S_2$  does

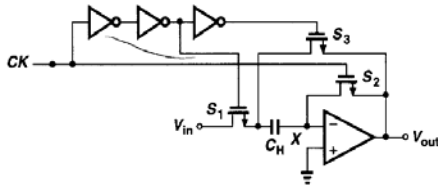


Figure 12.33 Generation of proper clock edges for unity-gain sampler.

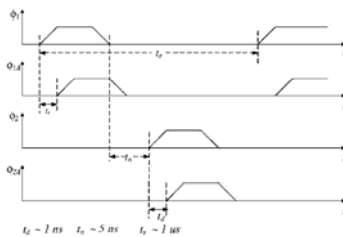


Figure 4. Nonoverlapping clock phases.

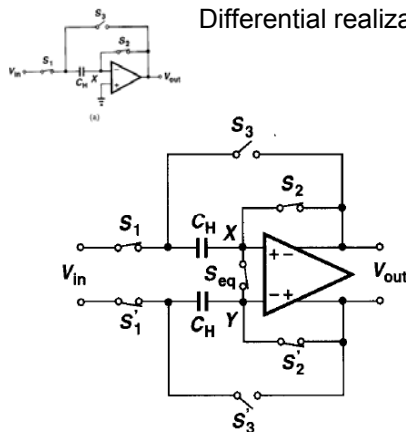
- Skewed clocks (left) often used, for example in Sigma-Delta modulators for oversampling converters.

A MICRO POWER SIGMA-DELTA A/D CONVERTER IN 0.35- $\mu$ M CMOS FOR LOW FREQUENCY APPLICATIONS

Adnan Gundakci<sup>1,2</sup>, William N. Carr<sup>1</sup>

<sup>1</sup>New Jersey Institute of Technology, Newark, NJ 07102  
<sup>2</sup>Telephonics Corporation, 815 Broad Hollow Road, Farmingdale, NY 11735

Differential realization of unity-gain sampler



- With proper timing the charge injected by  $S_1$  and  $S_3$  is unimportant and the charge injected by  $S_2$  results in a constant offset voltage

- The differential implementation uses two sampling capacitors, so that the charge injected by  $S_2$  and  $S_2'$  appears as a common-mode disturbance at nodes X and Y.
- The finite charge injection mismatch between  $S_2$  and  $S_2'$  is resolved by adding  $S_{eq}$ , that turns off slightly after  $S_2$  and  $S_2'$  (and before  $S_1$  and  $S_1'$ ), thereby equalizing the charge at nodes X and Y.

## unity-gain sampler precision considerations

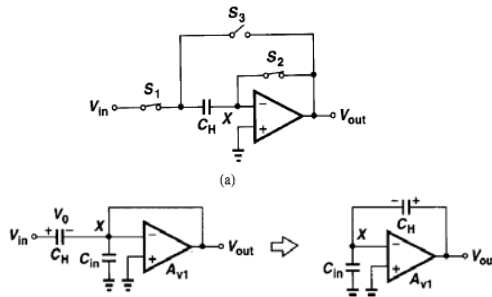


Figure 12.35 Equivalent circuit for accuracy calculations.

$$V_{out} = \frac{V_0}{1 + \frac{1}{A_{v1}} \left( \frac{C_{in}}{C_H} + 1 \right)} \quad (12.43)$$

$$\approx V_0 \left[ 1 - \frac{1}{A_{v1}} \left( \frac{C_{in}}{C_H} + 1 \right) \right] \quad (12.44)$$

- A finite input capacitance,  $C_{in}$ , is assumed.
- In the **amplification mode** the circuit from Fig. 12.30 operates as a **unity-gain** buffer. How close to unity?

### Example 12.4

In the circuit of Fig. 12.35,  $C_{in} = 0.5$  pF and  $C_H = 2$  pF. What is the minimum op amp gain that guarantees a gain error of 0.1%?

### Solution

Since  $C_{in}/C_H = 0.25$ , we have  $A_{v1,min} = 1000 \times 1.25 = 1250$ .

- The input capacitance should be minimized even if speed is not critical. (Larger input transistors mean higher  $C_{in}$ .)

**Noninverting amplifier** ; final output having same **polarity** as  $V_{in0}$  and the possibility of **gain**  $> 1$ .

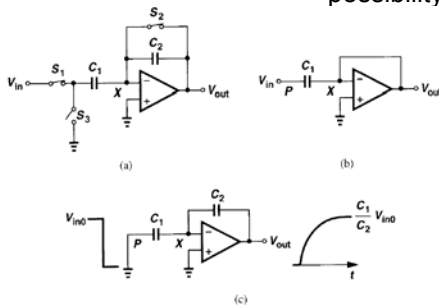


Figure 12.41 (a) Noninverting amplifier. (b) circuit of (a) in sampling mode. (c) transition of circuit to amplification mode.

- **Sample**:  $S_1$  and  $S_2$  on,  $S_3$  off. Virtual ground at X. The voltage across  $C_1$  tracks  $V_{in}$ . At the end of the sampling mode,  $S_2$  turns off, injecting  $\Delta_{q2}$  on X. Subsequently  $S_1$  turns off, and in
- **Amplification mode**,  $S_3$  turns on.

- Since  $V_p$  goes from  $V_{in0}$  to 0, the output voltage changes from 0 to approximately  $V_{in0}(C_1/C_2)$ .
- **Input dependent charge injection** is again **avoided** by proper **timing**, turning  $S_2$  off before  $S_1$ .  $V_{out}$  is free for errors due to  $S_1$  and  $S_3$ , and offset due to  $S_2$  can be suppressed by **differential** operation (Fig. 12.46).

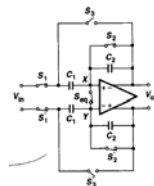


Figure 12.46 Differential realization of noninverting amplifier.

## Noninverting amplifier – timing and behaviour

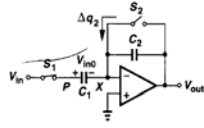


Figure 12.42 Transition of noninverting amplifier to amplification mode.

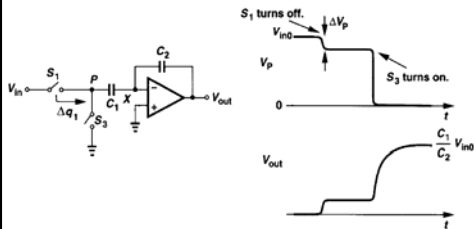


Figure 12.43 Effect of charge injected by  $S_1$ .

- After  $S_3$  turns on,  $V_p$  drops to zero. Thus the overall change in  $V_p$  is equal to  $0 - V_{in0} = -V_{in0}$ , producing an overall change in the output equal to  $-V_{in0}(-C_1/C_2) = V_{in0}C_1/C_2$
- $V_p$  goes through an intermediate perturbation but the output of interest is measured after P is connected to ground, so that charge injected by  $S_1$  does not affect the final output.
- From  $S_2$  turns off to  $S_1$  turns off,  $V_{in}$  may undergo changes that does not introduce any error; sampling instant is defined by the turn-off of  $S_2$ .
- **In summary:** Proper timing ensures that node X is perturbed by only the charge injection of  $S_2$ , making the final  $V_{out}$  free from errors due to  $S_1$  and  $S_3$ . Offset due to  $S_2$  may be suppressed by differential operation
- $S_2$  turns off before  $S_1$ , making the circuit insensitive to charge injection (total charge at X constant) of  $S_1$  or charge "absorption" of  $S_3$ .
- $\Delta q_1$  gives rise to  $\Delta V_p = \Delta q_1/C_1$ , and the output voltage by  $-\Delta q_1/C_2$ .

## Noninverting amplifier – timing and behaviour

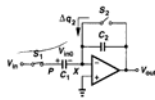


Figure 12.42 Transition of noninverting amplifier to amplification mode.

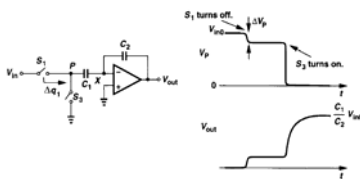


Figure 12.43 Effect of charge injected by  $S_1$ .

- **In summary:** Proper timing ensures that node X is perturbed by only the charge injection of  $S_2$ , making the final  $V_{out}$  free from errors due to  $S_1$  and  $S_3$ . Offset due to  $S_2$  may be suppressed by differential operation.
- Differential implementation shown in Figure 12.46.

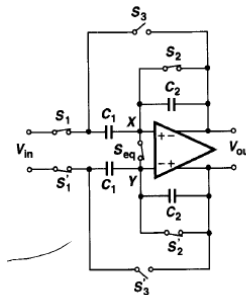


Figure 12.46 Differential realization of noninverting amplifier.

## Switched Capacitor Integrator

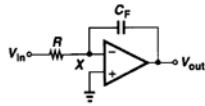


Figure 12.52 Continuous-time integrator.

$$V_{out} = -\frac{1}{RC_F} \int V_{in} dt,$$

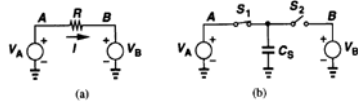


Figure 12.53 (a) Continuous-time and (b) discrete-time resistors.

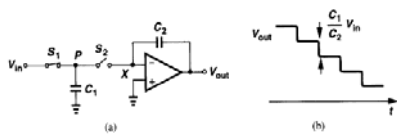


Figure 12.54 (a) Discrete-time integrator, (b) response of circuit to a constant input voltage.

Used in filters and oversampling ADCs.

For sampled data systems we use a discrete time counterpart to the continuous time integrator.

- Continuous time resistor:  $I = (V_A - V_B)/R$
- SC:  $I_{av} = C_s(V_A - V_B)f_{CK}^{-1} = C_s(V_A - V_B)f_{CK}$ ; the average current flowing from A to B being the charge moved in one clock period.
- A resistance is simulated by the SC-circuit.
- Figure 12.54 shows the discrete time integrator.
- In every clock cycle  $C_1$  absorbs a charge equal to  $C_1 V_{in}$  when  $S_1$  is on and deposits the charge on  $C_2$  when  $S_2$  is on. Approximating the staircase with a ramp, we note that the circuit behaves as an integrator.

## Switched Capacitor Integrator -drawbacks

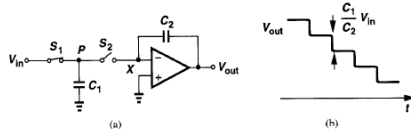


Figure 12.54 (a) Discrete-time integrator, (b) response of circuit to a constant input voltage.

The final value of  $V_{out}$  in Fig. 12.54(a) after every clock cycle can be written as

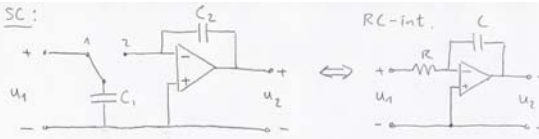
$$V_{out}(kT_{CK}) = V_{out}[(k-1)T_{CK}] - V_{in}[(k-1)T_{CK}] \cdot \frac{C_1}{C_2}. \quad (12.64)$$

- Input dependent charge injection of  $S_1$  introduces nonlinearity in the charge stored on  $C_1$  and hence the output voltage.
- The nonlinear capacitance at node P resulting from S/D junctions of  $S_1$  and  $S_2$  leads to nonlinear charge to voltage conversion when  $C_1$  is switched to X, giving an nonlinear component at the output.
- An integrator topology that resolves both issues may be found (in Fig. 12.56 a)) in "Razavi".

## Transfer function for simple discrete time integrator



SC:



$$Q = C \cdot V$$

$$f = \frac{1}{T} \dots$$



Svitsjen er ved tidspunkt  $t = (n-1)T$  i posisjon 1, og det blir tatt en punktvise ("et sampel") av  $u_1(t)$ , da  $C_1$  blir ladet til:

$$q_1[(n-1)T] = C_1 \cdot u_1[(n-1)T]$$

Ladningen på  $C_2$  er (samtidig):

$$q_2[(n-1)T] = C_2 \cdot u_2[(n-1)T]$$

Ved tidspunkt  $t = n \cdot T$  blir ladningen på  $C_1$  overført til  $C_2$  ved at svitsjen er i posisjon 2.

Hele ladningen på  $C_1$  blir ført over til  $C_2$  fordi operasjonsforsterker tvinger spenningen over  $C_1$  til å bli null.

Ladn. på  $C_1$  subtraheres dermed fra ldn. på  $C_2$ .

Ladn. på  $C_2$  ved  $t = nT$  blir dermed:

$$q_2[nT] = q_2[(n-1)T] - q_1[(n-1)T]$$

$$C_2 \cdot u_2[nT] = C_2 \cdot u_2[(n-1)T] - C_1 \cdot u_1[(n-1)T]$$

$$u_2[nT] = u_2[(n-1)T] - \frac{C_1}{C_2} \cdot u_1[(n-1)T]$$

Kan benytte z-transform

$$\text{cos: } \text{If } x(n) \Leftrightarrow X(z), \text{ then } x(n-k] \Leftrightarrow z^{-k} X(z)$$

$$U_2(z) = U_2(z) \cdot z^{-1} - \frac{C_1}{C_2} U_1(z) z^{-1}$$

$$\frac{U_2(z)}{U_1(z)} = -\frac{C_1}{C_2} \cdot \frac{z^{-1}}{(1-z^{-1})}$$

ref.: Nils Haakeim: Analog (MS) Universitetet i Trondheim - NTH, 1994

## Improved Switched Capacitor Integrator without charge injection problems

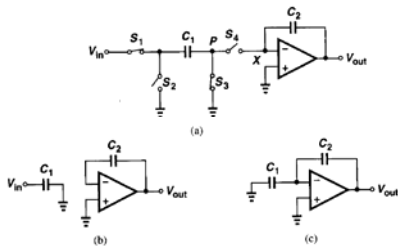
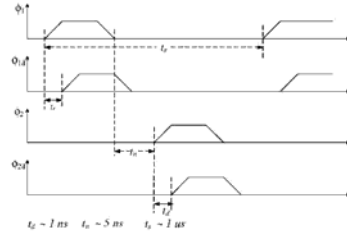
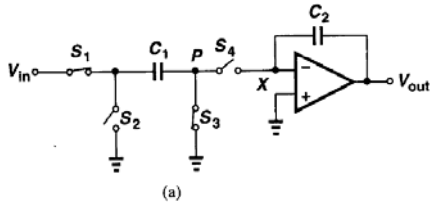


Figure 12.56 (a) Parasitic-insensitive integrator, (b) circuit of (a) in sampling mode, (c) circuit of (a) in integration mode.

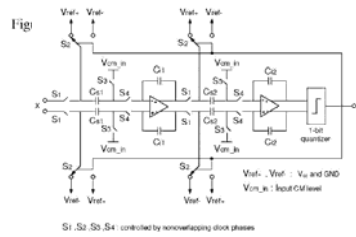
$$\Delta q = WLC_{OX} V_{\text{eff}} = WLC_{OX} (V_{GS} - V_{TH})$$

- **Sampling mode:**  $S_1$  and  $S_3$  on,  $C_1$  tracks  $V_{in}$ .
- In the transition to the **integration** mode  $S_3$  turns off first, injecting a constant charge onto  $C_1$ .  $S_1$  turns off next, and subsequently  $S_2$  and  $S_4$  turns on (Fig. 12.56 c)). The charge stored on  $C_1$  is transferred to  $C_2$  via the virtual ground node. Since  $S_3$  turns off first, it introduces only a **constant offset**, which can be suppressed by differential operation.
- Moreover, since the left plate of  $C_1$  is "driven" (section 12.3.2), the **charge injection or absorption** of  $S_1$  and  $S_2$  contributes no error.
- Also, since node X is a virtual ground, the **charge** injected or absorbed by  $S_4$  is **constant** and independent of  $V_{in}$ .
- **Nonlinear junction capacitances** of  $S_3$  and  $S_4$  have voltages going from near zero in sampling mode to virtual ground in integration mode  $\rightarrow$  **negligible nonlinear contribution** to the output voltage.

Unity-Gain Sampler/Amplifier and generation of proper clock edges ensuring that  $S_1$  turns off after  $S_2$  does



- Similar integrators widely used in oversampling ADCs exploiting SC  $\Delta\Sigma$  modulators/ $\Sigma\Delta$  modulators



A MICRO POWER SIGMA-DELTA A/D CONVERTER IN 0.35- $\mu$ M CMOS FOR LOW FREQUENCY APPLICATIONS

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Improved Switched Capacitor Integrator

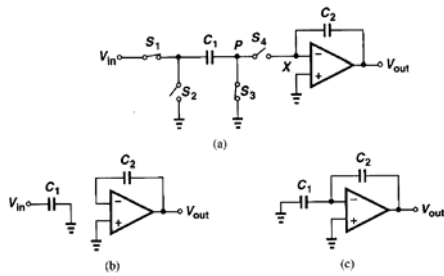


Figure 12.56 (a) Parasitic-insensitive integrator, (b) circuit of (a) in sampling mode, (c) circuit of (a) in integration mode.

- Sampling mode:  $S_1$  and  $S_3$  on, tracks  $V_{in}$ .
- In the transition to the integration mode  $S_3$  turns off first, injecting a constant charge onto  $C_1$ .  $S_1$  turns off next, and subsequently  $S_2$  and  $S_4$  turns on (Fig. 12.56 c)). The charge stored on  $C_1$  is transferred to  $C_2$  via the virtual ground node. Since  $S_3$  turns off first, it introduces only a constant offset, which can be suppressed by differential operation.

## Litterature



- Razavi, chapter 12.3, 12.4: Introduction to Switched Capacitor Circuits

### A MICRO POWER SIGMA-DELTA A/D CONVERTER IN 0.35- $\mu$ M CMOS FOR LOW FREQUENCY APPLICATIONS

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Next week, 15/03:



- Next week: Oversampling converters, from chapter 14 in Johns & Martin.
- Messages are given on the INF4420 homepage.
- Questions: [sa@ifi.uio.no](mailto:sa@ifi.uio.no) , 22852703 / 90013264