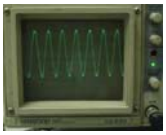
Oscillators, Phase Locked Loops

Tuesday, March 29th, 9:15 – 11:30



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Last time – and today, Tuesday 29th of March:

Oscillators
14.1 General considerations
14.2 Ring Oscillators
14.4 Voltage-Controlled Oscillators
14.5 Mathematical model of VCOs
Phase Locked Loops
15.1 Simple PLL

Last time:
From chapters 13 and 14 in Razavi;
Nonlinearity and Mismatch and
Oscillators:
13.1 Nonlinearity
13.1.1 general considerations
13.1.2 nonlinearity and differential circuits
13.1.3 effects of negative feedback on nonlin.
13.1.4 capacitor nonlinearity
13.1.5 linearization techniques
13.2 Mismatch
DC offsets, even order distortion,
13.2.1 offset cancellation techniques
13.2.2 reduction of noise by offset cancellation

Oscillators

- Clock generation
- Carrier synthesis
- Vast number of different topologies and solutions
- ”Razavi” abot analysis and design of VCOs
- Oscillation in feedback systems
- Ring osc.
- (LC osc.)
- Used in Phase Locked Loops (PLLs – chapter 15)

- Periodic output, usually a voltage
- Negative feedback systems can oscillate ; oscillator as ”badly designed amplifier”
- CMOS implementations typical ring oscillators or LC osc.

Oscillators

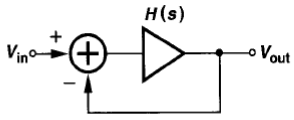


Figure 14.1 Feedback system.

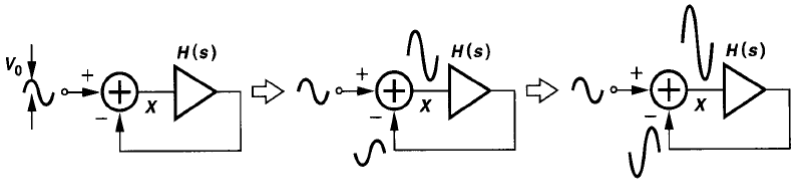


Figure 14.2 Evolution of oscillatory system with time.

- If the amplifier itself experiences so much phase shift at high frequencies that the overall feedback becomes positive, oscillation may occur.
- In Fig. 14.2 a noise component at ω_0 experiences a total gain of unity and a phase shift of 180°, returning to the subtractor as a negative replica of the input.. Upon subtraction, the input and the feedback signals give a larger difference, making the circuit ”regenerate” and the component at ω_0 to grow (if loop gain is larger than unity).

4

Barkhausen" criteria", necessary but not sufficient, for oscillation

In summary, if a negative-feedback circuit has a loop gain that satisfies two conditions:

$$|H(j\omega_0)| \geq 1 \quad (14.4)$$

$$\angle H(j\omega_0) = 180^\circ, \quad (14.5)$$

then the circuit may oscillate at ω_0. Called "Barkhausen criteria," these conditions are

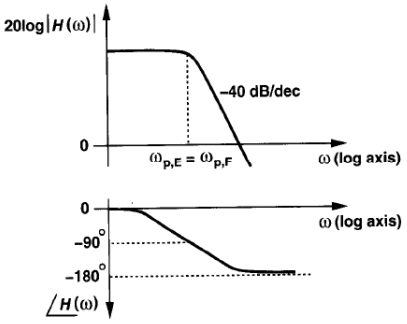


Figure 14.7 Loop gain characteristics of a two-pole system.

- Typically choose loop gain 2-3 times the required value for robustness.
- Two-pole system in Fig. 14.7; Phase shift can reach 180 degrees, but at a frequency of infinity.
- We go for greater phase shift and add a 3rd stage…

5

Ring Oscillators Ex. 14.1

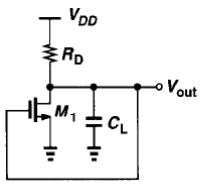
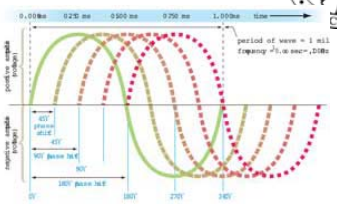


Figure 14.4



- Example 14.1 Why does not a single common source stage oscillate if it is placed in a unity-gain loop?
- Solution: From Fig. 14.4 it is seen that the open-loop circuit contains only one pole, thereby providing a maximum frequency-dependent phase shift of 90 degrees (at a frequency of infinity). Since the common source stage exhibits a dc phase shift of 180 degrees due to the signal inversion from the gate to the drain, the maximum phase shift is 270 degrees. The loop therefore fails to sustain oscillation growth.

6

Two stages

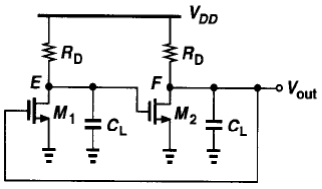


Figure 14.5 Two-pole feedback system.

- Two poles appear in the signal path, allowing the frequency-dependet phase shift to approach 180 °.

  The circuit exhibits positive feedback near zero frequency due to the signal inversion through each common-source stage. This may lead to ”latch up” rather than oscillation.

  $V_E \uparrow$: $V_F \downarrow$or vice versa. May remain indefinitely

7

Ring Oscillators

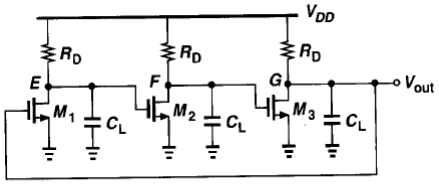


Figure 14.8 Three-stage ring oscillator.

$$H(s) = -\frac{A_0^3}{(1+\frac{s}{\omega_0})^3}.$$

$$\tan^{-1}\frac{\omega_{osc}}{\omega_0} = 60^\circ$$

$$\omega_{osc} = \sqrt{3}\omega_0.$$

$$\frac{A_0^3}{\left[\sqrt{1+(\frac{\omega_{osc}}{\omega_0})^2}\right]^3} = 1.$$

$$A_0 = 2.$$

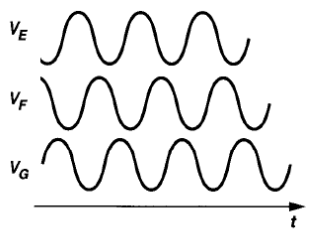
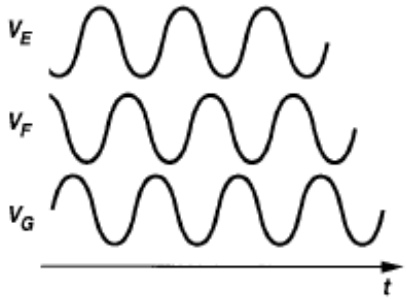


Figure 14.9 Waveforms of a three-stage ring oscillator.

- Oscillates only if the frequency-dependent phase shift equals 180 °, i.e. if each stage contributes 60 °. LF gain of 2 per stage is minimum. It oscillates at $\omega_{osc} = \sqrt{3}\omega_0.$ where ω_0 is the 3-dB bandwidth of each stage.

8

Ring osc



- Each stage contributes a frequency dependent phase shift of 60 ° as well as a low frequency signal inversion, the waveform at each node is 240 ° (or 120 °) out of phase with respect to its neighbouring nodes.
- The ability to generate multiple phases is a very useful property of ring oscillators.

9

Ring Oscillators

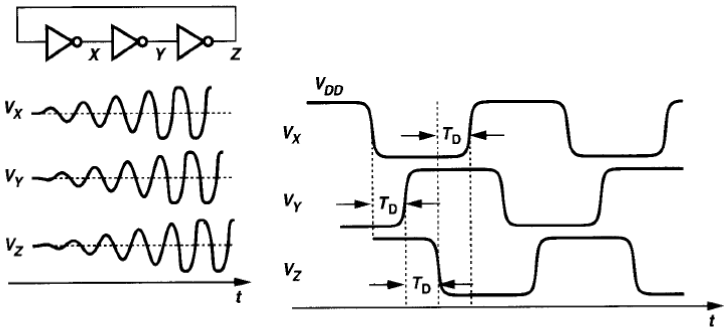


Figure 14.14 Waveforms of ring oscillator when one node is initialized at V_{DD}.

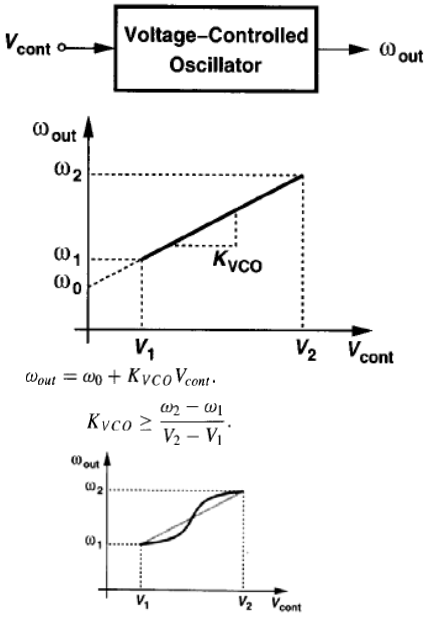
- Simple implementation without resistors. If each inverter had an initial voltage at the trip point, with identical stages and no noise in the devices, the circuit woul dremain in this state indefinitely.
- But noise components disturb each node voltage, yielding a growing waveform, and rail-to-rail swing.
- Period 6 T_D (6 inverter delays), after some time, starting with ”small signal delay” given by oscilation frequency of $\sqrt{3}A_0\omega_0/2$

10

Voltage controlled oscillators (VCOs)

- A VCO has it's oscillation frequency controlled by a voltage input.
- The frequency of oscillation is varied by the applied DC voltage, while modulating signals may also be fed into the VCO to cause frequency modulation (FM) or phase modulation (PM); a VCO with digital pulse output may similarly have its repetition rate (FSK, PSK) or pulse width modulated (PWM).
- Harmonic oscillators generate a sinus waveform.
- Relaxation oscillators can generate a sawtooth or triangular waveform.
- (from Wikipedia)

Voltage Controlled Oscillators

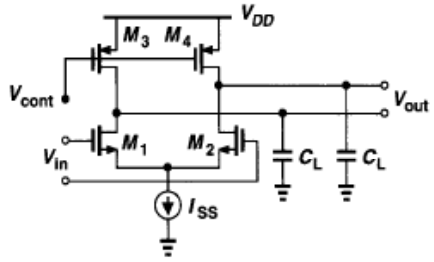


$$\omega_{out} = \omega_0 + K_{VCO} V_{cont}.$$

$$K_{VCO} \geq \frac{\omega_2 - \omega_1}{V_2 - V_1}.$$

- Ideally linear function of the control voltage (Eq. 14.55)
- K_{VCO} : "gain"; rad / s / V
- Center frequency. Could be 10 GHz or higher
- The Tuning range, $\omega_2 - \omega_1$, is dictated by; 1) variation in VCO center frequency with PT (process and temperature), and 2) frequency range necessary for the application.
- Variation in output phase and frequency as a result of noise on the control line is important. To minimize the effect, the VCO gain must be minimized (in conflict with the tuning range)
- Tuning linearity
- Output amplitude, power dissipation, supply and CMRR, output signal purity

Tuning in ring oscillators



$$f_{osc} \propto \frac{1}{T_D} \qquad (14.64)$$

$$\propto \frac{\mu_p C_{ox}(\frac{W}{L})_{3,4}(V_{DD} - V_{cont} - |V_{THP}|)}{C_L}. \qquad (14.65)$$

- $f_{osc} = (2NT_D)^{-1}$
- T_D : This large signal delay can be varied
- Increasing V_{cont} decreases f_{osc}
- Critical drawback: The output swing varies considerably accross the tuning range.

13

Reducing the output swing variation (compared to the circuit in Fig. 14.42)

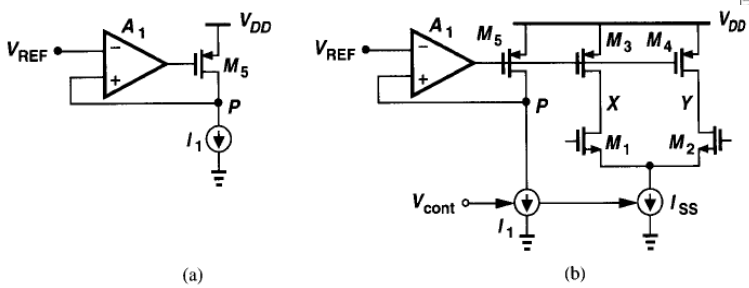


Figure 14.43 (a) Simple feedback circuit defining V_P, (b) replica biasing to define voltage swings in a ring oscillator.

- $I_{SS}R_{on3,4}$ relatively constant , tail current adjusted by V_{cont}.
- Tuning range max. 2-3
- M5 operates in deep triode
- The bandwidth of A1 is important for the settling speed of a PLL if the circuit is used for such purpose.

14

Delay variation by interpolation

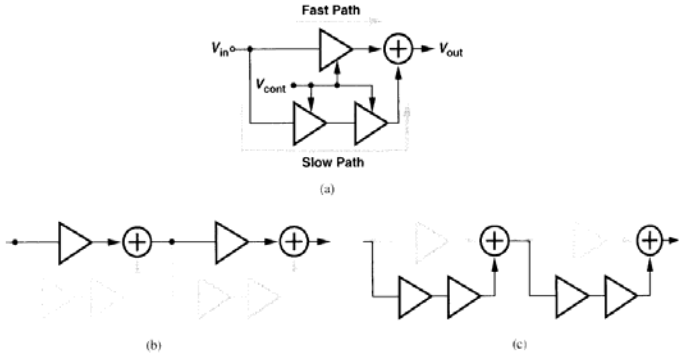


Figure 14.48 (a) Interpolating delay stage, (b) smallest delay, (b) largest delay.

- Each stage consist of a slow path and a fast path whose outputs are summed and whose gains are adjusted by V_{cont} in opposite directions.
- In one extreme only the fast path is on and the slow path disabled, and in the other extreme the slow path is on and the fast path off (providing minimum oscillating frequency).

15

Delay variation by interpolation – implementation of the concept from Fig. 14.48 on transistor level.

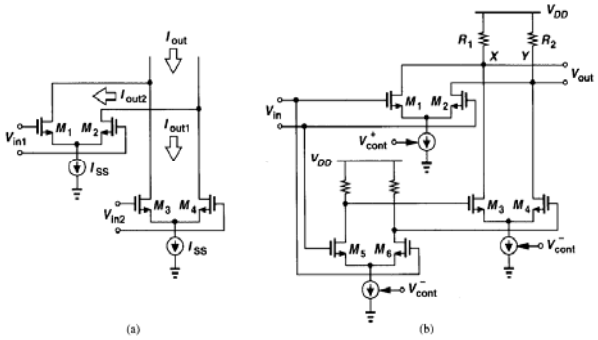
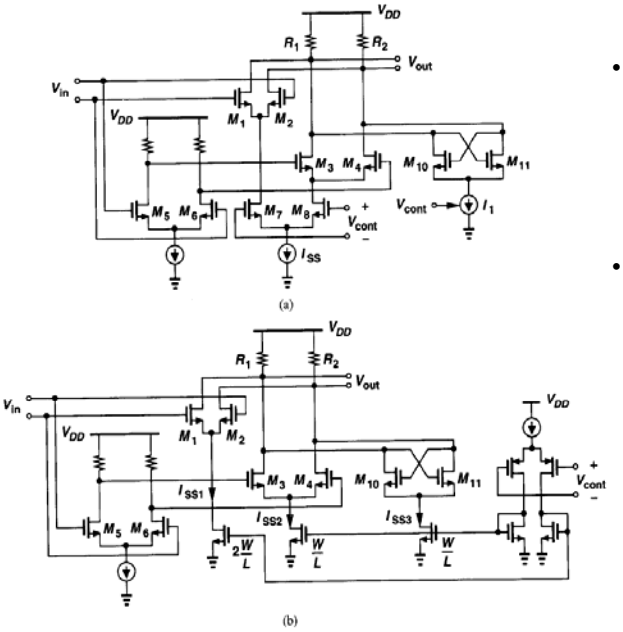


Figure 14.49 (a) Addition of currents of two differential pairs, (b) interpolating delay stage.

- Addition of currents; simply short circuiting, since the two transistors in a differential pair provide output currents. Fig. 14.49 a)
- Gain controlled by tail current
- Fig. 14.49 b); overall interpolating stage configuration. The output currents of M_1-M_2 and M_3 – M_4 are summed at X and Y and flow through R_1 and R_2, producing V_{out}.

16

Wide Range Tuning



- The oscillation frequency can be varied by more than 4 orders of magnitude (with less than twofold variation in the amplitude).
- M_5 and M_6 pull each output node to V_{dd}, creating relatively constant output swing even with large variations in I_{ss}

Mathematical Model of VCOs

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont}. \qquad (14.55)$$

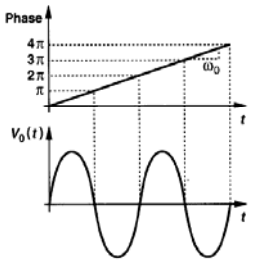


Figure 14.59 Illustration of phase of a signal.

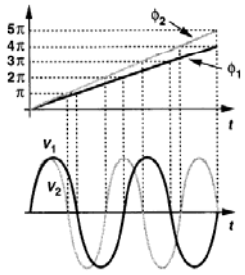


Figure 14.60 Variation of phase for two signals.

- Memoryless (Eq. 14.55)
- $V_0(t) = V_m \sin\omega_0 t$ See Fig. 14.59
- $V_1(t) = V_m \sin[\Phi_1 t]$, $V_2(t) = V_m \sin[\Phi_2 t]$, $\Phi_1 t = \omega_1 t$, $\Phi_2 t = \omega_2 t$, $\omega_1 < \omega_2$
- $V_2(t)$ accumulates phase faster. (Fig. 14.60)

$$\omega = \frac{d\phi}{dt}. \qquad (14.73)$$

Mathematical Model of VCOs

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont}. \qquad (14.55)$$

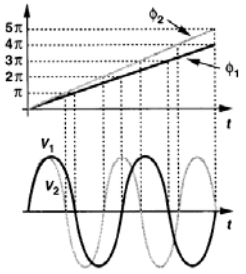


Figure 14.60 Variation of phase for two signals.

$$\omega = \frac{d\phi}{dt}. \qquad (14.73)$$

Equation (14.73) indicates that, if the frequency of a waveform is known as a function of time, then the phase can be computed as

$$\phi = \int \omega dt + \phi_0. \qquad (14.74)$$

In particular, since for a VCO, $\omega_{out} = \omega_0 + K_{VCO} V_{cont}$, we have

$$V_{out}(t) = V_m \cos\left(\int \omega_{out} dt + \phi_0\right) \qquad (14.75)$$

$$= V_m \cos(\omega_0 t + K_{VCO} \int V_{cont} dt + \phi_0). \qquad (14.76)$$

Equation (14.76) proves essential in the analysis of VCOs and PLLs.[13] The initial phase ϕ_0 is usually unimportant and is assumed zero hereafter.

As explained in Chapter 15, if a VCO is placed in a phase-locked loop, then only the second term of the total phase in Eq. (14.76) is of interest. This term, $K_{VCO} \int V_{cont} dt$, is called the "excess phase," ϕ_{ex}. In fact, in the analysis of PLLs, we view the VCO as a system whose input and output are the control voltage and the excess phase, respectively:

$$\phi_{ex} = K_{VCO} \int V_{cont} dt. \qquad (14.77)$$

That is, the VCO operates as an *ideal* integrator, providing a transfer function:

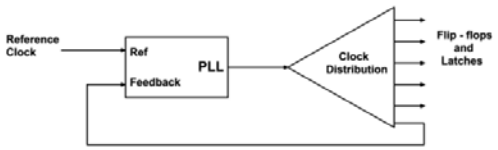
$$\frac{\Phi_{ex}}{V_{cont}}(s) = \frac{K_{VCO}}{s}. \qquad (14.78)$$

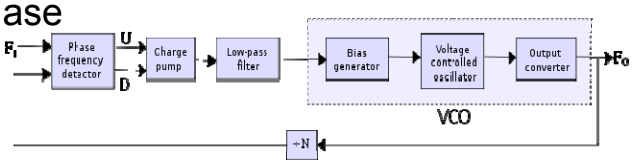
- Memoryless (Eq. 14.55)
- $V_0(t) = V_m \sin\omega_0 t$ See Fig. 14.59
- $V_1(t) = V_m \sin[\Phi_1 t]$, $V_2(t) = V_m \sin[\Phi_2 t]$, $\Phi_1 t = \omega_1 t$, $\Phi_2 t = \omega_2 t$, $\omega_1 < \omega_2$
- $V_2(t)$ accumulates phase faster. (Fig. 14.60)

19

Phase-Locked Loops (Ch. 15)

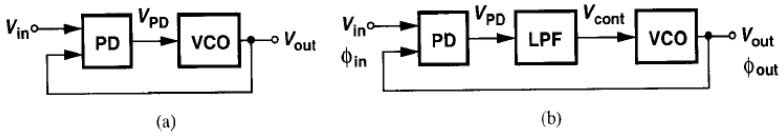
- Invented in the 1930s
- Widely used in electronics and telecomm.
- Clock generation
- Frequency synthesis
- Compares the output phase with the input phase





20

Phase-Locked Loops (Ch. 15)



(a) (b)

Figure 15.5 (a) Feedback loop comparing input and output phases, (b) simple PLL.

- The Phase Detector (”PD”) compares the phases of the input and output signals, generating an error that varies with the VCO frequency until the phases are aligned, i.e. the loop is locked.
- The PD output consists of a DC component (desirable) and high-frequency components (undesirable).
- The PD output is therefore filtered by a low-pass filter (”LPD”).
- Fig. 15.5 b) forms the basic PLL topology.

Phase-Detector

- V_{out} is ideally linearly proportional to the phase difference, $\Delta\Phi$, between the two inputs, crossing the origin for $\Delta\Phi = 0$.
- ”gain”; slope of the line, K_{PD}, is expressed in V/rad.
- The function in Fig. 15.1 may be implemented by an XOR followed by a LP filter.
- XOR(A,B) outputs 1 if and only if A ≠ B. The DC level of the output is proportional to $\Delta\Phi$.
- The XOR produces error pulses on both rising and falling edges, while other types of PD may respond only to positive or negative transitions.

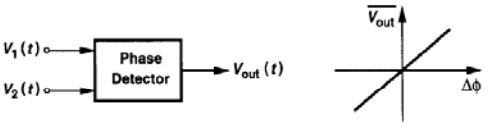


Figure 15.1 Definition of phase detector.

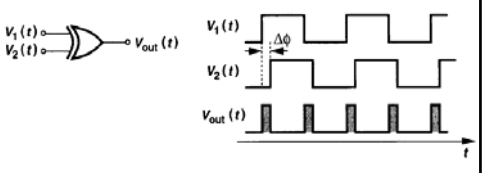


Figure 15.2 Exclusive OR gate as phase detector.

Phase Detector

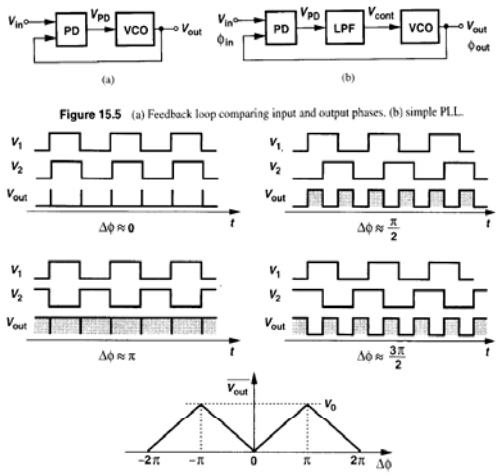


Figure 15.5 (a) Feedback loop comparing input and output phases. (b) simple PLL.

Figure 15.3

- The average output voltage rises to $[V_0 / \Pi] \times \Pi / 2 = V_0/2$ for $\Delta\Phi = \Pi/2$ and V_0 for $\Delta\Phi = \Pi$. For $\Delta\Phi > \Pi$, the average begins to drop. The characteristic is periodic, exhibiting both negative and positive gains.

23

Basic PLL Topology – phase alignment through temporary frequency change

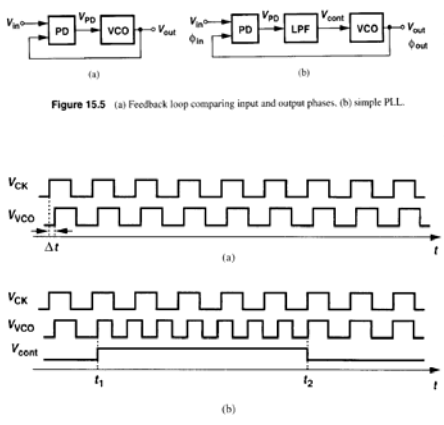


Figure 15.5 (a) Feedback loop comparing input and output phases. (b) simple PLL.

Figure 15.4 (a) Two waveforms with a skew, (b) change of VCO frequency to eliminate the skew.

- Problem of aligning the output phase of the VCO with the phase of a reference clock.
- Fig. 15.4 a): The rising edges of V_{VCO} are "skewed" by Δt seconds with respect to V_{CK}, and we wish to eliminate this error.
- V_{cont} is the only control input to the VCO. To vary the phase, the frequency has to be varied. In Fig. 15.4 b) the frequency is stepped to a higher value at t_1. The circuit accumulates phase, gradually decreasing the phase error. At $t = t_2$ it drops to zero, and V_{cont} is returned to it's original value. V_{cont} and V_{CK} remain aligned.

24

Basic PLL Topology – phase alignment through temporary frequency change

Figure 15.5 (a) Feedback loop comparing input and output phases. (b) simple PLL.

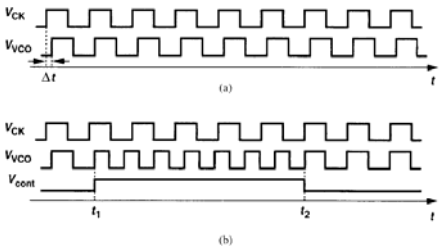


Figure 15.4 (a) Two waveforms with a skew, (b) change of VCO frequency to eliminate the skew.

$$\frac{d\phi_{out}}{dt} - \frac{d\phi_{in}}{dt} = 0 \qquad (15.1)$$

$$\omega_{out} = \omega_{in}. \qquad (15.2)$$

- The discussion suggests that the output phase of a VCO can be aligned with thephase of reference if
- 1) the frequency of the VCO is changed momentarily, and
- 2) a means of comparing the two phases, i.e. a phase detector, is used to determine when the VCO and reference signals are aligned.
- The task of aligning the output phase of the VCO with the phase of the reference is called ”phase locking”.
- Fig. 15.5 b): LPF added to remove high frequency components, to present only a DC level to the oscillator.
- Lock: $\Phi_{out} - \Phi_{in}$ is small, and $\Phi_{out} - \Phi_{in}$ does not change with time.

25

PLL Waveforms in locked condition

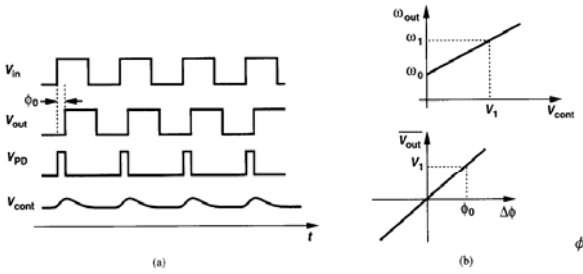


Figure 15.7 (a) Waveforms in a PLL in locked condition, (b) calculation of phase error.

$$V_1 = \frac{\omega_1 - \omega_0}{K_{VCO}}. \qquad (15.3)$$

$$\phi_0 = \frac{V_1}{K_{PD}} \qquad (15.4)$$

$$= \frac{\omega_1 - \omega_0}{K_{PD}K_{VCO}}. \qquad (15.5)$$

- The PLL is locked.
- LPF has a gain of 1 at low frequencies.
- The small pulses in V_{LPF} is called ”ripple”.
- Unknown quantities in Fig.15.7 a) Φ0 and V_{cont} . To fond these values the characteristics of the VCO and PD are constructed.
- Eq. 15.5 reveals 1) as the input frequency of the PLL varies, so does the phase error. 2) To minimize the phase error, $K_{PD}K_{VCO}$ must be maximized.

Equality of input and output frequencies is critical..

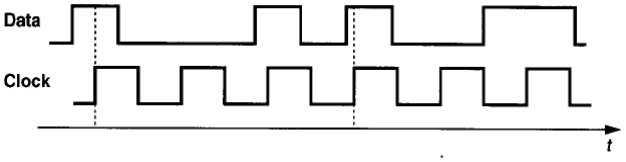


Figure 15.9 Drift of data with respect to clock in the presence of small frequency error.

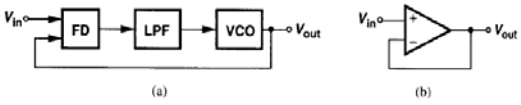


Figure 15.10 (a) Frequency-locked loop, (b) unity-gain feedback amplifier.

- Two observations: In many applications a small (deterministic) frequency error may prove unacceptable. For example , if a data stream is to be processed synchronously by a clocked system, even a slight difference between the data rate and clock frequency resuolts in a ”drift”, creating errors (Fig. 15.9).
- The equality would not exist if the PLL compared frequencies rather than phases; Fig 15.10: A loop employing a frequency detector (FD) would suffer from a finite difference between ω_{out} and ω_{in} due to various mismatches and nonidealities. This could be understood by an analogy with the unity-gain feedback circuit of Fig. 15.10 b). Even if the opamp's open loop gain is infinity, the input referred offset voltage leads to a finite errorbetween V_{in} and V_{out} .

27

Small transients in locked condition

$$V_{in}(t) = V_A \cos \omega_1 t \qquad (15.6)$$

$$V_{out}(t) = V_B \cos(\omega_1 t + \phi_0), \qquad (15.7)$$

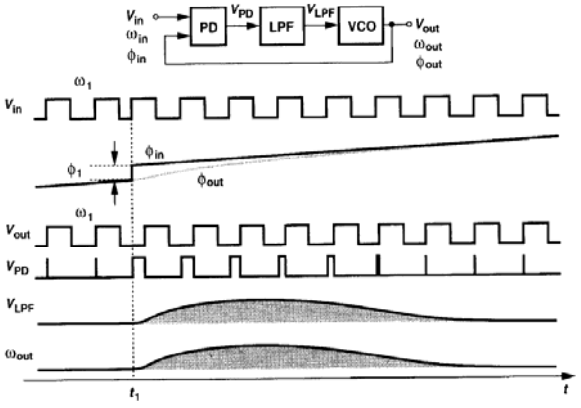
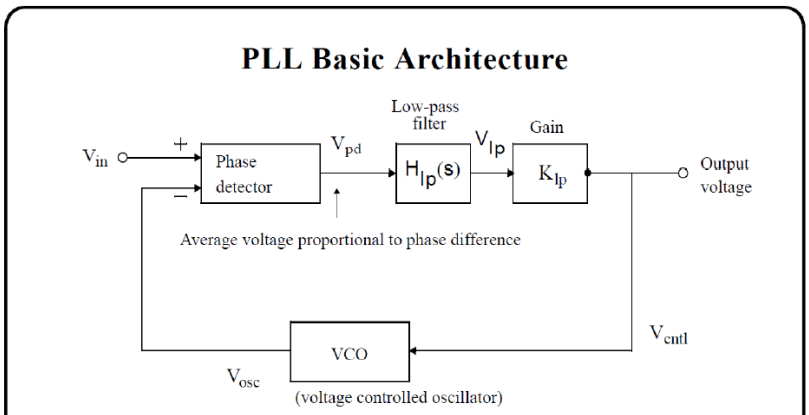


Figure 15.11 Response of a PLL to a phase step.

28



- In general, output may be V_{cntl} or V_{osc}

University of Toronto 3 of 26

29

Preliminary plan for next week..

- http://www.uio.no/studier/emner/matnat/ifi/INF4420/v11/undervisningsplan.xml
- More on PLLs (chapter 15 in ”Razavi”)
- Report writing and layout (ch. 18)

30