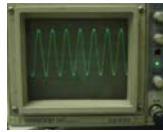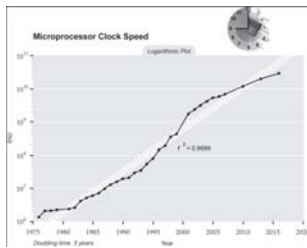# Phase Locked Loops, Report Writing, Layout

Tuesday, April 5th, 9:15 – 11:00

Snorre Aunet (sa@ifi.uio.no)
Nanoelectronics group
Department of Informatics
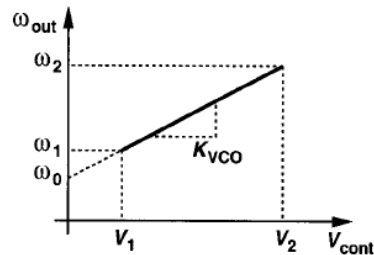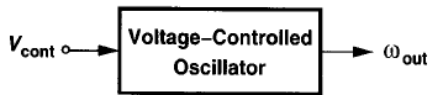University of Oslo

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Last time – and today, Tuesday 5th of April:
Oscillators
14.1 General considerations
14.2 Ring Oscillators
14.4 Voltage-Controlled Oscillators
14.5 Mathematical model of VCOs
Phase Locked Loops
15.1 Simple PLL

Today:
15.2 Charge Pump PLLs
Report Writing
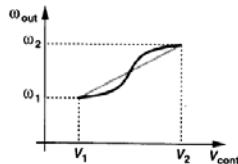ch. 18.1 and 18.2; Layout and Packaging

Voltage Controlled Oscillators

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont}.$$

$$K_{VCO} \geq \frac{\omega_2 - \omega_1}{V_2 - V_1}.$$

- Ideally linear function of the control voltage (Eq. 14.55)
- K_{VCO} : "gain"; rad / s / V
- Center frequency. Could be 10 GHz or higher
- The Tuning range, $\omega_2 - \omega_1$, is dictated by; 1) variation in VCO center frequency with PT (process and temperature), and 2) frequency range necessary for the application.
- Variation in output phase and frequency as a result of noise on the control line is important. To minimize the effect, the VCO gain must be minimized (in conflict with the tuning range)
- Tuning linearity
- Output amplitude, power dissipation, supply and CMRR, output signal purity

3

Basic PLL Topology – phase alignment through temporary frequency change

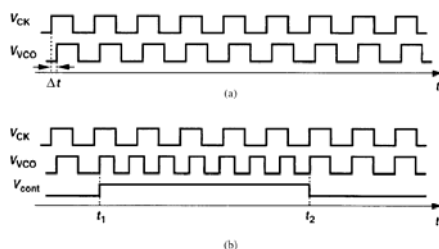Figure 15.5 (a) Feedback loop comparing input and output phases. (b) simple PLL.

Figure 15.4 (a) Two waveforms with a skew, (b) change of VCO frequency to eliminate the skew.

- Problem of aligning the output phase of the VCO with the phase of a reference clock.
- Fig. 15.4 a): The rising edges of V_{VCO} are "skewed" by Δt seconds with respect to V_{CK}, and we wish to eliminate this error.
- V_{cont} is the only control input to the VCO. To vary the phase, the frequency has to be varied. In Fig. 15.4 b) the frequency is stepped to a higher value at t_1. The circuit accumulates phase, gradually decreasing the phase error. At t = t_2 it drops to zero, and V_{cont} is returned to it's original value. V_{cont} and V_{CK} remain aligned.

4

PLL Waveforms in locked condition

$$V_1 = \frac{\omega_1 - \omega_0}{K_{VCO}}. \qquad (15.3)$$

$$\phi_0 = \frac{V_1}{K_{PD}} \qquad (15.4)$$

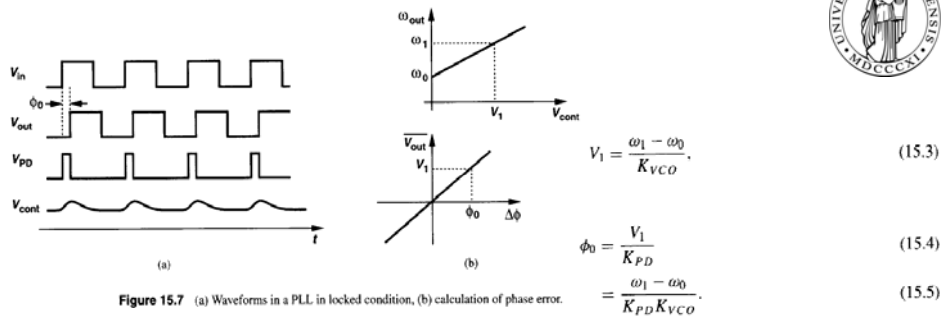$$= \frac{\omega_1 - \omega_0}{K_{PD}K_{VCO}}. \qquad (15.5)$$

Figure 15.7 (a) Waveforms in a PLL in locked condition, (b) calculation of phase error.

- The PLL is locked.
- LPF has a gain of 1 at low frequencies.
- The small pulses in V_{LPF} is called "ripple".
- Unknown quantities in Fig.15.7 a) Φ0 and V_{cont} . To fond these values the characteristics of the VCO and PD are constructed.
- Eq. 15.5 reveals 1) as the input frequency of the PLL varies, so does the phase error. 2) To minimize the phase error, $K_{PD}K_{VCO}$ must be maximized.

Small transients in locked condition

$$V_{in}(t) = V_A \cos \omega_1 t \qquad (15.6)$$

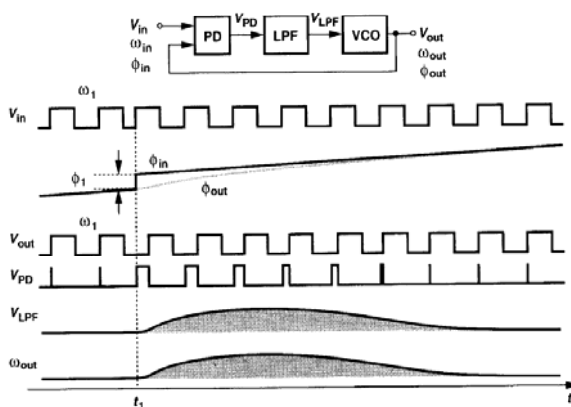$$V_{out}(t) = V_B \cos(\omega_1 t + \phi_0), \qquad (15.7)$$

Figure 15.11 Response of a PLL to a phase step.
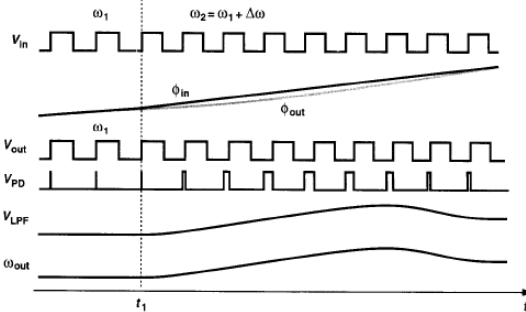
6

Response to frequency step, $\Delta\omega$

Figure 15.12 Response of a PLL to a small frequency step.

Figure 15.5 (a) Feedback loop comparing input and output phases. (b) simple PLL.

- Initially: VCO continues oscillating at freq. ω_1 .
- PD generates pulses of increasing width and V_{LPF} increases.
- When ω_{out} approaches $\omega+\Delta\omega$ the width of the pulses from the PD is becoming narrower, and end up on a value producing a dc-component equal to ($\omega_1 +\Delta\omega - \omega_0$)/K_{VCO} .
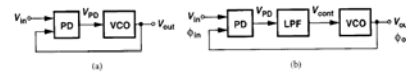
7

Both phase and frequency must settle to proper values

Figure 15.13 Example of phase step response.

Figure 15.5 (a) Feedback loop comparing input and output phases. (b) simple PLL.
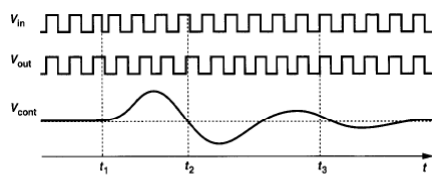
- V_{cont} rings before settling
- t_2: frequency is equal to final value, since V_{cont} is.
- t_3 : phase value equal to final, but frequency not.

8

4

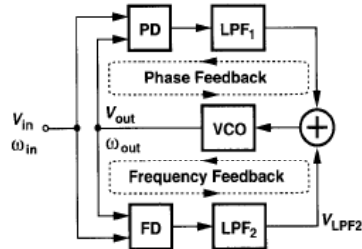PD for charge pump PLL with increased lock acquisition range

Figure 15.21 Addition of frequency detection to increase the acquisition range.

- Compare ω_{in} and ω_{out} by means of a frequency detector and generate a dc component V_{LPF2} proportional to the difference from the comparison. This dc component is added to the VCO input in a negative feedback loop. In the beginning the FD drives ω_{out} towards ω_{in} while the PD output remain "quiet". When $|\omega_{out} - \omega_{in}|$ is small enough, the phase locked loop takes over, and lock is acquired.
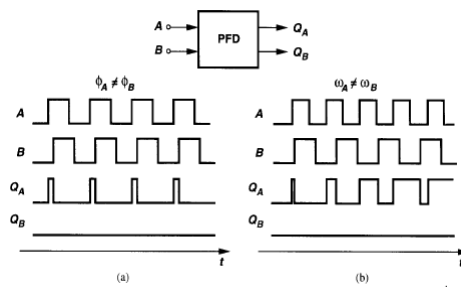
9

Phase Frequency Detector (PFD)

Figure 15.22 Conceptual operation of a PFD.

- 15.22 a) equal freq., but A leads B.
- 15.22 b) A has higher freq. Than B.
- DC contents provide information about $\Phi_A - \Phi_B$ or $\omega_A - \omega_B$.
- Q_A and Q_B : "UP" and "DOWN" pulses, respectively.

Merging the loops from Fig. 15.21, getting a circuit that can detect both phase and frequency (Fig. 15.22).

Three states detecting rising or falling edges; If Q_A = Q_B = 0, then a rising transition on A leads to Q_A = 1, Q_B = 0. The circuit remains in this state until B goes high, at which point Q_A returns to zero. (The behaviour is similar for the B input.)
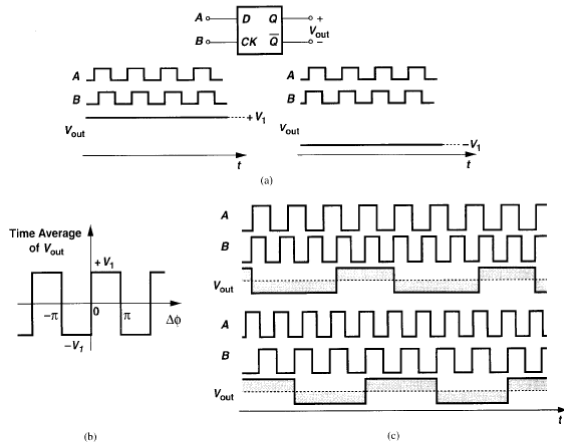
10

Unequal frequencies for A and B

Figure 15.23   (a) D flipflop as a phase detector, (b) input/output characteristic, (c) response of D flipflop to unequal input frequencies.

- Two cases:
- $\omega_A > \omega_B$
- and $\omega_A < \omega_B$
- Positive edge triggered, B on CK input

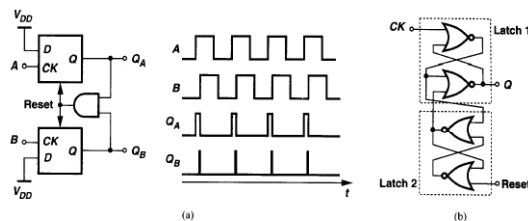# 1st Circuit realization of the PFD

Figure 15.24   (a) Implementation of PFD, (b) implementation of D flipflop.

- Two edge triggered resetable D-flip flops with their D inputs tied to logical 1.
- If $Q_A = Q_B = 0$ and A goes high, Q_A rises. If this event is followed by a raising transition on B, Q_B goes high and the AND gate resets both flip-flops.
- QA and QB are simultaneously high for a short ime but the difference between their outputs still represents phase of frequency difference correctly. (FF impl. In Fig. 15.24 b))
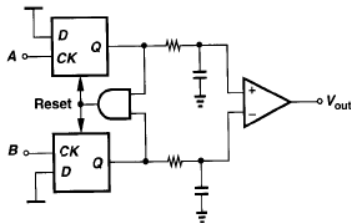
PFD implementation for PLL

Figure 15.27 PFD followed by low-pass filters.

- The difference between the two flip-flop outputs is of interest. They are low-pass filtered and sensed differentially in Fig. 15.27
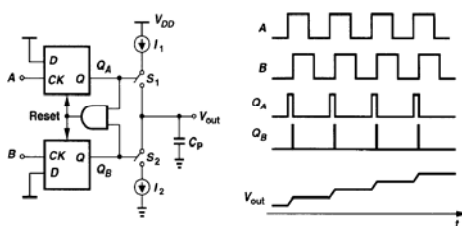- We'll see a more common approach

PFD with charge pump

Figure 15.28 PFD with charge pump.

- Charge pump containing two switches that pump charge into or out of the loop filter according to the logical inputs
- V_{out} may remain constant, or increase if I_1 ("UP current") charges C_p, or decrease, if I_2 ("DOWN current") discharge C_p.
- If for example A leads B, then Q_A produces pulses and V_{out} rises.
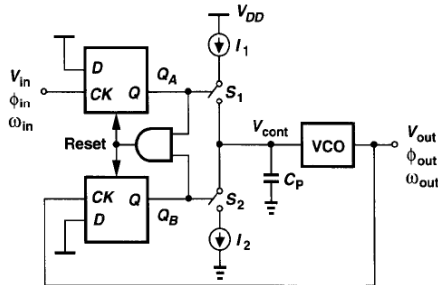
Basic Charge Pump PLL

Figure 15.30 Simple charge-pump PLL.

- Senses the transitions at the input and output, detects phase or frequency differences and activates the charge pump accordingly
- ω_{out} may be far from ω_{in} when the loop is turned on, and the charge pump vary the control voltage until the input and output frequencies are sufficiently close.
- When $Q_A = Q_B = 0$ that does not mean that the PFD and CP are no longer needed. Sooner or later the VCO frequency and phase begin to drift, particlularly due to noise sources in the VCO creating random variations in the oscillation frequency.
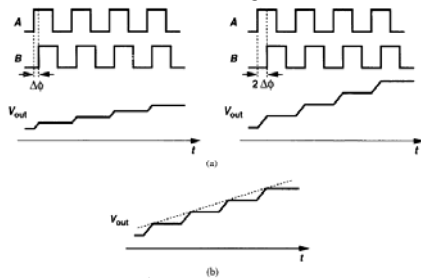
15

Dynamics of CPPLL

Figure 15.31 (a) Test of linearity of PFD/CP/LPF combination, (b) ramp approximation of the response.
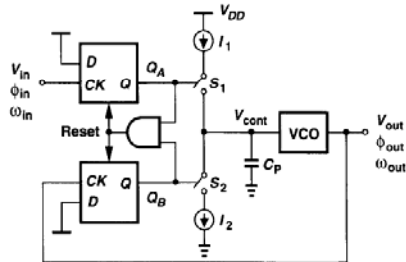

Figure 15.30 Simple charge-pump PLL.

- Dynamics of CPPLL
- Use ramp approximation to linear system, arriving at a linear relationship between V_{out} and Δ_{Φ} .
- The discrete-time system is approximated by a continous-time model.
- Want a transfer function..
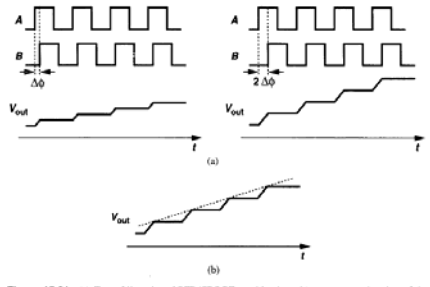
16

8

Dynamics of CPPLL

Figure 15.31 (a) Test of linearity of PFD/CP/LPF combination, (b) ramp approximation of the response.
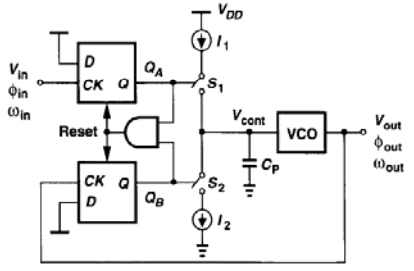
Figure 15.30 Simple charge-pump PLL.

compute V_{out} in the time domain. Since a phase difference impulse is difficult to visualize, we apply a phase difference step, obtain V_{out}, and differentiate the result with respect to time.

Let us assume the input period is T_{in} and the charge pump provides a current of $\pm I_P$ to the capacitor. As shown in Fig. 15.32, we begin with a zero phase difference and, at $t = 0$, step the phase of B by ϕ_0, i.e., $\Delta\phi = \phi_0 u(t)$. As a result, Q_A or Q_B continues to produce

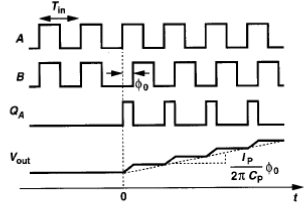Figure 15.32 Step response of PFD/CP/LPF combination.

pulses that are $\phi_0 T_{in}/(2\pi)$ seconds wide, raising the output voltage by $(I_P/C_P)\phi_0 T_{in}/(2\pi)$ in every period.[10] Approximated by a ramp, V_{out} thus exhibits a slope of $(I_P/C_P)\phi_0/(2\pi)$ and can be expressed as

$$V_{out}(t) = \frac{I_P}{2\pi C_P}t \cdot \phi_0 u(t).$$ (15.37)

The impulse response is therefore given by

$$h(t) = \frac{I_P}{2\pi C_P}u(t),$$ (15.38)

yielding the transfer function

$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_P}{2\pi C_P} \cdot \frac{1}{s},$$ (15.39)

Consequently, the PFD/CP/LPF combination contains a pole at the origin, a point of contrast to the PD/LPF circuit used in the type I PLL. In analogy with the expression K_{VCO}/s, we call $I_P/(2\pi C_P)$ the "gain" of the PFD and denote it by K_{PFD}.

Remember: Grading is based on the contents of the report

Some pointers

- http://www.idi.ntnu.no/~lasse/DM/SkriveTips.php
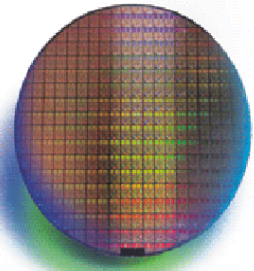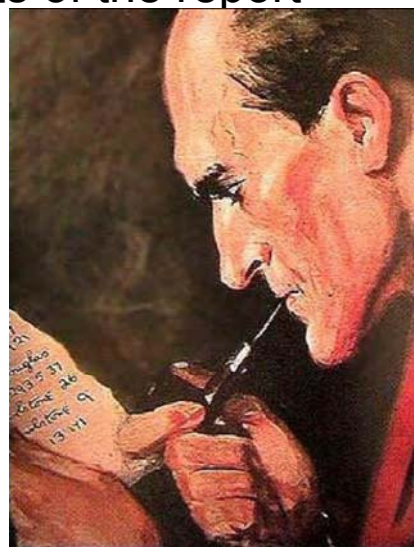
- **Preface**
- **(Acknowledgement)**
- **1 Introduction**
- **2 Theoretical background**
- **(2.1 Various approaches to Nifty Gadgets)**
- **2.2 Nifty Gadgets my way**
- **3 My implementation of a Nifty Gadget**
- **4 Nifty Gadget results**
  5 Discussion
- **6 References**

Nifty Gadget / DAC chapter 3

- **3 My implementation of a Nifty Gadget**
- Can you describe your implementation in detail?
  Why did you use this technology?
  How does the theory relate to your implementation?
  What are your underlying assumptions?
  What did you neglect and what simplifications have you made?
  What tools and methods did you use?
  Why use these tools and methods?

Nifty Gadget / DAC chapter 4

- **4 Nifty Gadget results**
- Did you actually build it?
  How can you test it?
  How did you test it?
  Why did you test it this way?
  Are the results satisfactory?
  Why should you (not) test it more?
  What compensations had to be made to interpret the results?
  Why did you succeed/fail?

Nifty Gadget / DAC chapter 5

- **5 Discussion**
- Are your results satisfactory?
  Can they be improved?
  Is there a need for improvement?
  Are other approaches worth trying out?
  Will some restriction be lifted?
  Will you save the world with your Nifty Gadget?

Guide to writing a thesis

Guide to Writing a Thesis

Department of Applied Electronics
Last updated 1997-03-12

Original manuscript written by Sven Mattisson

The Design and Implementation of a Nifty Gadget

Tekla-Liz Book

April 32, 1992

Abstract
What is all this about?
Why should I read this thesis?
Is it any good?
What's new?

Preface

Have you done anything that doesn't have to do with your research?
Have you published parts of this work before?

Acknowledgement

Who is your advisor?
Did anyone help you?
Who funded this work?
What's the name of your favorite pet?

1 Introduction

What is the use of a Nifty Gadget?
What is the problem?
How can it be solved?
What are the previous approaches?
What is your approach?
Why do it this way?
What are your results?
Why is this better?
Is this a new approach?
Why haven't anyone done it before?
or
Why do you reiterate previous work?
What is your contribution to the field of Nifty Gadgets?

2 Theoretical background

What is the required background knowledge?
Where can I find it?

2.1 Various approaches to Nifty Gadgets

What is the relevant prior work?
Where can I find it?
Why should it be done differently?
Has anyone attempted your approach previously?
Where is that work reported?

2.2 Nifty Gadgets my way

What is the outline of your way?
Have you published it before?

3 My implementation of a Nifty Gadget

Can you describe your implementation in detail?
Why did you use this technology?
How does the theory relate to your implementation?
What are your underlying assumptions?
What did you neglect and what simplifications have you made?
What tools and methods did you use?
Why use these tools and methods?

4 Nifty Gadget results

Did you actually build it?
How can you test it?
How did you test it?
Why did you test it this way?
Are the results satisfactory?
Why should you (not) test it more?
What compensation had to be made to interpret the results?
Why did you succeed/fail?

5 Discussion

Are your results satisfactory?
Can they be improved?
Is there a need for improvement?
Are other approaches worth trying out?
Will some restriction be lifted?
Will you save the world with your Nifty Gadget?

6 References

What is the background reading list?

Guide to writing a thesis

Where is the related work?
Where is the prior work?
Where can I find important material?

Appendix A

Can you outline fiddlary calculus or whatever complicated theory or results you are using that will obscure the text?

Appendix B

A thesis should discuss the following topics:

- **Introduction**

  Presentation of the problem or phenomenon to be addressed, the situation where the problem or phenomenon occurs, and references to earlier relevant research.

  Common errors
  Problem is not properly specified or formulated, insufficient references to earlier work.

- **Purpose**

  What can be gained by more knowledge about the problem or phenomenon.

  Common errors
  The purpose is not mentioned, not connected to earlier research, or not in line with what the actual contents of the thesis.

- **Problem/Hypothesis**

  Questions that need to be answered to reach the goal and/or hypothesis formulated be means of underlying theories.

  Common errors
  Missing problem description; deficiencies in the connections between questions; badly formulated hypothesis.

- **Method**

  Choice of an adequate method with respect to the purpose and problem/hypothesis.

  Common errors
  An inappropriate method is used, for example due to lack of knowledge about different methods; erroneous use of chosen method.

- **Result**

  Answers to the forwarded questions by means of the achieved results.

  Common errors
  The results are not properly connected to the problem; blurry presentation; the results are inter-

mixed with discussion.

- **Discussion**

  Discussion of the accuracy and relevance of the results; comparison with other researchers results.

  Common errors
  Too far reaching conclusions; guesswork not supported by the data; introduction of a new problem and a discussion around this.

- **Conclusion**

  Consequences of the achieved results, for example for new research, theory and applications.

  Common errors
  The conclusions are too far reaching with respect to the achieved results; the conclusions do not correspond with the purpose.

Home Page for the Department of Applied Electronics

Prosjektrapport

INF4420 - Prosjekter i analog/mixed-signal CMOS konstruksjon

Henrik Hagen og Mats Risopatron Knutsen
11.05.2009

Sammendrag

Prosjektet omhandler reduksjon av offset spenning til en OTA. Dette løses ved å benytte en digital kalibreringssløyfe som inneholder et suksessiv approksimasjonsregister (SAR), og en DAC. Offset korreksjonen foretas av en trimmekrets som trekker en strøm fra transistorene i inngangssteget til OTAen. Ytelsen til OTAen påvirkes minimalt av denne trimmekretsen. Trimmekretsen styres av DACen. Det har blitt laget et forslag til utlegg av M3M DAC og trimmekrets. Uten noen form for kalibrering har OTAen et standardavvik til offset spenningen på 7.1 mV. Med kalibreringssløyfen oppnår vi en reduksjon av standardavviket til 0.323 mV med ideell DAC, til 0.638 mV med M3M DAC og til 0.581 mV med ekstrahert layout av M3M DAC og trimmekrets. Med kalibreringssløyfen og egen layout av har standardavviket til offset spenningen til OTAen blitt redusert med nesten 92 %.
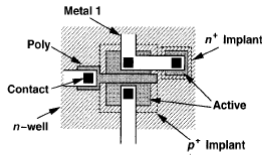
25

IMRaD structure

26

Layout Ch. 18

Figure 18.1 Layout of a PMOS transistor.

- Mimimum width
- Minimum spacing
- Minimum enclosure
- Minimum extension

- PMOS:
- 1) nwell must surround the device with enough margin to ensure that the transistor is contained in the well for all expected misalignments during fabrication.
- 2) each active area (S/D regions and n+ contact to the well) is surrounded by a proper implant geometry with enough margin.
- 3) from the fabrication steps in chapter 17 (read the necessary stuff on your own), the gate requires it's own mask.
- The contact windows mask provides connection from active and poly regions to the first layer of metal.

Layout (Ch. 18)

Figure 18.1 Layout of a PMOS transistor.
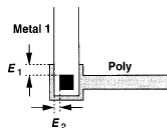
Figure 18.2 Excessive width variation in a narrow poly line.

Figure 18.5 Enclosure rule for poly and metal surrounding a contact.

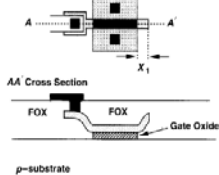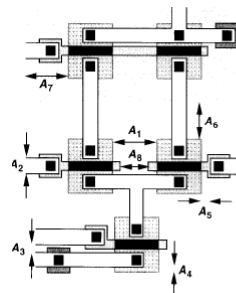Figure 18.6 Extension of poly beyond the gate area.

- Layout rules guaranteeing proper transistor and interconnect fabrication despite various tolerances in each step of processing
- Mimimum width, spacing, enclosure, extension

A_1: Active–Active Spacing
A_2: Metal Width
A_3: Metal–Metal Spacing
A_4: Enclosure of Contact by Active
A_5: Poly–Active Spacing
A_6: Active–Well Spacing
A_7: Enclosure of Active by Well
A_8: Poly–Poly Spacing

Figure 18.7 Layout of a differential pair with PMOS current-source loads.

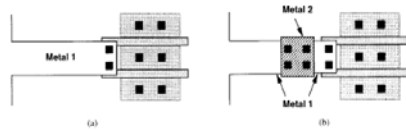# More layout techniques to maximize yield

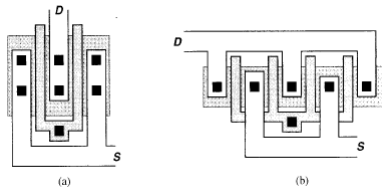Figure 18.8 (a) Layout susceptible to antenna effect. (b) discontinuity in metal 1 layer to avoid antenna effect.

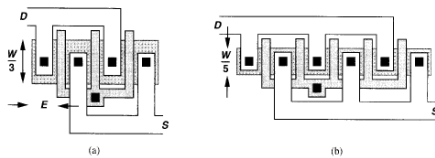Figure 18.9 (a) Simple folding of a MOSFET. (b) use of multiple fingers.

Figure 18.10 Layout of a transistor using (a) three fingers. (b) five fingers.

- **Antenna effect**: may occur for any large piece of conductive material tied to the gate, including polysilicon.
- During etching of metal 1 the metal area attracts ions and may rise in potential. It is possible that the increased gate voltage leads to irreversible oxide breakdown.
- Therefore the area for such geomteries must be limited.

- **Folded structures** using "fingers" to reduce the S/D area and the gate resistance.
- Increases perimeter S/D area cap.

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Simplified layout by letting sources share the same junctions
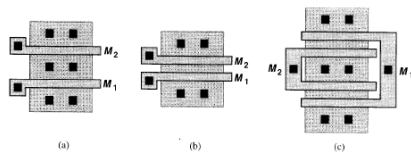

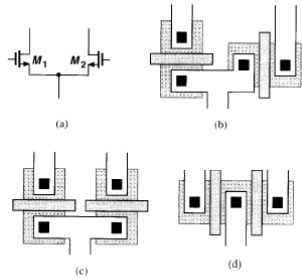Figure 18.12 Layout of cascode devices having the same width.

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Symmetry

Figure 18.13 (a) Differential pair, (b) layout of M_1 and M_2 with different orientations, (c) layout with gate-aligned devices, (d) layout with parallel-gate devices.
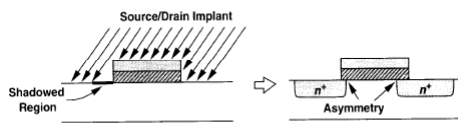
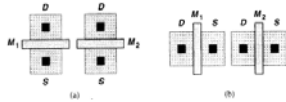Figure 18.14 Shadowing due to implant tilt.

Figure 18.15 Effect of shadowing on (a) gate-aligned and (b) parallel-gate transistors.

- Symmetry may reduce input referred offsets and enable detection of small signal levels.
- Symmetry may also suppress the effect of common-mode noise and even-order nonlinearity.
- Fig. 18.13 b) matching suffers greatly.
- Fig. 18.13 c) and d) better
- Fig. 18:15 a) preferable when having gate shadowing, as M1 and M2 sees more similar surroundings.
- The asymmetry in Fig. 18.15 b) can be improved by adding dummy structures.. (We'll see)

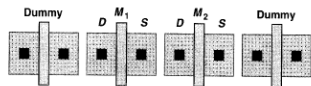# Dummy devices and removal of 1st order gradients

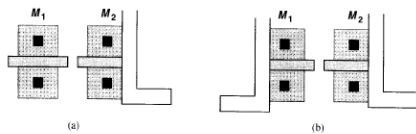Figure 18.16 Addition of dummy devices to improve symmetry.

Figure 18.17 (a) Asymmetry resulting from a metal line passing over M_2, (b) removing the asymmetry by replicating the line on top of M_1.
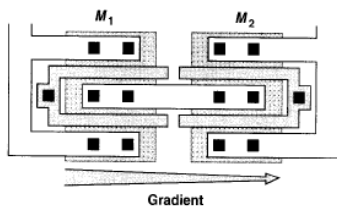
Figure 18.18 Effect of gradient in a differential pair.

Figure 18.19 Common-centroid layout.

- Fig. 18.19; Each transistor is decomposed into two halves that are plaed diagonally oposite of each other and connected in parallel. Routing may become complicated though.
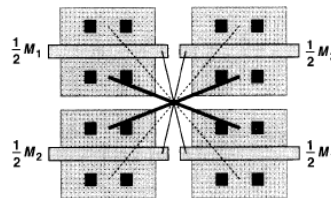
Suppressing linear gradients by "one-dimensional" cross coupling

Figure 18.18 Effect of gradient in a differential pair.
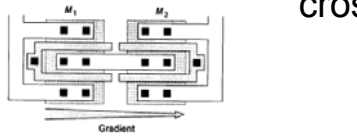
M_{1a} M_{2a} M_{3a} M_{4a}

C_{ox} $C_{ox}+\Delta C_{ox}$ $C_{ox}+2\Delta C_{ox}$ $C_{ox}+3\Delta C_{ox}$

(a)

M_{1b} M_{2b} M_{3b} M_{4b}

C_{ox} $C_{ox}+\Delta C_{ox}$ $C_{ox}+2\Delta C_{ox}$ $C_{ox}+3\Delta C_{ox}$
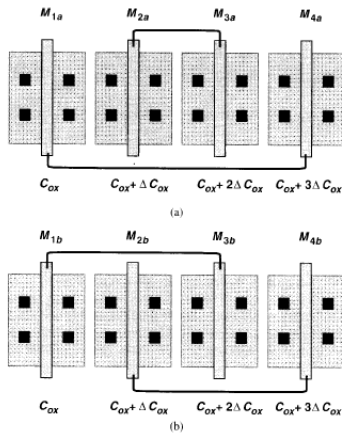
(b)

Figure 18.20 One-dimensional cross-coupling.

- Differential pair
- All four halv transistors are placed along the same axis and M1 and m2 are formed by connecting either the near ones or the far ones.
- The topology in a) is better than the one in b) and contains smaller errors (See pages 641-642 in "Razavi")

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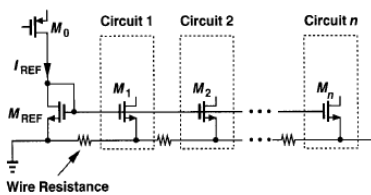# Distribution of current to reduce the effect of interconnect resistance

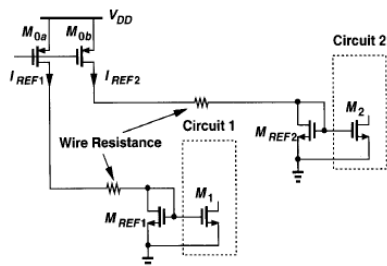Figure 18.21 Distribution of a reference voltage for current-mirror biasing.

Figure 18.22 Distribution of current to reduce the effect of interconnect resistance.

- Fig 18.21: I_{ref} is produced by a bandgap reference and M_1-M_n serve as bias current sources of building blocks that are located far from M_{ref} and far from each other. IR drops around the ground lines may lead to unnacceptable mismatch between current sources.
- Remedy: Distribute the reference in the current domain rather than the voltage domain.
- Fig. 18.22: Route the reference current to the vicinity of the building blocks and perform the current mirror operation locally.
- Large systems: Consider using local bandgap references to alleviate routing problems.

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Preliminary plan for next week..

- http://www.uio.no/studier/emner/matnat/ifi/INF4420/v11/undervisningsplan.xml
- More on layout (chapter 18 in "Razavi")
- Short Channel Effects and Device Models (ch. 17)

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