INF4420 / INF9425 -2011
”repetition” / about the final exam

Tuesday, May 31th, 9:15

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University of Oslo

Today

- A brief look at earlier exam problems
- Some practical information about the exam

Curriculum: Chapters from the three books

- ”Razavi”
- ”Maloberti”
- ”Johns & Martin”

- Detailed Curriculum will be put on the web later today.

2008

UNIVERSITY OF OSLO

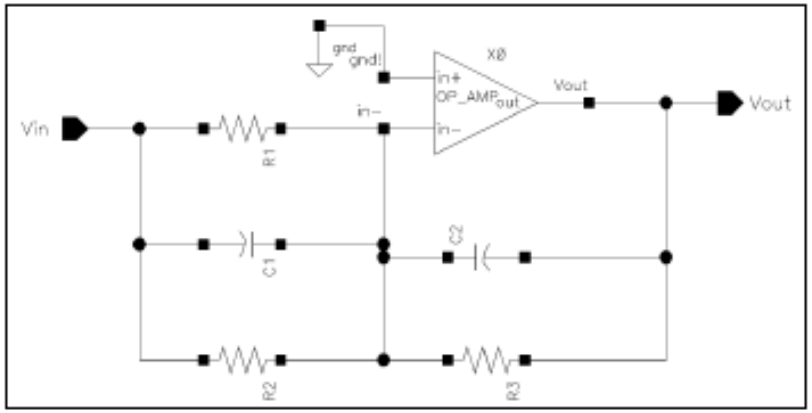
Faculty of Mathematics and Natural Sciences

Exam in: INF4420 Projects in Analog / Mixed Signal CMOS Construction.
Day of exam: Thursday, June the 5th, 2008.
Exam hours: 14:30 – 17:30.
This examination paper consists of 5 page(s).
Appendices: None.
Permitted materials: Any written material and calculator.

Make sure that your copy of this examination paper is complete before answering.

1 a) (Weight 10 %)

An active-RC filter is depicted below. Draw the schematics for a Switched Capacitor ("SC") equivalent. Simplify the schematics, if possible.



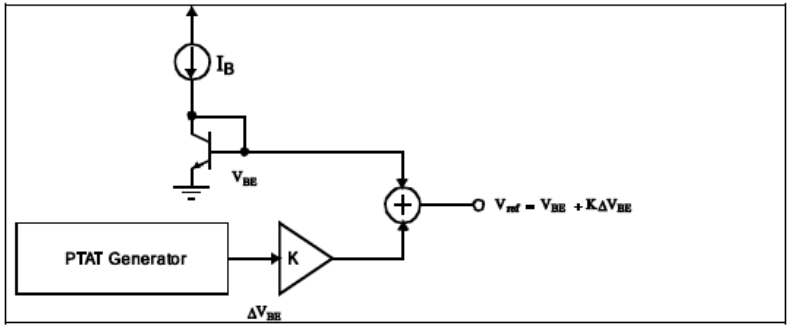
1 b) (Weight 10 %)

Find a transfer function, H(z) = Vout(z) / Vin(z), for the SC equivalent from problem 1 a).

2 a) (Weight 8 %)

A simplified circuit of a bandgap reference is shown below. Describe briefly which voltages that are generated on the base of the bipolar transistor shown, the output from the PTAT, the output from the

triangular block with "K" in it, and the output from the sum node. You may make a simple drawing to explain the concept. The figure depicts the same circuit as in figure 8.23 In the book by Johns & Martin.



2 b) (Weight 8 %)

Assume that a bandgap reference of the same type shall be used at a temperature of 300 Kelvin. The PTAT depends on two base-emitter junctions, where the two bipolar transistors have emitter areas differing by a factor of 8. Let $V_{BE0\text{-}2} = 0.65$ V, $\Delta V_{BE} = -2$ mV / degree Kelvin, $V_{G0} = 1.18$ V and m = 2.3. The following, fundamental relationship, holds:

$$V_{ref} = V_{BE2} + K\,\Delta V_{BE}$$
$$= V_{G0} + \frac{T}{T_0}(V_{BE0\text{-}2} - V_{G0}) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + K\frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right)$$

Calculate K, under the given conditions.

3 a) (Weight 10 %)

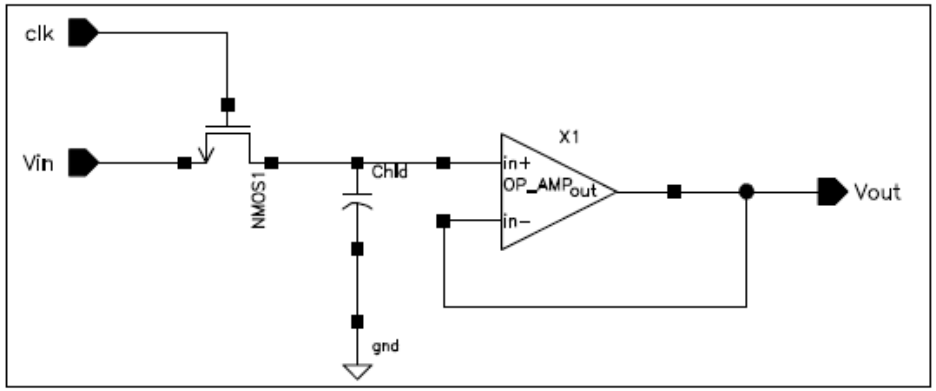
A sampled signal is bandlimited to $f_0 = 22$ kHz. What is the sampling frequency, f_s, for an oversampling ratio ("OSR") of 128?
A 1-bit analog-to-digital converter ("ADC") has an inherent 6-dB SNR. Which maximum SNR is acquired by combining it with strict oversampling and an OSR of 128, if no noise shaping is used? What is the maximum SNR in the similar case exploiting 2nd order noise shaping?
If a 1-bit ADC using 3rd order noise shaping has a maximum SNR of 125 dB for an OSR of 128, what is the expected maximum SNR if the OSR is reduced to 32?

3 b) (Weight 6 %)

Assume that a 1st order noise shaping modulator is considered for use in a battery driven hearing aid, being part of the sound processing signal path. Are you aware of any reasons for increasing the order of the modulator(s), instead?

4 a) (Weight 8 %)

A simple sample-and-hold ("S/H") circuit is shown in the schematics below. It is implemented in a standard 90 nm CMOS technology, having a supply voltage of 1.0 V. The clock signal ("clk") varies between 0 V and 1 V, while a sine wave varying between 0.3 V AND 0.5 V is connected to the input ("Vin"). Make a sketch depicting the two previously mentioned signals as well as the voltage across the hold capacitor ("Chld"), and the output ("Vout").



4 b) (Weight 12 %)

Consider the S/H from 4 a) and describe certain problems that may arise if Chld is made very small.

5 a) (Weight 6 %)

Assume that you are going to design an ADC (Analog-to-Digital Converter) for use in a sensor-node utilizing energy harvesting (containing no batteries), leading to a very strict budget with respect to average power consumption. This ADC should measure slowly changing physiological parameters for humans, needing a maximum resolution of 8 bits ("Effective Number of Bits" ; ENOB). What is most likely to be the best choice among a FLASH ADC or an integrating ADC? Please explain.

5 b) (Weight 6 %)

Sampling in the frequency domain, under two different basic conditions, is depicted below. Could the situation in the lower half of the picture represent a problem ($f_s/2$, f_s, and f is written along the horisontal lines.)? Please explain.

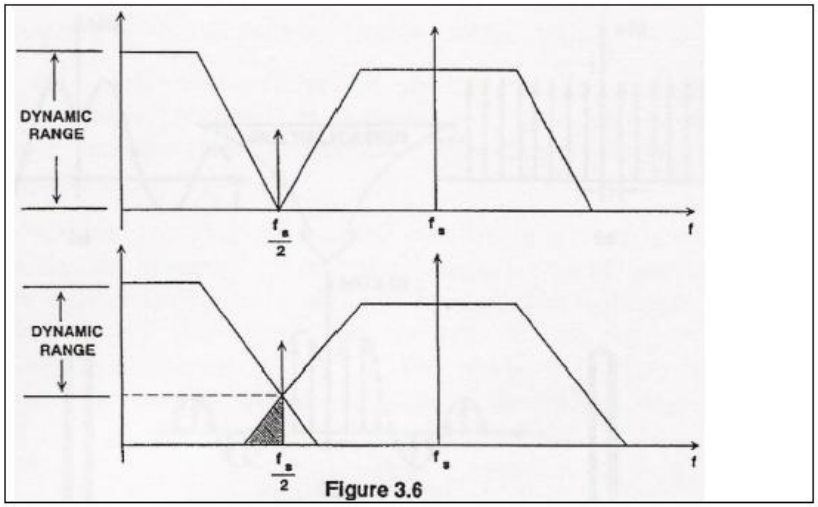
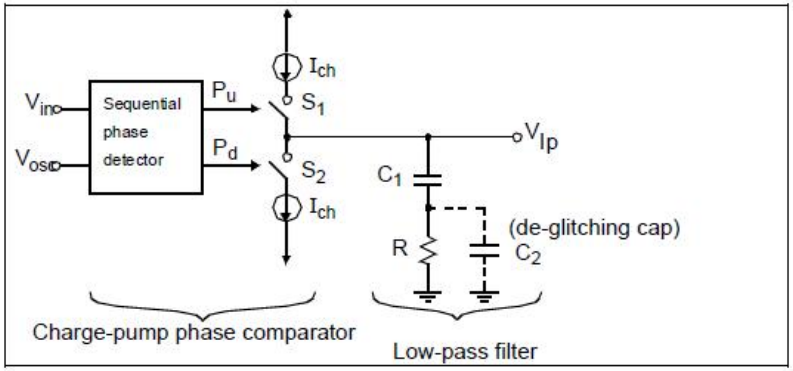


Figure 3.6

6 a) (Weight 8 %)

A ring oscillator consisting of inverters has it's supply voltage increased from 1.0 V to 1.2 V. What is the resulting expected increase in it's oscillating frequency?
Using fully differential inverters would improve the power supply rejection and lead to a more stable circuit. Can you imagine any negative effects of changing the simple inverter based ring oscillator for a differential solution?



6 b) (Weight 6 %)

How would you choose the Q-factor in a PLL (to obtain a maximally flat group delay) given that the architecture is a charge-pump PLL with a deglitching capacitor in the loop-filter, as shown above?
What is most likely the value of C_1 if the "de-glitching" capacitor, C_2, was choosen to be 1 pF?

Good luck!

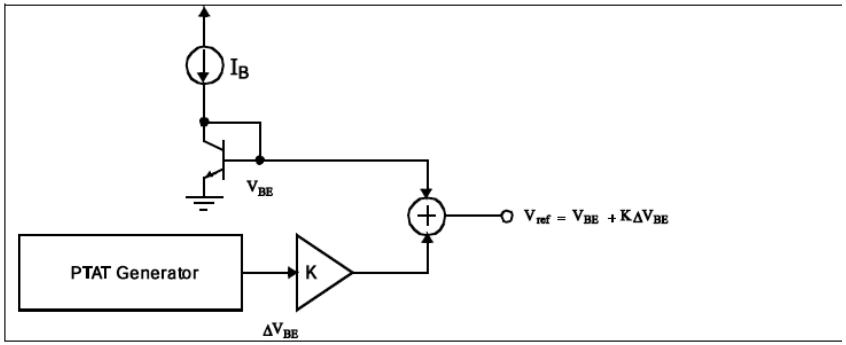
2009

UNIVERSITY OF OSLO

Faculty of Mathematics and Natural Sciences

Exam in: INF4420 Projects in Analog / Mixed Signal CMOS Construction.
Day of exam: Thursday, June the 4th, 2009.
Exam hours: 14:30 – 17:30.
This examination paper consists of 5 page(s).
Appendices: None.
Permitted materials: Any written material and calculator.

Make sure that your copy of this examination paper is complete before answering.



Problem 1 (Problem 1 has a weight of 6 % out of the total exam.)

1 a) (Weight 6 %)

We have a bandgap reference operating at 300 °K and a current-density ratio of X:1 for the two biased transistors in the PTAT generator. Assume that $V_{BE0\text{-}2}$ = 650 mV. Also assume that the value for K required to get zero temperature dependence at this temperature, under normal assumptions given in "Analog Integrated Circuit Design" (by Johns and Martin), is 10.41. Find X.
A bandgap reference is shown above, and the fundamental equation giving the relationship between the output voltage of a bandgap voltage reference and temperature is given by:

$$V_{ref} = V_{BE2} + K\,\Delta V_{BE}$$
$$= V_{G0} + \frac{T}{T_0}(V_{BE0\text{-}2} - V_{G0}) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + K\frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right)$$

Problem 2 (Problems 2 a) and b) have a weight of 12 % out of the total exam.)

2 a) (Weight 6 %)

Assume that we are Analog-to-Digital Converting signals of 8 bit resolution, for a wireless sensor node operating at an input signal from 0 – 10 Hz, monitoring biological parameters in mammals. What is the maximum sampling time uncertainty?

2 b) (Weight 6 %)

If you should choose an ADC ("Analog-to-Digital Converter") to convert such a signal, which architecture would you most likely pick if you could choose either an *oversampling and noise shaping ADC* or a *pipelined ADC*? Please explain.

Problem 3 (Problems 3 a), b), c), d) and e) have a weight of 30 % out of the total exam.)

3 a) (Weight 6 %)

Se(f) is assumed to be the spectral density of the quantization noise, when the quantizer is modeled as in chapter 14.1, in our book by Johns & Martin, and the sampling frequency is f_s. Can you explain what could happen to the dynamic range if a sampling frequency of $f_s/2$ was chosen instead? Illustrate in a figure with similarities to the one below, if you like.

3 b) (Weight 6 %)

Suppose that an ideal 7th order Delta-Sigma modulator provides a SNR of 118 dB at a certain sampling rate, f_s. What would happen to the SNR if one halved the peak-to-peak input signal range and at the same time the OSR is halved?

3 c) (Weight 6 %)

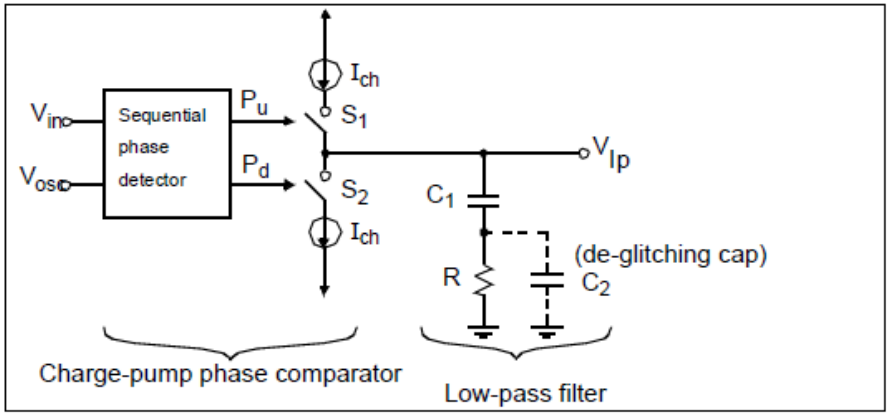
Given an oversampled and noise shaped data converter using a 1-bit quantizer and having SNRmax = 82.5 dB. Quantify the potential improvement in performance if the 1-bit quantizer is replaced by a 3-bit quantizer.

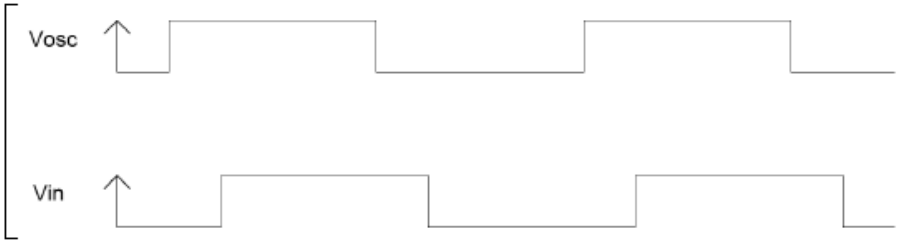
3 d) (Weight 6 %)

Assuming that the data converter is a DAC, could you mention any disadvantages due to increasing the number of output levels, given that the oversampling rate is unchanged?

3 e) (Weight 6 %)

If the converter from problem 3 c) uses 2nd order noise shaping, what is the minimum oversampling ratio (OSR)?





Problem 4 (Problems 4 a) and b) have a weight of 12 % out of the total exam.)

4 a) (Weight 6 %)

A *charge-pump phase comparator* for integrated PLLs is shown above. There is also an example of two waveforms related to it, V_{osc} and V_{in}. Draw the related P_u and P_d waveforms and explain briefly how they relate to V_{in} and V_{osc}.

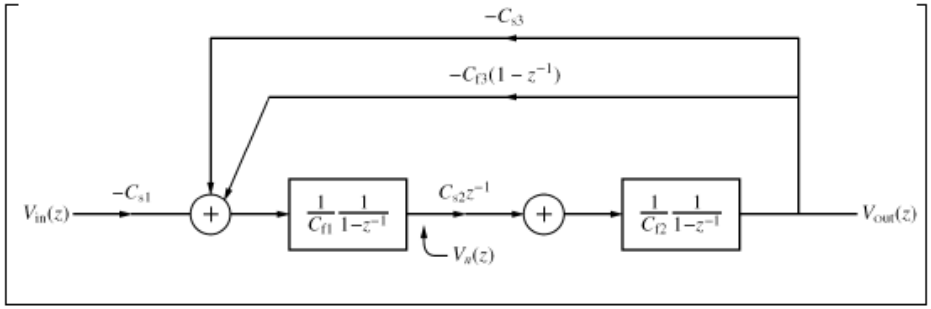
4 b) (Weight 6 %)

CMOS technology still continue toward finer scale geometries. Do you think that this development could make any influence on the choice of PLL architectures? Could you explain why and how?

Problem 5 (Problems 5 a), b), c) and d) have a weight of 40 % out of the total exam.)

5 a) (Weight 10 %)

The figure below depicts a signal flow graph ("SFG"), for a switched-capacitor circuit. Note that $V_a(z)$ is just a node in the circuit that might be useful when later determining H(z). Draw an equivalent switched capacitor realization of this SFG.



5 b) (Weight 12 %)

Derive the transfer function, H(z) = Vout(z) / Vin(z), from the SFG shown above, and show that it can be written as:

$$H(z) = -\frac{az}{bz^2 + cz + d}$$

$$a = C_{s1}C_{s2}$$
$$b = C_{f1}C_{f2}$$
$$c = C_{s2}C_{s3} + C_{f3}C_{s2} - 2C_{f1}C_{f2}$$
$$d = C_{f1}C_{f2} - C_{f3}C_{s2}$$

5 c) (Weight 8 %)

With capacitor values $C_{s1} = C_{s2} = C_{s3} = 1$ pF, $C_{f1} = C_{f2} = 1.987$ pF, and $C_{f3} = 2.325$ pF, what is the gain (magnitude response) at DC and at 0.2π?

5 d) (Weight 10 %)

Suppose all capacitors are scaled by 0.01. Does this affect the magnitude response? List advantages from such scaling as well as potential problems in an integrated circuit implementation.

Good luck!

2010

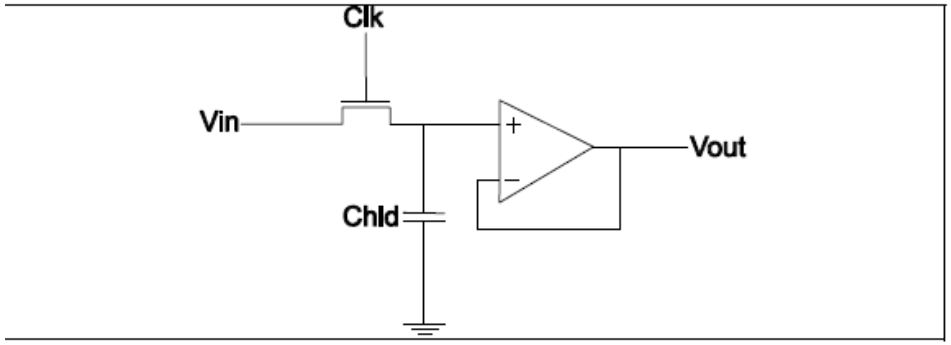
UNIVERSITETET I OSLO

Det matematisk-naturvitenskapelige fakultet

Eksamen i: INF4420 – Prosjekter i analog/mixed-signal CMOS Konstruksjon.
Eksamensdag: Torsdag 3. juni 2010.
Tid for eksamen: 14:30 – 17:30.
Oppgavesettet er på 4 sider.
Vedlegg: Ingen.
Tillatte hjelpemidler: Alle trykte og skrevne hjelpemidler samt kalkulator.

Kontroller at oppgavesettet er komplett
før du begynner å besvare spørsmålene.

Oppgave 1 (Oppgave 1 utgjør totalt 20 % av oppgavesettet.)

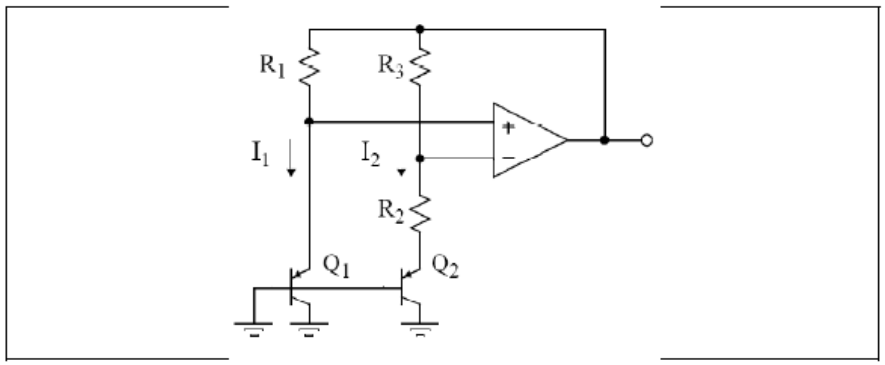


1 a) (vekt 7 %)

En Sample-and-Hold krets er vist i skjema ovenfor. Anta at C_{OX} = 1.92 fF/(μm)^2, V_{tn} = 0.5 V, og W/L = 2μm / 0.5 μm, supply-spenningene +/- 2.5 V og inngangssignalet svinger mellom maksimum 0.5 V og minimum -0.5 V. Hva må være minimum størrelse på kondensatoren for at absoluttverdien av samplingsfeil pga ladningsinjeksjon ikke skal overstige 5 mV?

1 b) (vekt 7 %)

En båndgapsreferanse er vist i figuren under, hvor følgende er gitt: $V_{EB1\text{-}0}$ = 0.65 V, T = 300 K, I_1 = 100 μA, ΔV_{EB} = 59 mV, J_1 / J_2 = 10. Finn verdiene på R1, R_2 og R_3.



1 c) (vekt 6%)

Med utgangspunkt i oppgave 1 a), hva blir verdien for K? Gjør relevante forutsetninger med utgangspunkt i læreboken ("Johns & Martin").

Oppgave 2 (Oppgave 2 teller totalt 24 % av oppgavesettet)

2 a) (vekt 6%)

Vi forutsetter følgende sammenheng for en SC-krets med inngangsspenning u_1, utgangsspenning u_2 og kapasitansene C_1 og C_2 :

$C_2u_2[nT] = C_2u_2[(n-1)T] - C_1u_1[(n-1)T]$

Signal på inngangen, u1, blir samplet vha ideell NMOS switch ved t = (n-1)T. Klokkesignalet til nevnte switch er lavt ved T = nT.
Benytt z-transformen og sett opp en overføringsfunksjon for kretsen, i z-planet.

2 b) (vekt 12 %)

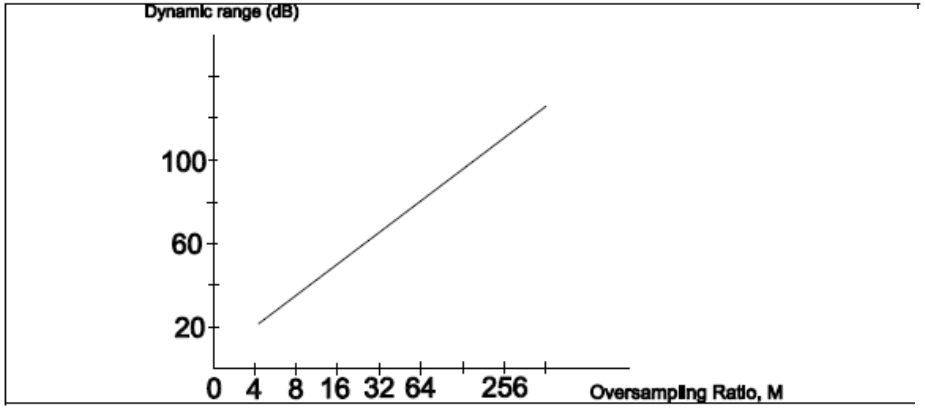
Gitt en SC-implementasjon med følgende overføringsfunksjon:

$H(z) = U_2(z) / U_1(z) = (-C_1/C_2)(1/z-1)$

Tegn skjema for en SC-implementasjon av H(z), samt en tilsvarende aktiv RC-filter implementasjon.

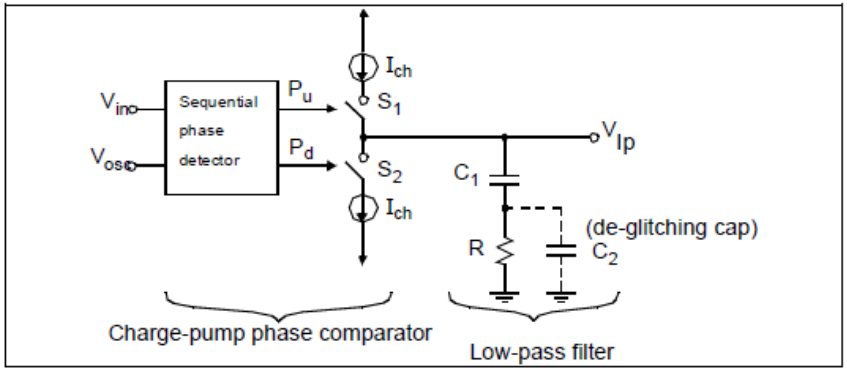
2 c) (Vekt 6 %)

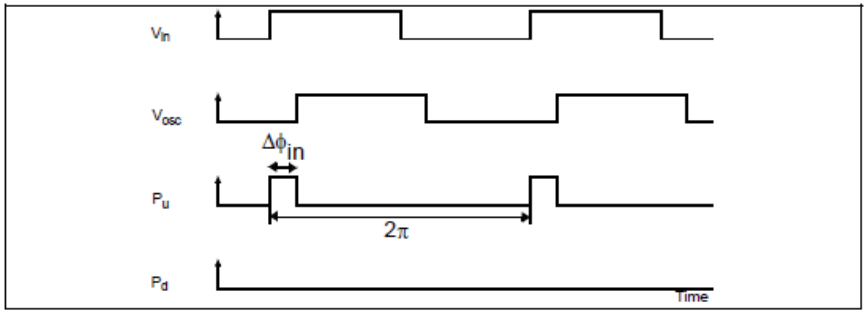
Anta at figuren under illustrerer sammenhengen mellom dynamisk område og oversamplingsgsrate for en oversamplende datakonverter. Hvilken orden, N, har sannsynligvis den datakonverteren som hører til figuren? N er et heltall. Begrunn svaret ditt.



Oppgave 3 (Oppgave 3 teller totalt 28 % av oppgavesettet.)

Figuren under viser skjema for en ladnings-pumpe fase-komparator (*"charge pump phase comparator"*). Deretter er det vist noen typiske signalforløp for fase-komparatoren.





3 a) (vekt 10%)

Ta utgangspunkt i kombinasjonen av nevnte skjema og signalforløp, og forklar hva som foregår i fase-komparatoren, basert på denne informasjonen.

3 b) (vekt 9 %)

Det antas at loop'en har en tidskonstant på 2 μs, eller 100 sykler. K_{osc} = 2π x 50 Mrad/s, free-running frekvensen til oscillatoren er 50 MHz, og I_{ch} = 10 μA. Anta C_2 = 0. Anta at maksimalt flat gruppe-forsinkelse er ønskelig. Bestem størrelsen på komponentene i lavpass-filteret.

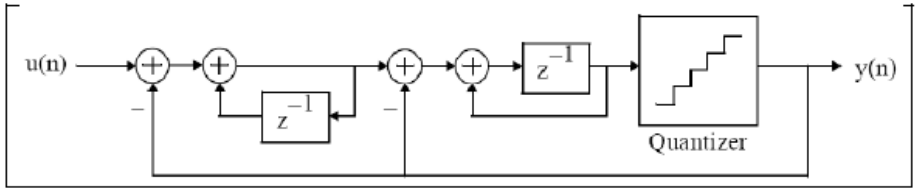
3 c) (vekt 9 %)

Dersom man forutsetter et annet tilfelle, der tiden $\Delta\phi_{in}$, er 0.1 μs, I_{ch} = 1 μA og C_2 = 0. Hvor mye ville spenningen over C_1 maksimalt ha forandret seg i løpet av tiden $\Delta\phi_{in}$ dersom C_1 hadde kapasitansen 2 nF?

Oppgave 4 (Oppgave 4 teller totalt 28 % av oppgavesettet.)

4 a) (vekt 10 %)

Figuren beskriver en ΔΣ modulator. Vis hvordan du kommer fram til et uttrykk for P_e ("quantization noise power") for denne kretstopologien, basert på formelen under og relevante forutsetninger fra læreboken av Johns & Martin.



$$P_e = \int_{-f_0}^{f_0} S_e^2(f)\left|N_{TF}(f)\right|^2 df$$

4 b) (vekt 10 %)

Vis hvordan du kan finne et uttrykk for SNR_{max}, basert på a) og $P_s = (\Delta^2 2^{2N}) / 8$. Forklar hva som normalt skjer med SNR_{max} når oversamplingsraten dobles, i dette tilfellet? Begrunn svaret.

4 c) (vekt 8 %)

Et matematisk uttrykk for SNR_{max} for en oversamplende konverter gir ingen øvre grense for oversamplingsraten ("OSR"). Vil en praktisk implementasjon i CMOS teknologi kunne ha en øvre grense for OSR? Begrunn svaret ditt.

Lykke til!

Included in the curriculum for INF4420:

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-
- From *Design of Analog CMOS Integrated Circuits*, by Behzad Razavi:
- Chapter 11, Bandgap References
- Chapter 12, Introduction to Switched Capacitor Circuits (minus ch. 1.2.5)
- Chapter 13, Nonlinearity and mismatch
- Chapter 14, Oscillators (minus ch. 14.3)
- Chapter 15, Phase Locked Loops (minus ch. 15.3 and 15.4)
- Chapter 16, Short-Channel Effects and Device Models
- Chapter 17, CMOS processing technology
- Chapter 18, Layout and packaging
- From *Analog Integrated Circuit Design*, by David A. Johns and Ken Martin:
- Chapter 14, Oversampling converters
- From *Data Converters*, by Franco Maloberti
- Chapter 1, Background elements
- Chapter 2, Data Converter Specifications
- Chapter 3, Nyquist Rate D/A Converters
- Chapter 4, Nyquist Rate A/D Converters
- Lecture Notes

Keep yourself updated regarding the time and place via the web

- **Eksamensplan og eksamensdager**
- Informasjon om tid og sted for eksamen publiseres for hver enkelt emnebeskrivelse på nettet. Den finnes ved å klikke på ”VÅR 2011”, og deretter under overskriften ”Eksamen og vurderingsformer” → ”Tid og sted”.
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- Information about the time and place for exams is published for every single description of subjects on the web. Click ”VÅR 2011” (= SPRING 2011) and then ”Eksamen og vurderingsformer” → ”Tid og sted”.

SA will visit 0.5-1 hour after the beginning of the exam, and (at least) once later.

- Emneansvarlige bør være tilgjengelige i eksamenslokalet innen 1 time etter at eksamen har startet. Ved eksamener med mange kandidater bør flere lærere gå runden i lokalene hvis det er nødvendig for å rekke alle kandidatene innen rimelig tid. Instruksen for lærere i eksamenslokalet er som følger:
-
- Instituttet utpeker én ansvarlig lærer som går rundt i eksamenslokalet ½ - 1 time etter at eksamen har begynt. Hvis forholdene tilsier det, kan det utpekes flere lærere.
- Overinspektør i eksamenslokalet kunngjør at ansvarlig lærer er til stede i eksamenslokalet.
- Læreren skal henvende seg til hver enkelt kandidat for å bringe på det rene om det er spørsmål.
- Læreren kan besvare spørsmål av språklig og typografisk art. Spørsmål av faglig art som har å gjøre med løsningen av oppgaven å gjøre, skal ikke besvares. Spørsmål som kan tilskrives manglende faglig forståelse hos kandidaten, besvares heller ikke.
- Hvis læreren oppdager feil eller uklarheter i teksten av en slik art at dette angår besvarelsen av oppgaven eller av andre grunner bør meddeles alle kandidatene, skal dette ikke skje ved å gå rundt til hver enkelt kandidat, men meddelelsen skal skje muntlig eller skriftlig til samtlige kandidater. Læreren avgjør meddelelsesformen. Vesentlige trykkfeilrettinger eller vesentlige nødvendige endringer i oppgaveteksten skal meddeles kandidatene skriftlig.
- Dersom læreren mener at eksamenstiden bør forlenges som kompensasjon for bortkastet tid ved feil i oppgaveteksten, skal dette avgjøres i samråd med fakultetsadministrasjonen.
- Læreren skal gi overinspektøren i eksamenslokalet beskjed om hvor han/hun kan treffes (oppgi telefonnummer)
- En student som mener at feil eller uklarheter i oppgaven vil få vesentlig betydning for karakteren, kan søke fakultetet om å få arrangert ny eksamen. Klagen rettes skriftlig til fakultetsadministrasjonen senest 3 uker etter eksamen.

Even if you can not make a perfect answer write at least something reasonably sane, to score some extra points.

Given that you have little time..

- Remember that you can bring any written material with you at the exam.

- Lecture Notes
- Books (”Razavi”, ”Maloberti”, chapter from ”Johns and Martin”
- Material from problem solving classes

Good luck!!

- Results should be handed in by the teachers, in cooperation with sensors, by June the 28th. (deadline).