Q.1 question 3 of 2008 exam

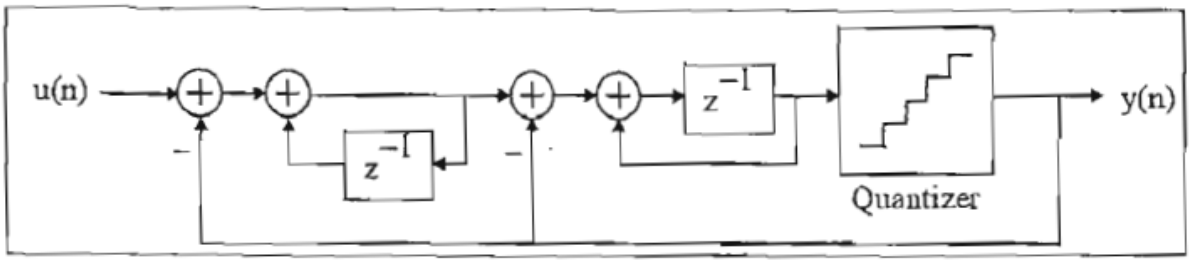
a) A sampled signal is bandlimited to f_0 = 22 kHz.What is the sampling frequency, f_s, for an oversampling ratio ("OSR") of 128? A 1-bit analog-to-digital converter ("ADC") has an inherent 6-dB SNR. Which maximum SNR is acquired by combining it with strict oversampling and an OSR of 128, if no noise shaping is used? What is the maximum SNR in the similar case exploiting 2nd order noise shaping? If a 1-bit ADC using 3rd order noise shaping has a maximum SNR of 125 dB for an OSR of 128, what is the expected maximum SNR if the OSR is reduced to 32?

b) Assume that a 1st order noise shaping modulator is considered for use in a battery driven hearing aid, being part of the sound processing signal path. Are you aware of any reasons for increasing the order of the modulator(s), instead?

Q.2 question 4 of 2010 exam

4 a) (weight 10 %)

Below you find a description of a ΔΣ modulator. Show how you can develop an expression for P_e (quantization noise power) for this topology, based on the formula below, ond relevant assumptions from "Johns & Martin".



$$P_e = \int_{f_0}^{f_0} S_e^2(f)\left|N_{TF}(f)\right|^2 df$$

4 b) (weight 8 %)

Show how you may develop an expression for SNR_{max}, based on a) and $P_s = (\Delta^2 2^{2N}) / 8$. Explain what normally happens to a SNR_{max} when the oversampling rate is doubled, in this case? Explain.

4 c) (weight 8 %)

Our mathematical expression for SNR_{max} for this oversampling converter does not provide an upper limit for the sampling rate ("OSR"). How would this be for a practical implementation in CMOS? Explain.

Q.3 14.14 of J&K

Show the block diagram for a MASH architecture that realizes third-order noise shaping using a second-order modulator as shown in Q.2 and a first-order modulator.