Q1. 8.7 of J&K's

Derive the output voltage of the S/H of Fig. 8.19 at the end of ϕ_2 in terms of the input voltage at the end of ϕ_1, the output voltage at the end of ϕ_1 from the previous period, and the capacitor ratio C_1/C_2. Take the z-transform of this difference equation, and substitute $z = e^{j\omega T}$ to find the frequency-domain transfer function of the S/H. Making the assumption that $e^{j\omega T} \equiv 1 + j\omega T$ for $\omega << (1/T) = f_{clk}$, where f_{clk} is the sampling frequency, show that

$$f_{-3\,dB} \cong \frac{1}{2\pi}\frac{C_1}{C_2} f_{clk}$$

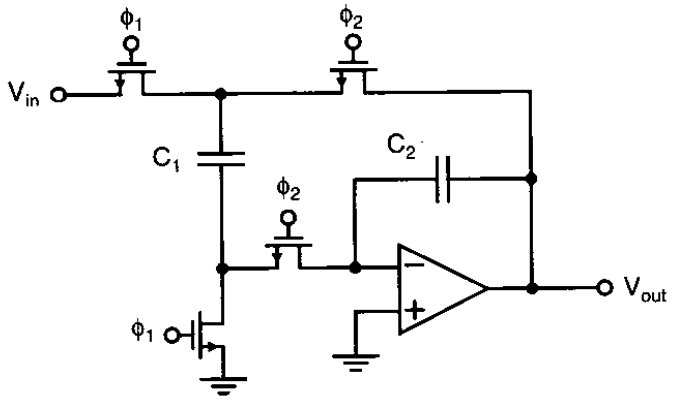

Fig. 8.19 A switched-capacitor sample and hold and low-pass filter.

Q2. 9.8 of J&K's

Sketch the magnitude response (in dB) of the following transfer function, $H(z)$, by finding the gains at dc and at $\omega = \pi$, as well as the location of the 3-dB frequency.

$$H(z) = \frac{0.05z}{z - 0.95}$$

Q.3 11.12 of J&K's

What sampling-time uncertainty (jitter) can be tolerated for a 16-bit ADC operating on an input signal from 0–20 kHz.