Q.1 (Example 12.1 of J&Ks')

Show that an estimate of the time constant for a network of n resistors, each of size R in series, with capacitive loading C at each node, is given by $\tau = RC\cdot(n^2/2)$. How much settling time is required for the output to settle to 0.1 percent of its final value.

Hints: Use zero-value time constant technique and assume a dominating pole exists.

The dominant-pole approximation is useful when a dominant pole exists. In some circuits, it may not be the case and zero-value time-constant analysis is used to estimate the **worst-case** –3dB frequency.

The procedure to find out the –3dB frequency of a given circuit is listed below:

1. Identity important capacitors and neglect all small capacitors. If not possible, consider all capacitors.
2. For each identified capacitor C_i, calculate the equivalent resistance R_i **seen by** C_i by
   - Shorting all independent voltage sources
   - Opening all independent current sources
   - Setting all other capacitors to zero (i.e. circuit-opening all other capacitors)
3. Calculate individual time constant τ_i contributed by each capacitor C_i using $\tau_i = R_i C_i$.
4. Approximate the –3dB bandwidth by

$$\omega_{-3dB} = \frac{1}{\sum R_i C_i}$$

Copy from HKUST ELEC304 Lecture notes 2003 by Alex Leung.

Q.2 (12.8 of J&Ks')

Consider an 4-bit DAC built using binary-weighted capacitors (shown in Fig. 1), where capacitor tolerances are ±0.5 percent. What would be the worst-case differential nonlinearity in units of LSBs, and at what transition does it occur?

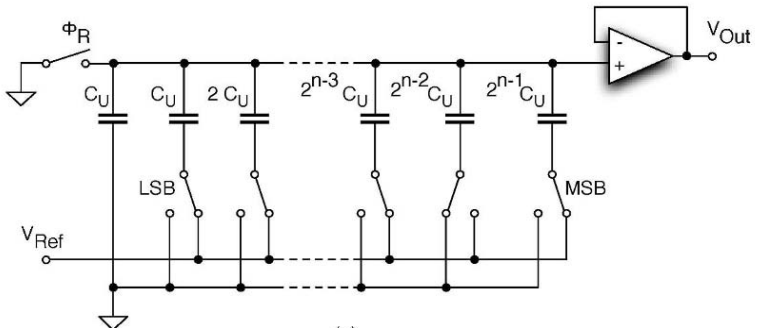
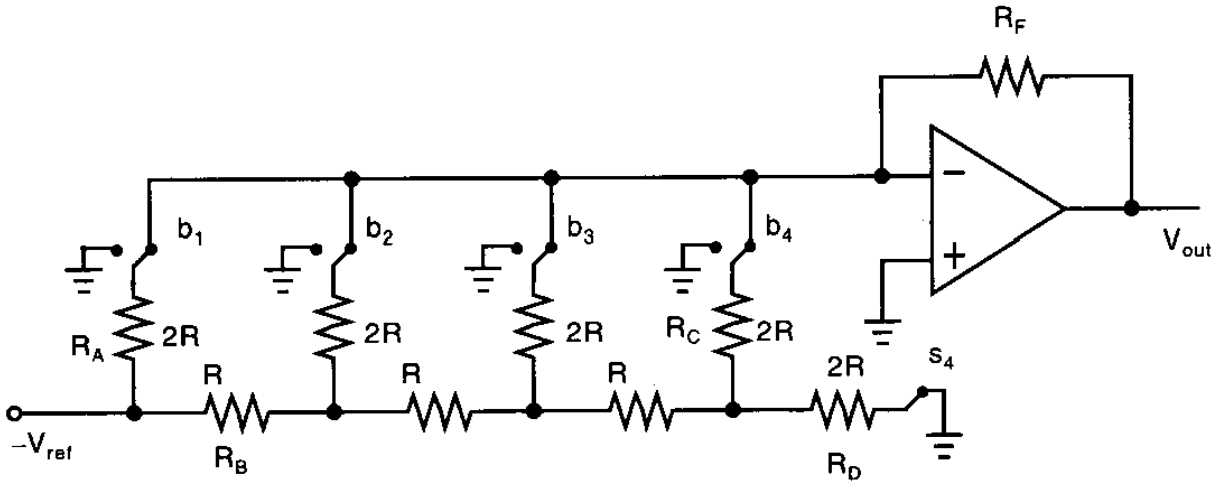


Fig. 1 (Fig. 3.28a in Maloberti's book)

Q.2 (12.8 of J&Ks')

For the 4-b R-2R DAC shown below, what is the output error (in LSBs) when $R_A = 2.01\ R_B$? What is the output error when $R_C = 2.01R$?


R_F
b_1
b_2
b_3
b_4
V_{out}
R_A
2R
2R
2R
R_C
2R
2R
s_4
R
R
R
$-V_{ref}$
R_B
R_D