MOS - TRANSISTOR AS SWITCH

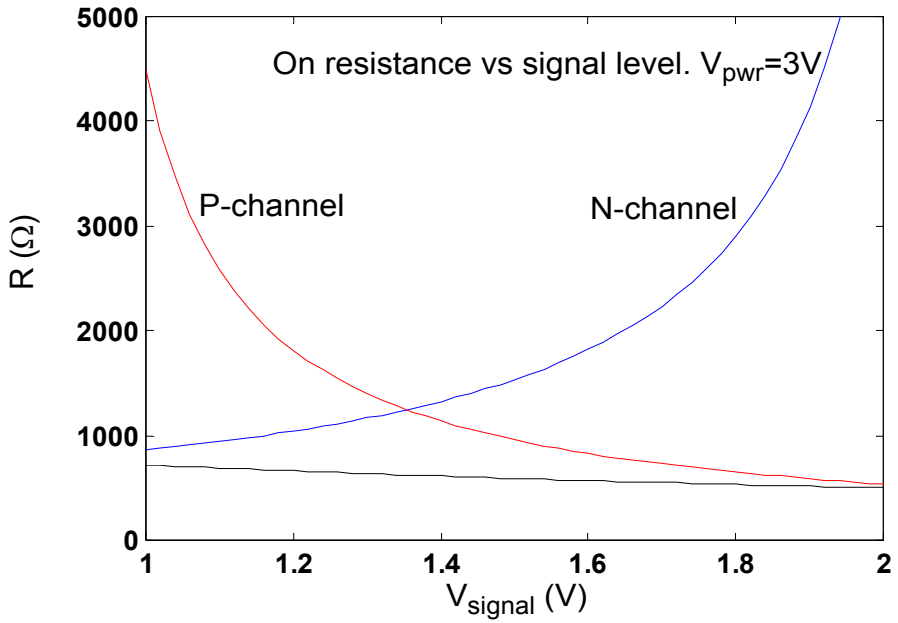
MOS-transistor as switch:

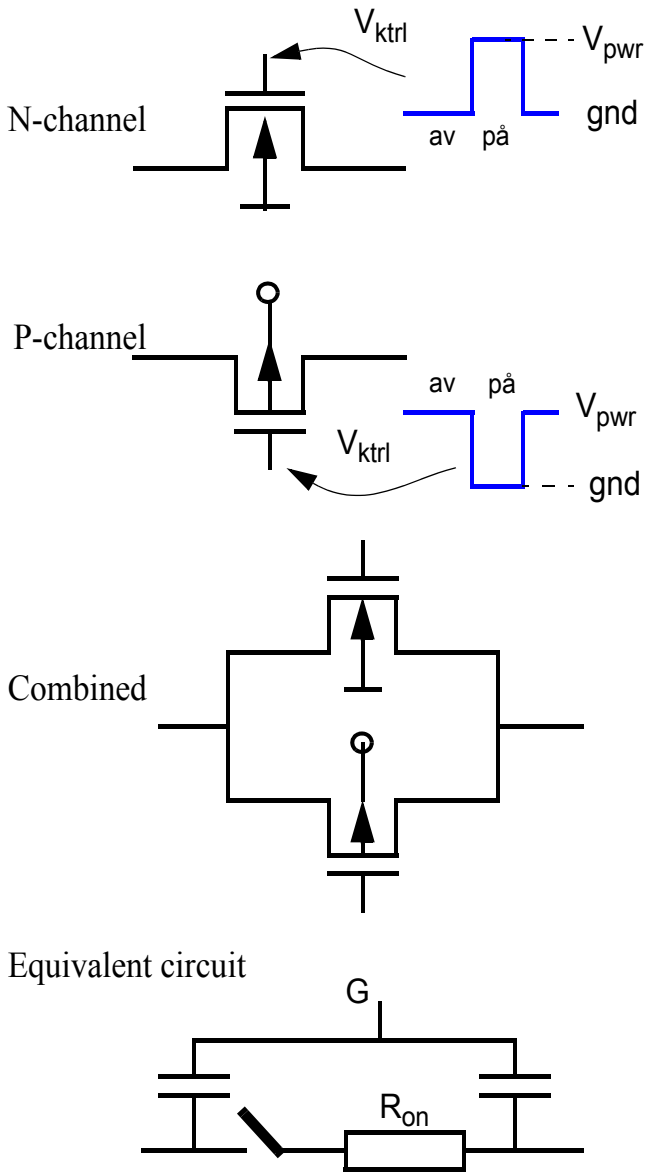
Off resistance:
In the range 0.1-10 GΩ
(Depends on technology and channel length).

On resistance:
Applying the expression for Drain current when the transistor operates in the linear region:

$$R_{on} = \frac{1}{g_d} = \frac{1}{\mu C_{ox}\frac{W}{L}[V_{gs} - V_T - V_{ds}]} \qquad (3.1)$$

Where $V_T = V_{T0} + \gamma(\sqrt{|2\Phi_F| + V_{sb}} - \sqrt{|2\Phi_F|})$

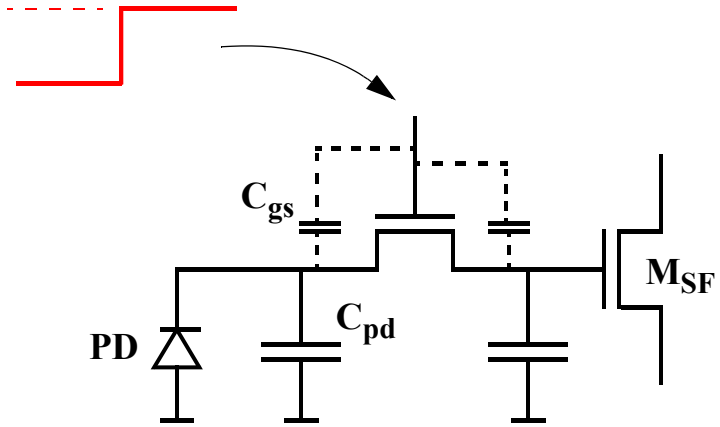




Clock Feed Through

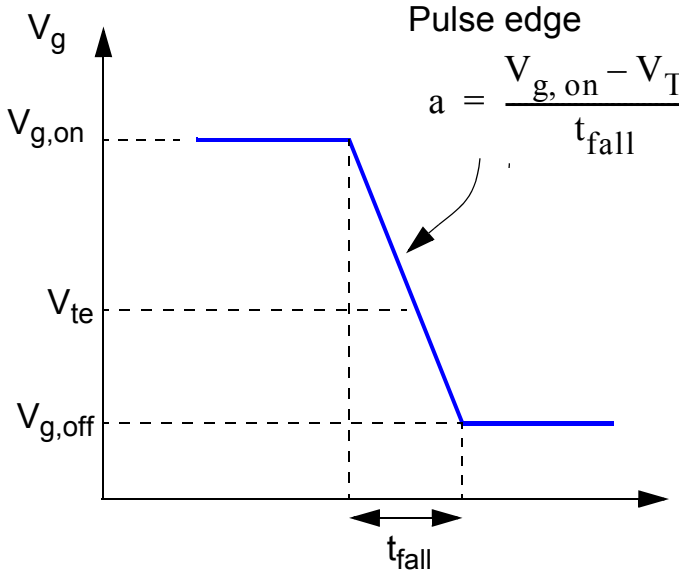
The control signal is coupled to the photo diode via a capacitive voltage divider:

$$v_{pd} = v_{sign} \frac{C_{gs}}{C_{gs} + C_{pd}} \qquad (3.2)$$



Charge injection in Source and Drain

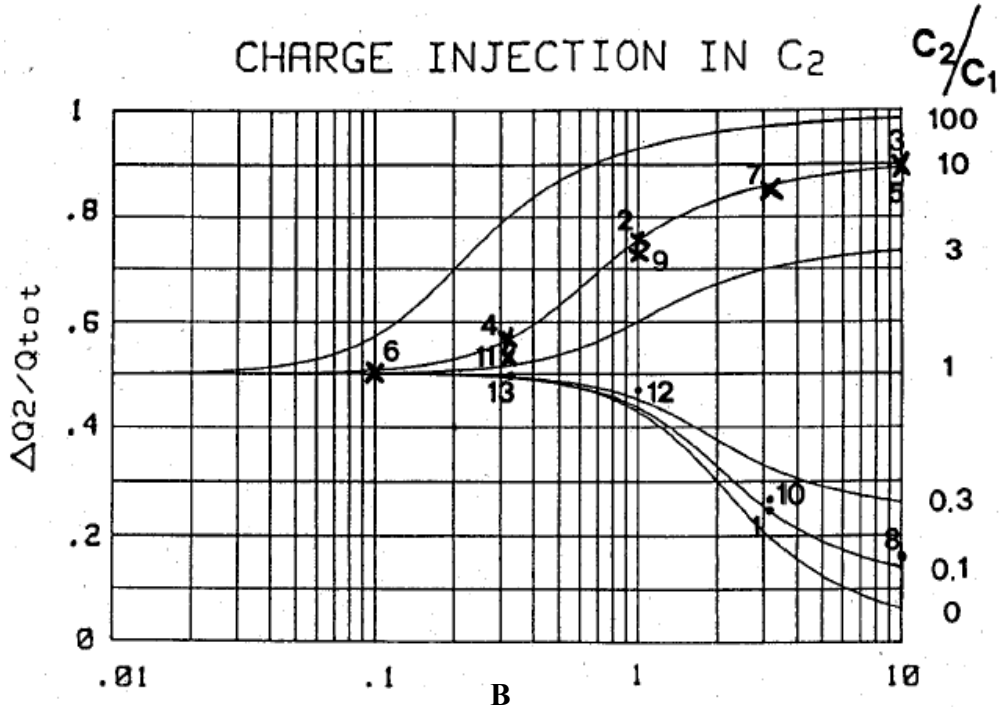
Extracts form:
Charge Injection in Analog MOS Switches
George Wegmann, Eric A. Vittoz and Fouad Rahali.
IEEE JSSC, vol. sc-22, no. 6, Dec 1987

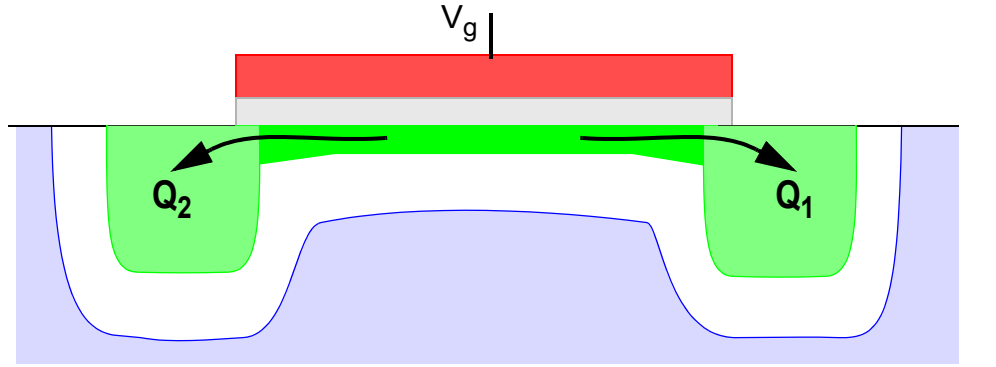


B expresses the normalized Transistor length related to mobility and time:

$$B = (V_{g,on} - V_{TE})\sqrt{\frac{\beta}{aC_2}}$$

$$\beta = \frac{W}{L}\mu C_{ox}$$

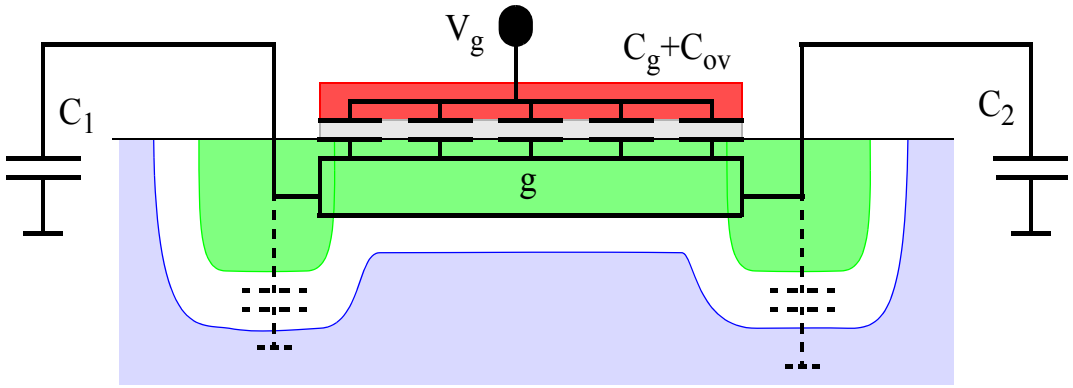




Ref.: Wegmann

Effective threshold voltage (Wegmann):

$$V_{TE} = V_{T0} + \left(1 + \frac{\gamma}{\sqrt{\Phi_F}}\right) V_{in}$$

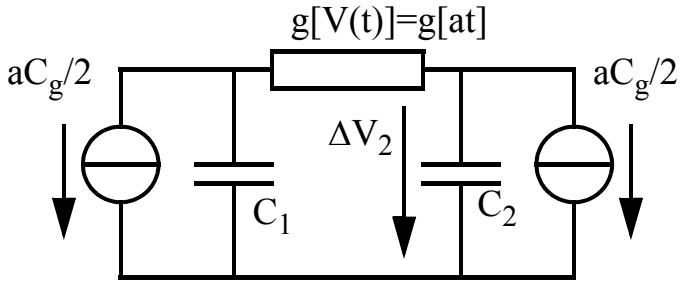


Conditions:

$$t_{fall} \gg T_{transit}$$
$$C_1, C_2 \gg G_g$$

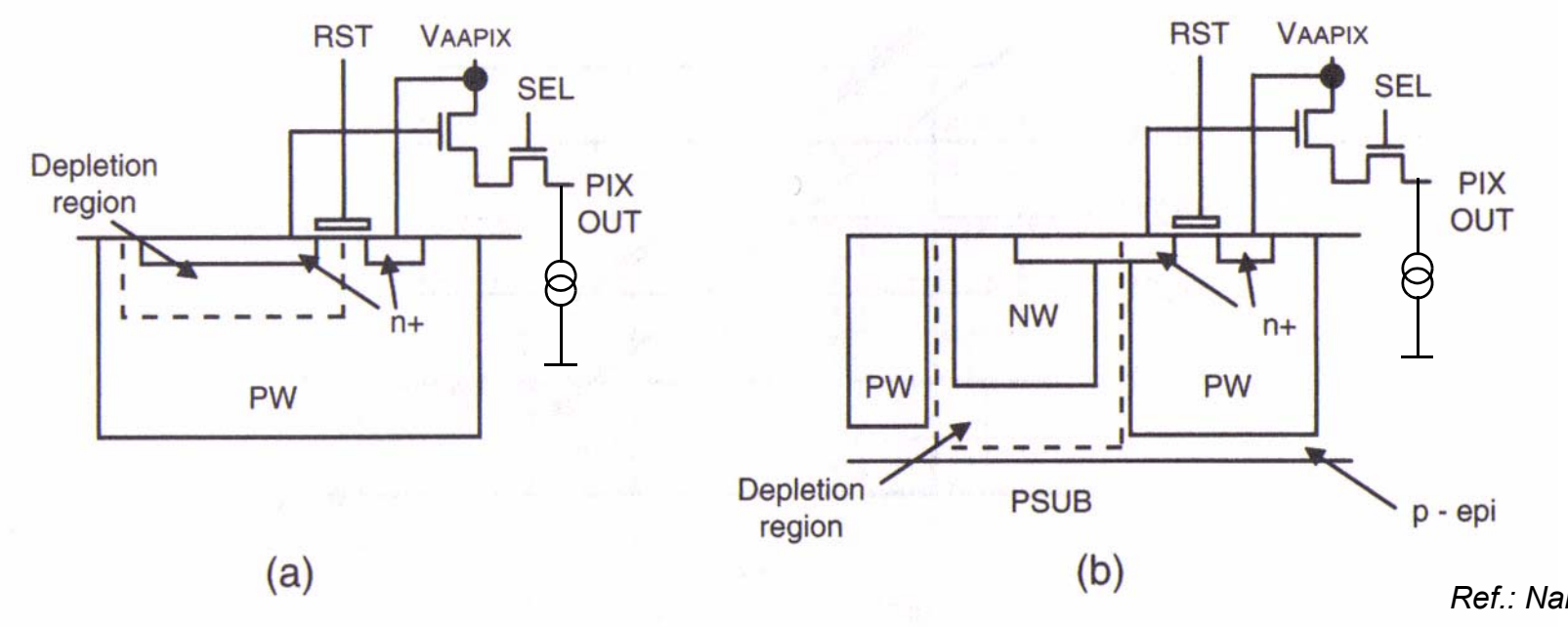
Consider the channel as a voltage controlled conductance:

$$g[V_g(t)] = \beta(V_g(t) - V_{TE})$$
$$= \beta(V_{g,\,on} - at - V_{TE})$$

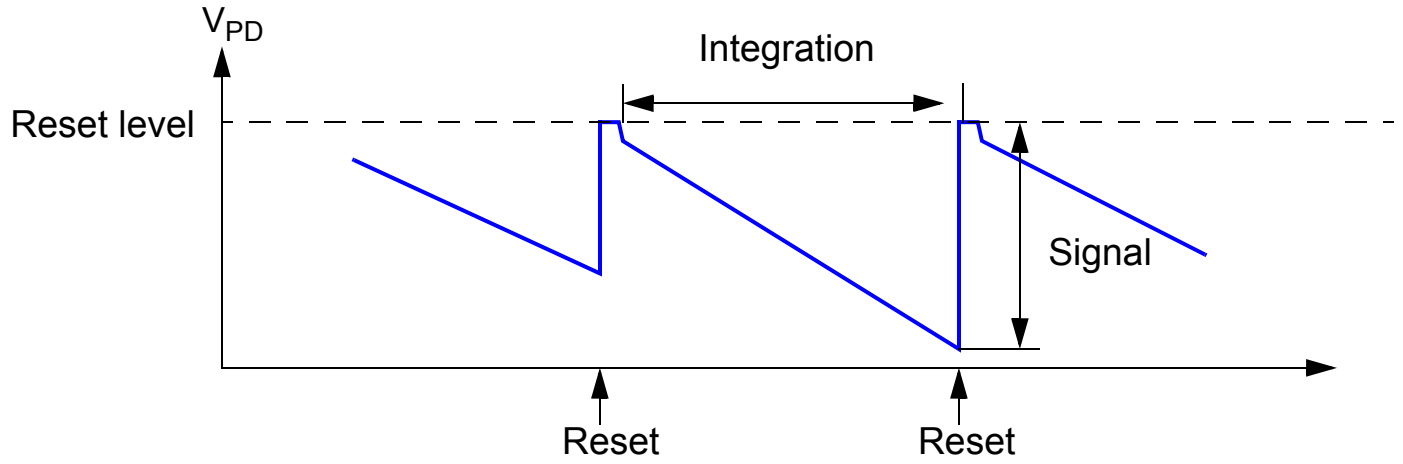


PIXEL READ OUT

3T - pixel



Ref.: Nakamura



Soft reset

The N-channel transistor does not completely reset the diode to V_{aa}.

Current in a saturated transistor:

$$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}[V_{gs} - V_T]^2 \qquad (3.3)$$

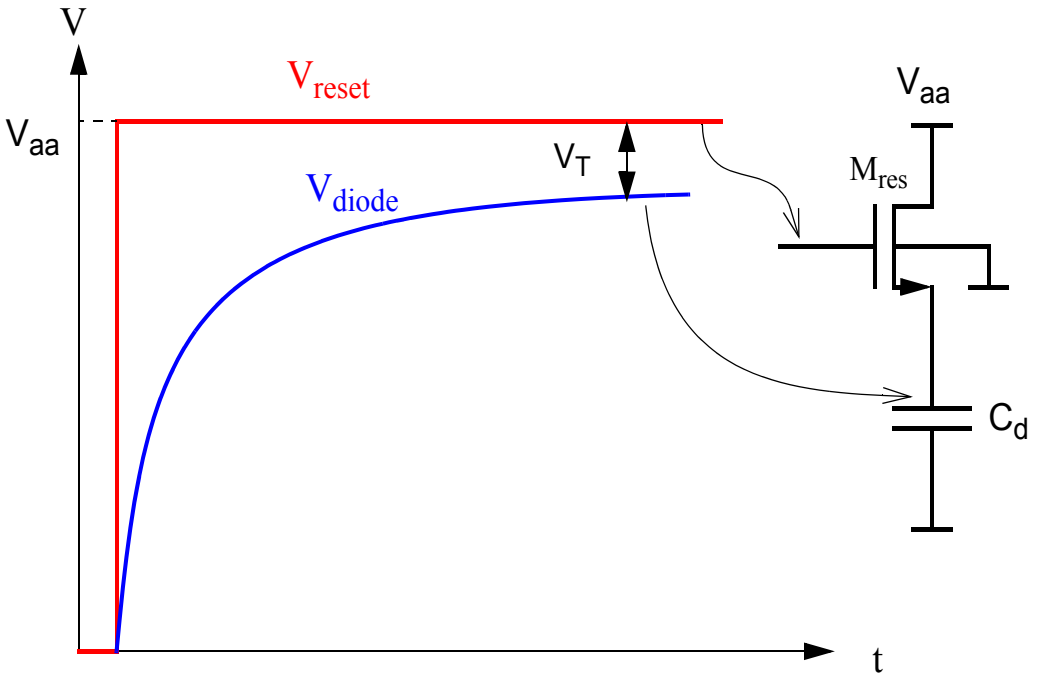
The transistor threshold voltage increases with the voltage across the diode due to the body effect:

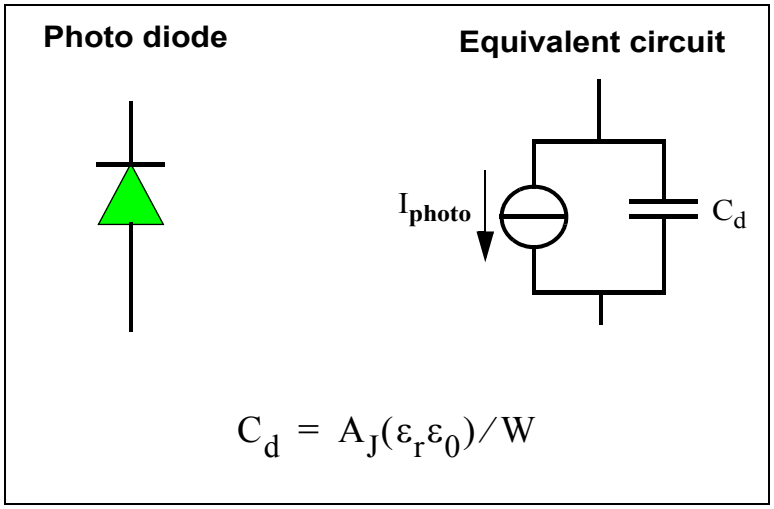
$$V_T = V_{T0} + \gamma(\sqrt{|2\Phi_F| + V_{sb}} - \sqrt{|2\Phi_F|}) \qquad (3.4)$$

By connection the maximum voltage (V_{aa}) to the gate, $V_{gs} = V_{ds}$, the transistor will always be saturated

$$V_{ds} > V_{ds,sat} = V_{gs} - V_T$$

but it will go into weak inversion and finally completely pinch off.



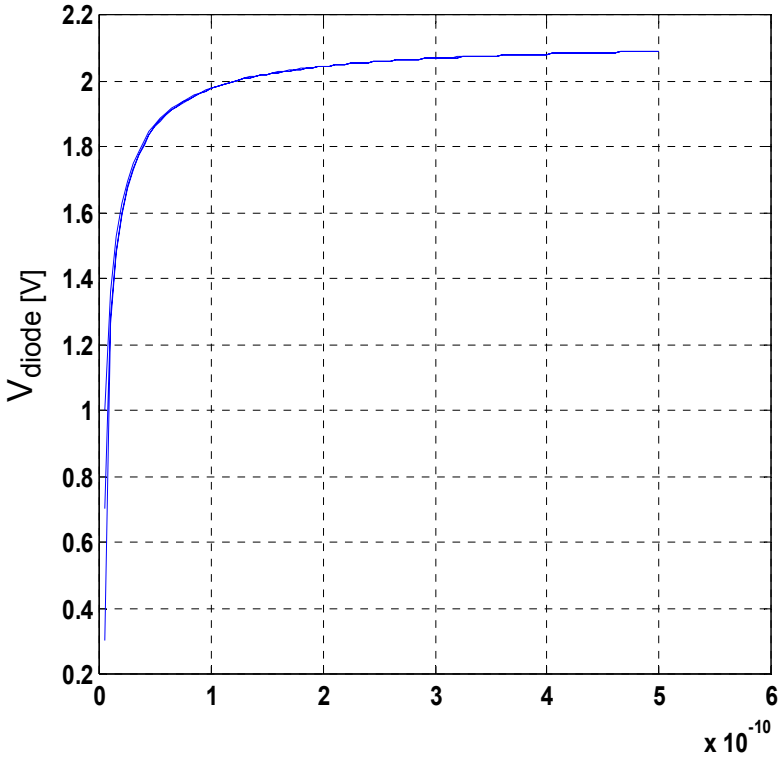


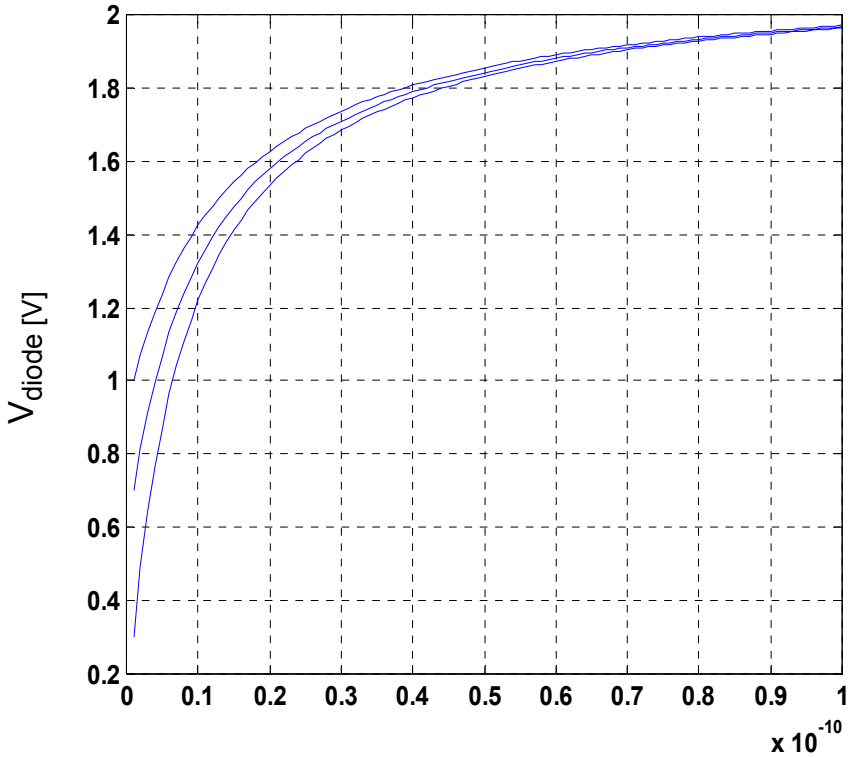
Simulated example:

W=2 μm
L= 0.3 μm

$V_{aa} = V_{rst} = 3$ V
$C_d = 10$ fF

$\mu C_{ox} = 150\ \mu A/V^2$
$\gamma = 0.2\ V^{1/2}$





Lag

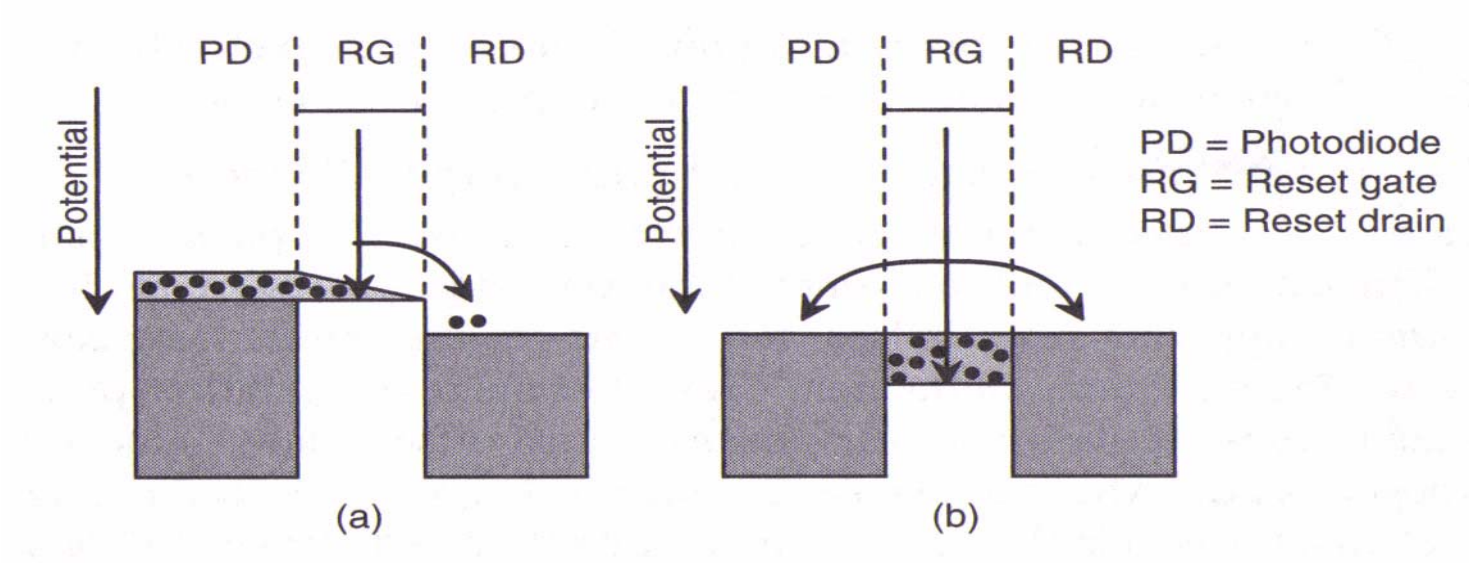
Final reset level at the end of the reset period, depends on the signal level at the beginning of the reset period. There will be some remaining charge in the photo diode. In other words, The image will contain remains from the previous image.

Methods to avoid lag:

Flushing: To charge the pixel completely before reset to make sure the start conditions are always the same, the remaining charge is always the same.

Hard reset: To make sure that the reset transistor does not pinch off, and the pixel is completely reset to V_{aa}.

- P-channel transistor. Draw back: Larger area due to the required N-well.
- Boosting the control signal V_{reset}. To generate a control signal with higher voltage than the power supply.



Boosting

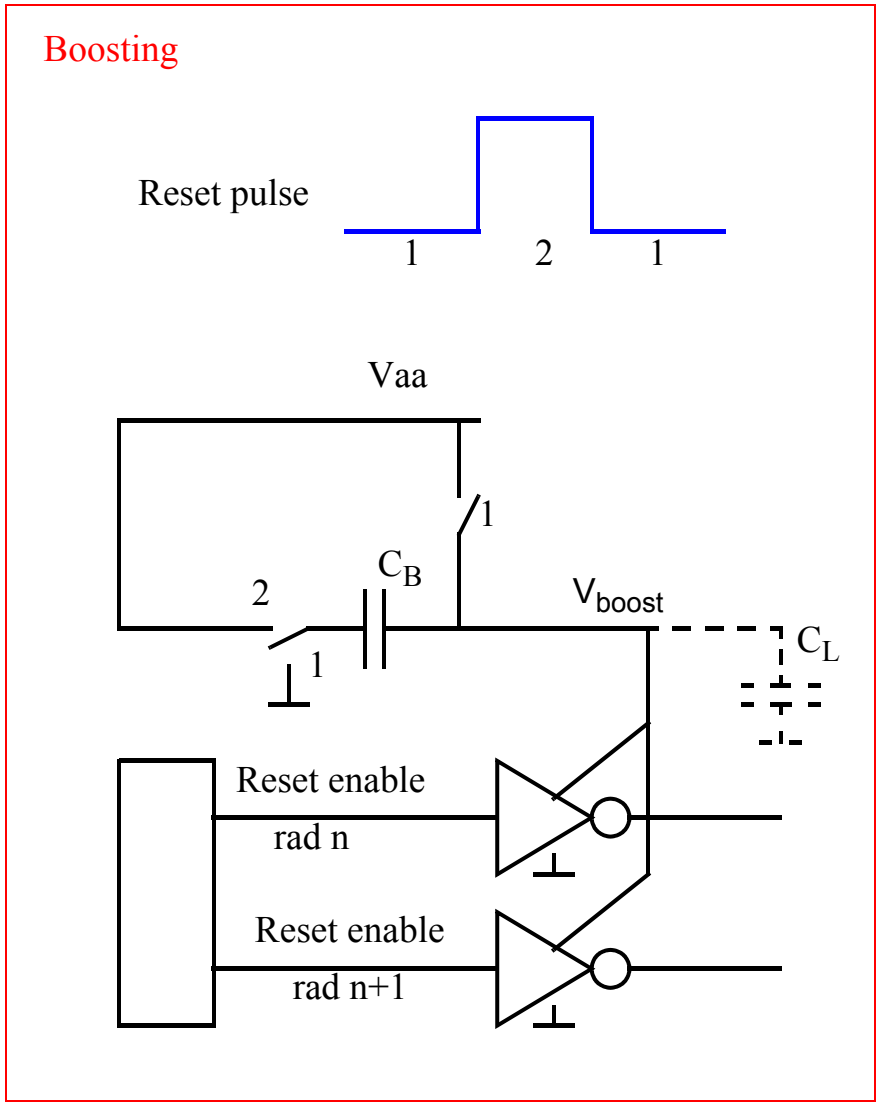
Phase 1:

C_B and C_L are charged to V_{aa}

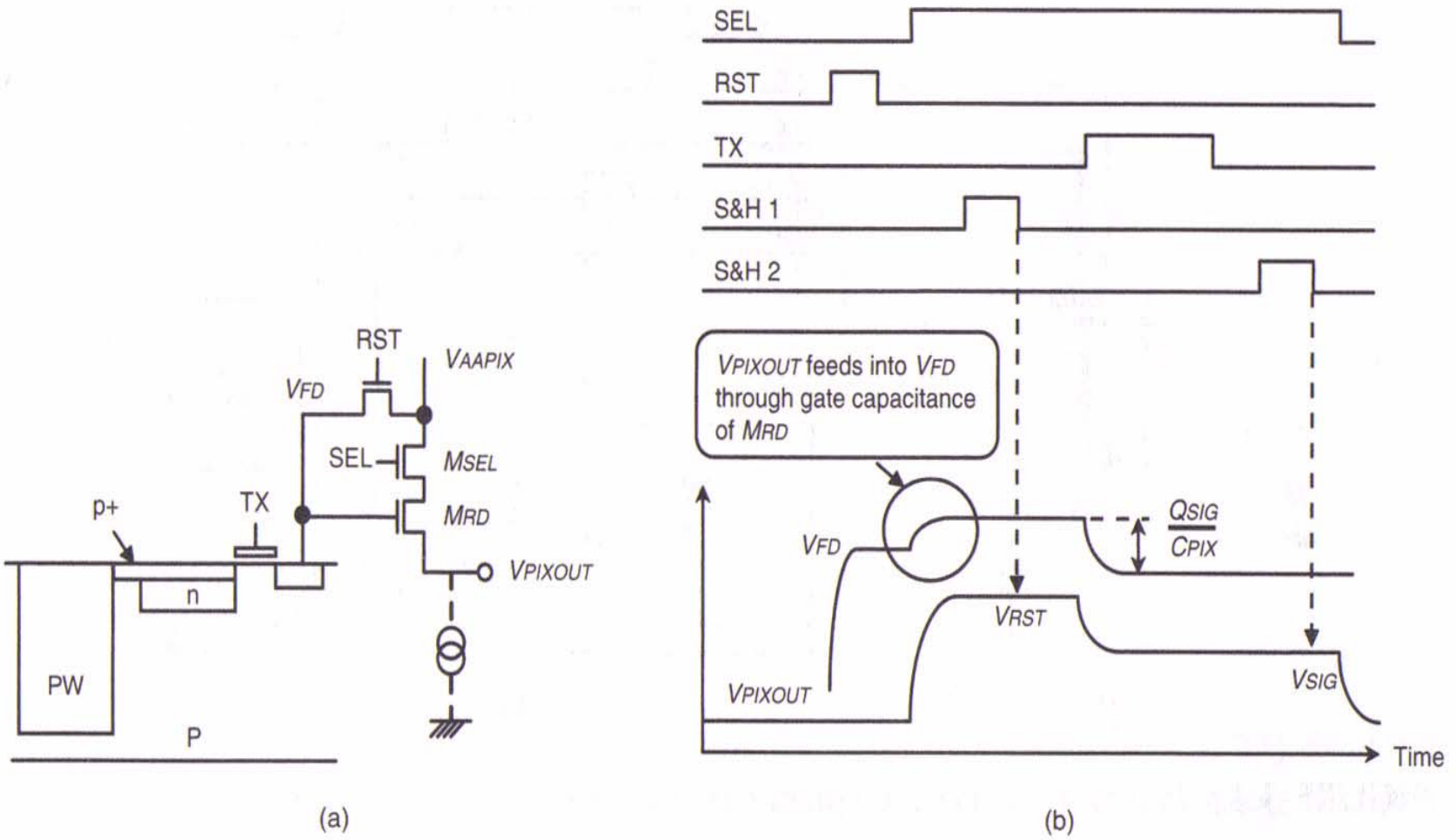
Phase 2:

Signal voltage is raised to

$V_{boost} = V_{aa} + V_{aa} * C_B / (C_L + C_B)$



Alternative boosting



Ref.: Nakamura

Pinned Photo diode

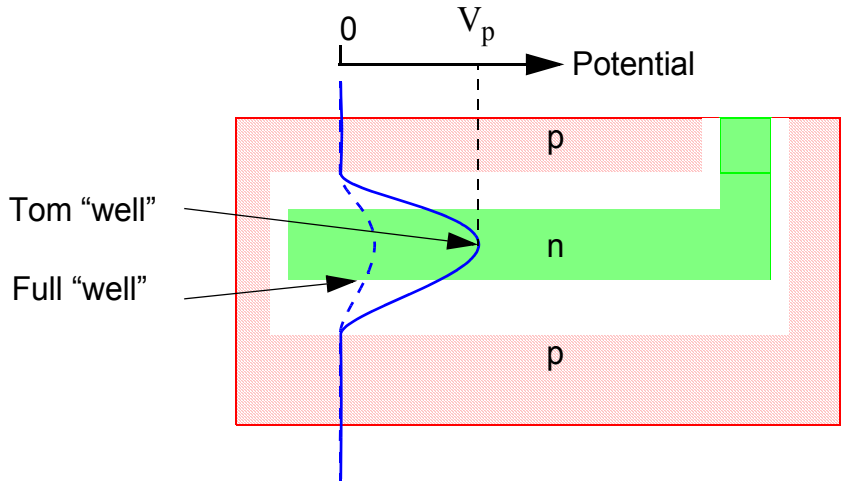
n-region buried in a p-substrate.
Reduces the effect of surface recombination

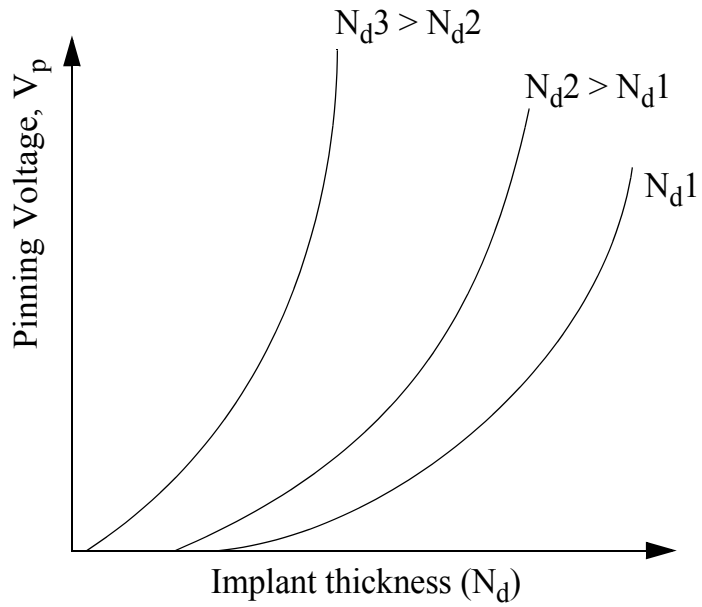
- Improved response in blue range
- Reduced dark current.

Pinned voltage = the voltage that results in a complete depletion of the n-region.

Pinning voltage depends on doping concentration and implantation range.

Added process step to standard CMOS process.
Patented: Eastman-Kodak/Motorola (ImageMOS^{TM}).





Noise Sampling

The signal that represents integrated light:

$$V_{signal} = V(t_{reset}) - V(t_{int}) \quad (3.5)$$

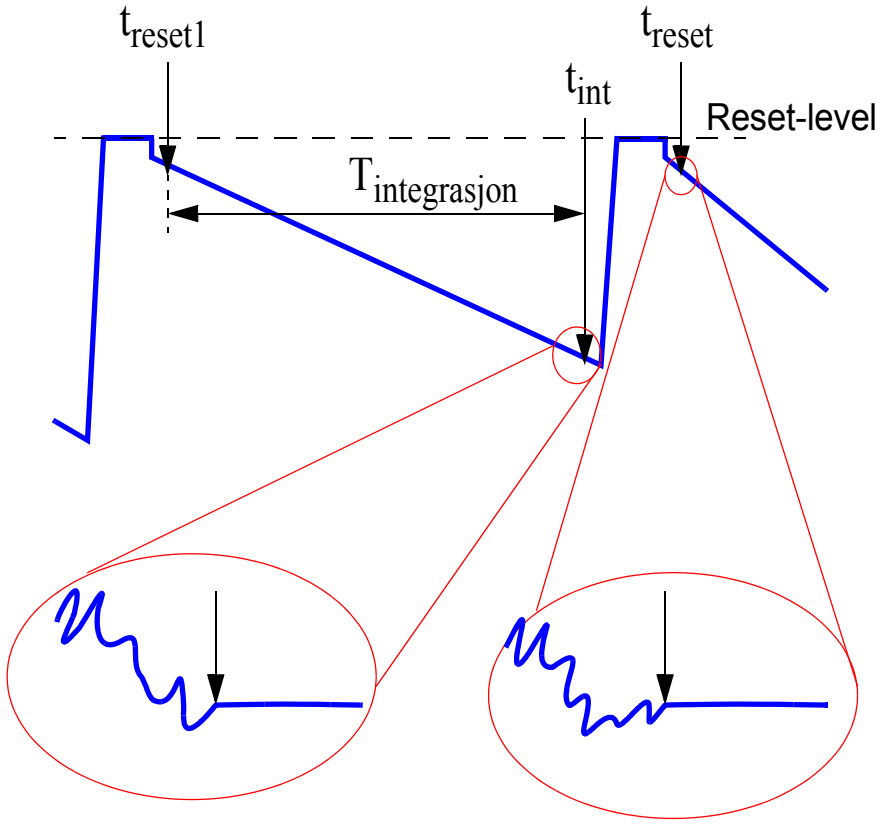
Noise sampled at the two time points are uncorrelated and contribute to the signal noise:

$$v_{n,\,rms} = \sqrt{[v_n(t_{reset})]^2 + [v_n(t_{int})]^2} \quad (3.6)$$

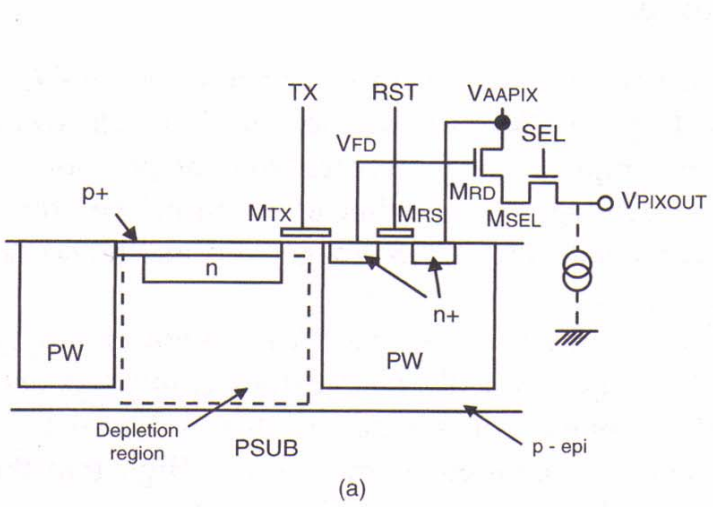
The noise sampled at point $t_{resert1}$ is correlated with the noise at t_{int}, but it cannot be used because it is not practical to store all pixel reset samples on capacitors during the exposure time.

However, the Fixed Pattern Noise due to variations in signal offset from pixel to pixel is removed.

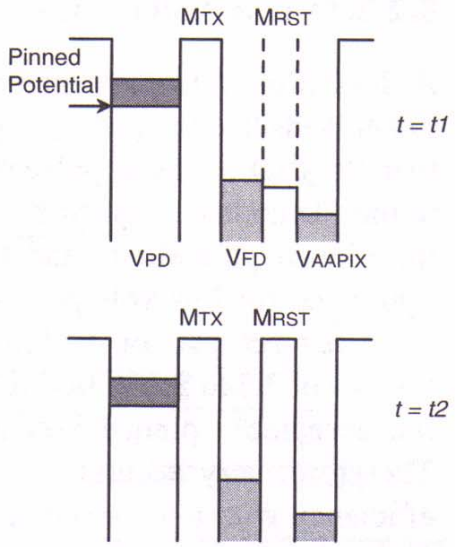
- Reset level variations
- Threshold voltage variations in the SF transistor

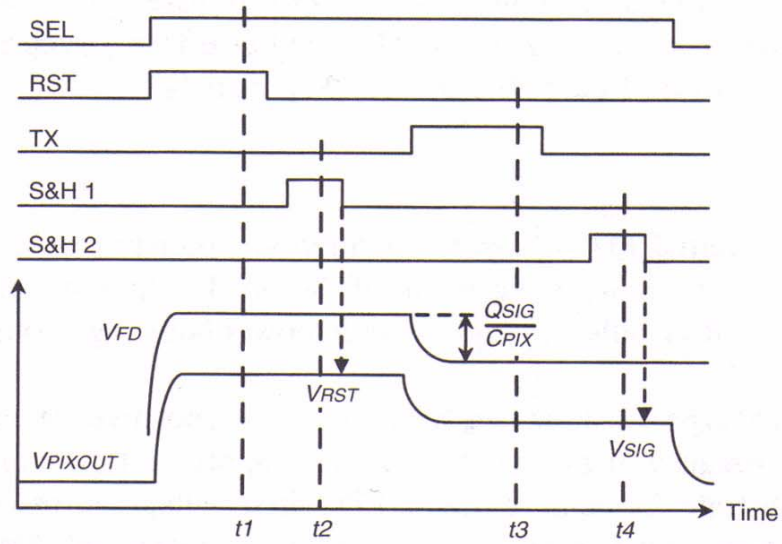


4T - Pixel



(a)



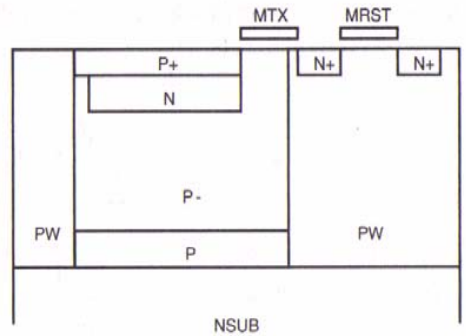


(b)

(c)

Ref.: Nakamura

Variant: N-sub

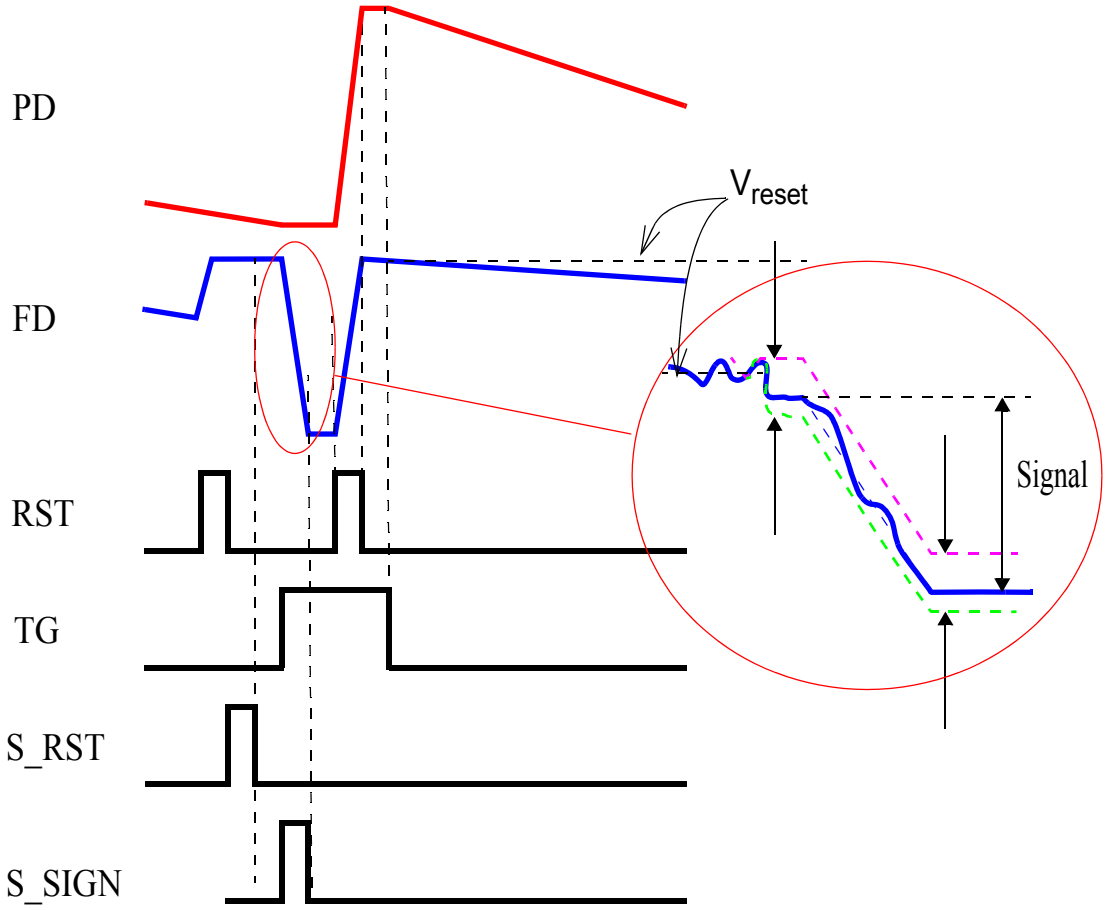


4T - pixel (forts.)

Correlated Double sampling

Both the Reset sample and signal sample after the charge transfer are related to the same reset voltage. No intermediate reset is performed.

Thus the difference V_{reset} - V_{signal} is independent on the noise from reset voltage source sampled on FD during the reset process. The reset noise cancels out.



4T Pixel - Summary

The generated charge stored on PD (Photo diode) during the integration is transferred completely to FD (Floating Diffusion) immediately after FD reset.
The signal is made up by the difference between the reset level and the level after integration:

$$V_{reset} - Q_{Transferred} / C_{FD}.$$

Pinning voltage, TX pulse height, and the capacity of FD is chosen such that complete transfer is achieved.

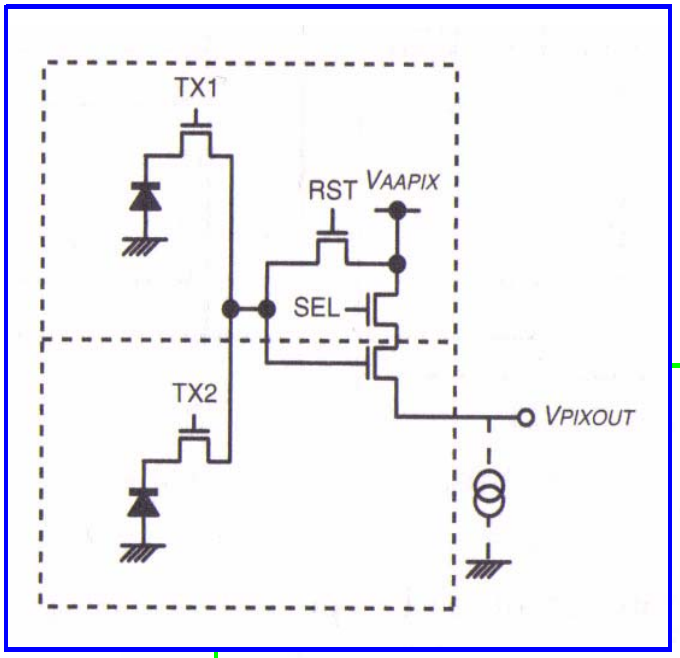
Advantages:

- High conversion gain -
  given by FD
- Large light sensitive area.
- High sensitivity to blue light.
- Low dark current
- Correlated double sampling reduces sampling noise.

Low threshold voltage for the TX-transistor is required.

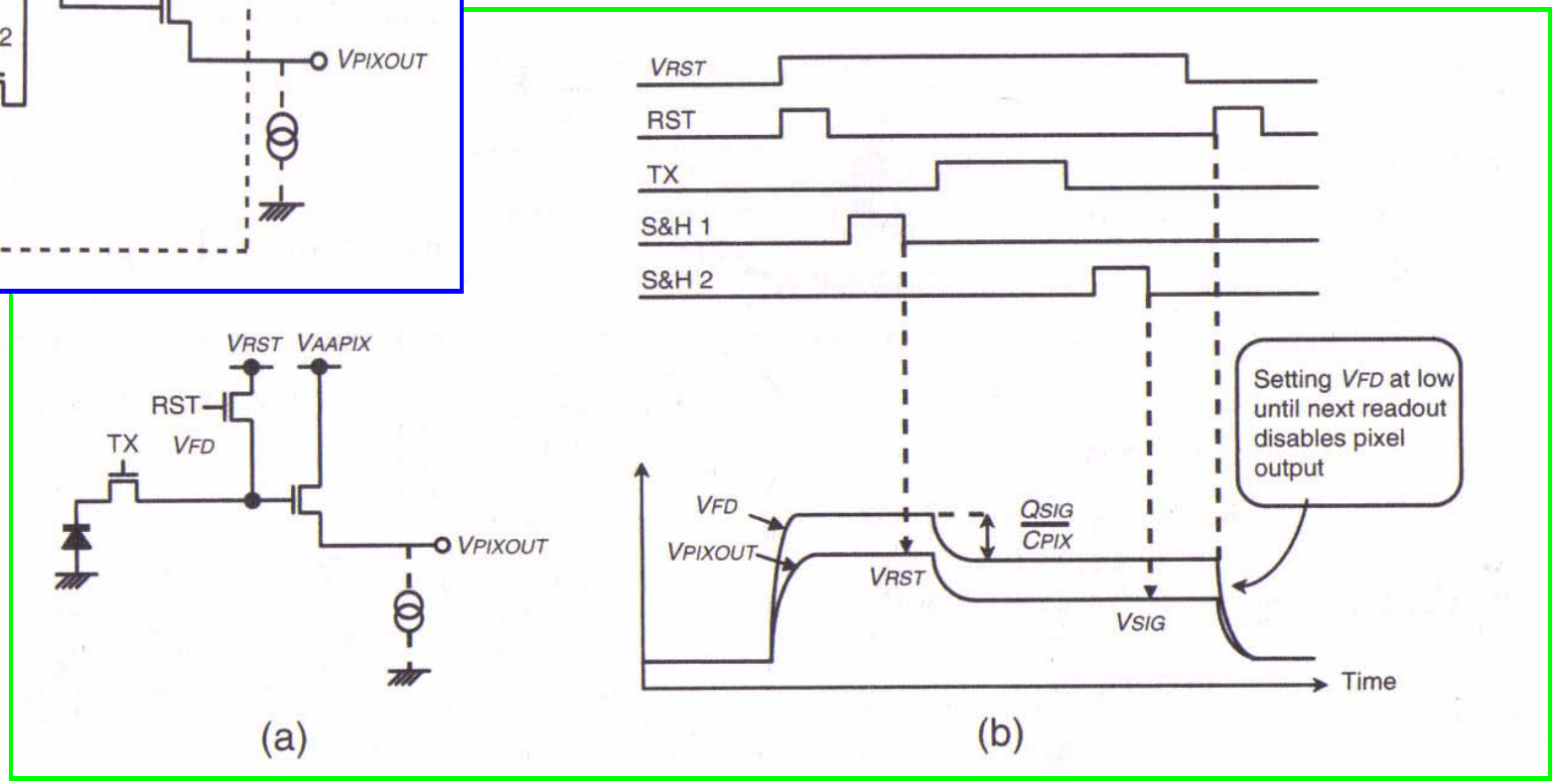
Complete charge transfer is prerequisite for low noise (zero sampling noise).

Method for reduction of the number of transistors



Two rows share
FD,
SF transistor,
RST transistor, and SEL transistor.

The two rows are separated by selection of TX1 or TX2,



Ref.: Nakamura

SOURCE FOLLOWER AMPLIFIER STAGE

Source follower

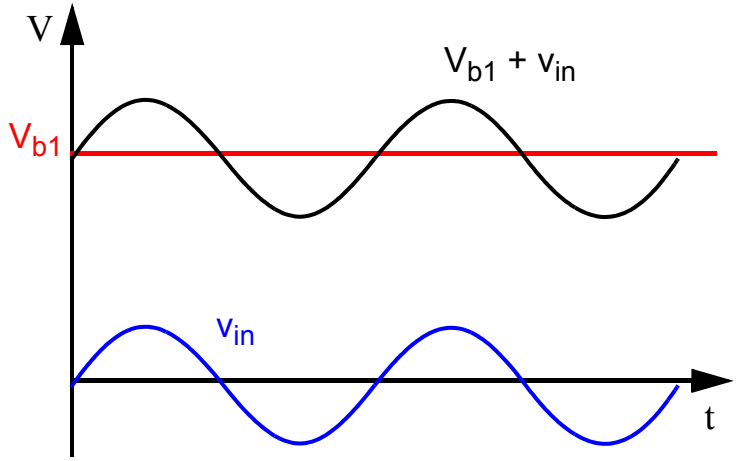
Quiescent point:

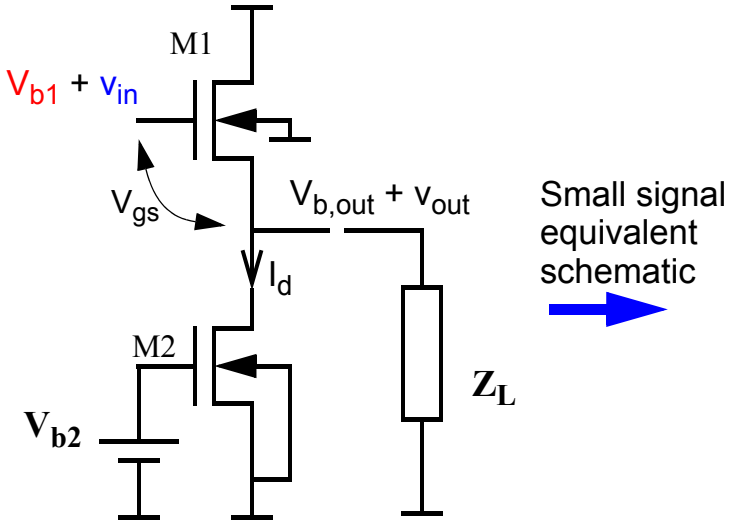
Quiescent current $$I_d = \frac{\mu C_{ox}}{2}\frac{W_2}{L_2}(V_{b2} - V_{T0})^2 \qquad (3.7)$$

Output voltage (DC), rel. V_{b1}: $$V_{gs} = \sqrt{\frac{2I_d}{\mu C_{ox}}\frac{L_1}{W_1}} + V_T \qquad (3.8)$$

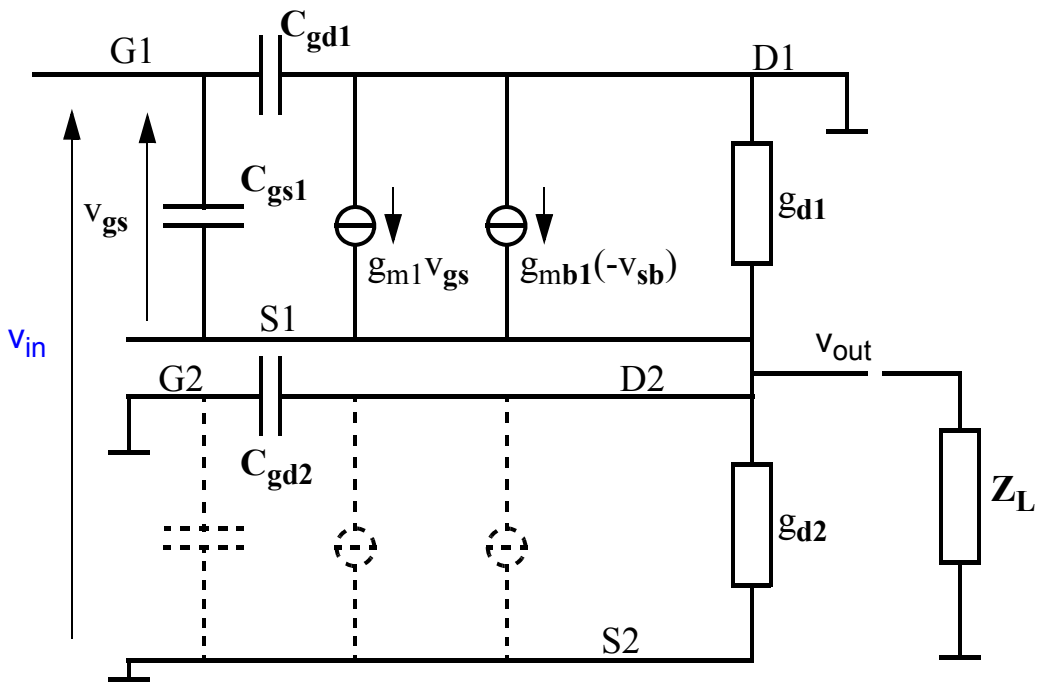
where V_T er given by

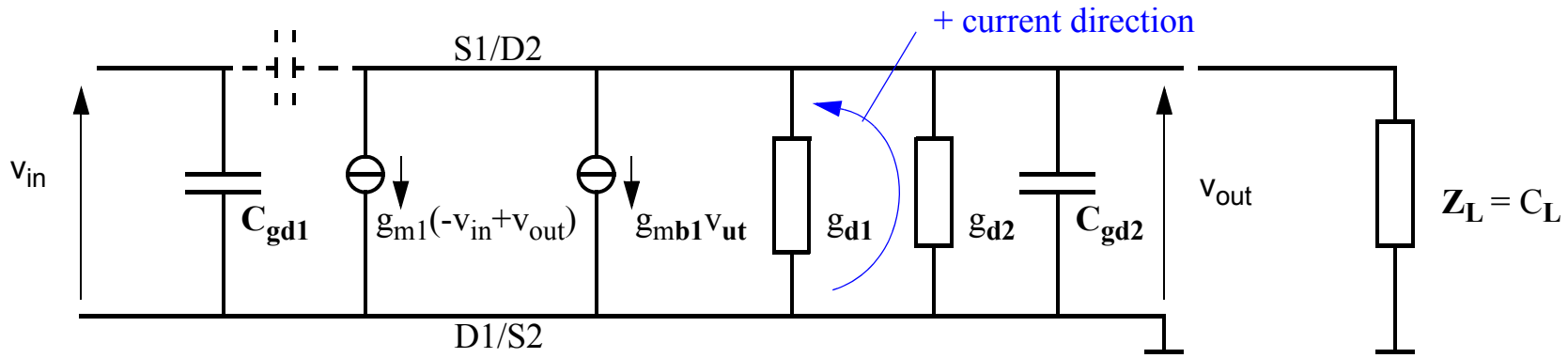
$$V_T = V_{T0} + \Delta V_T = V_{T0} + \gamma(\sqrt{|2\Phi_F| + V_{SB}} - \sqrt{|2\Phi_F|})$$





Small signal equivalent schematic





The pixel read-out circuit's output impedance, Z_L, is typically capacitive (C_L).
The time constant related to the output and upper cut off frequency f_h is:

$$\tau_h = \frac{C_{gd2} + C_L}{g_{d1} + g_{d2}} \quad \Rightarrow \quad f_h = \frac{\omega_h}{2\pi} = \frac{1}{2\pi\tau_h} \tag{3.9}$$

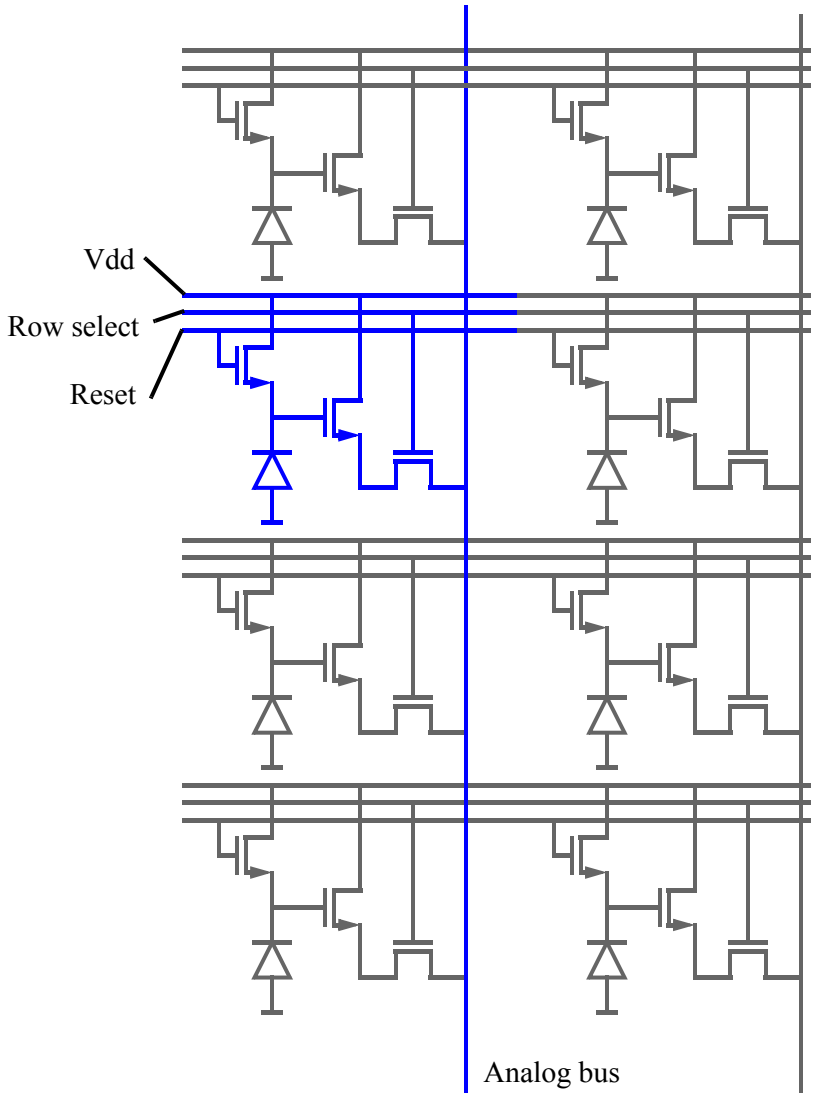
For $f << f_h$:

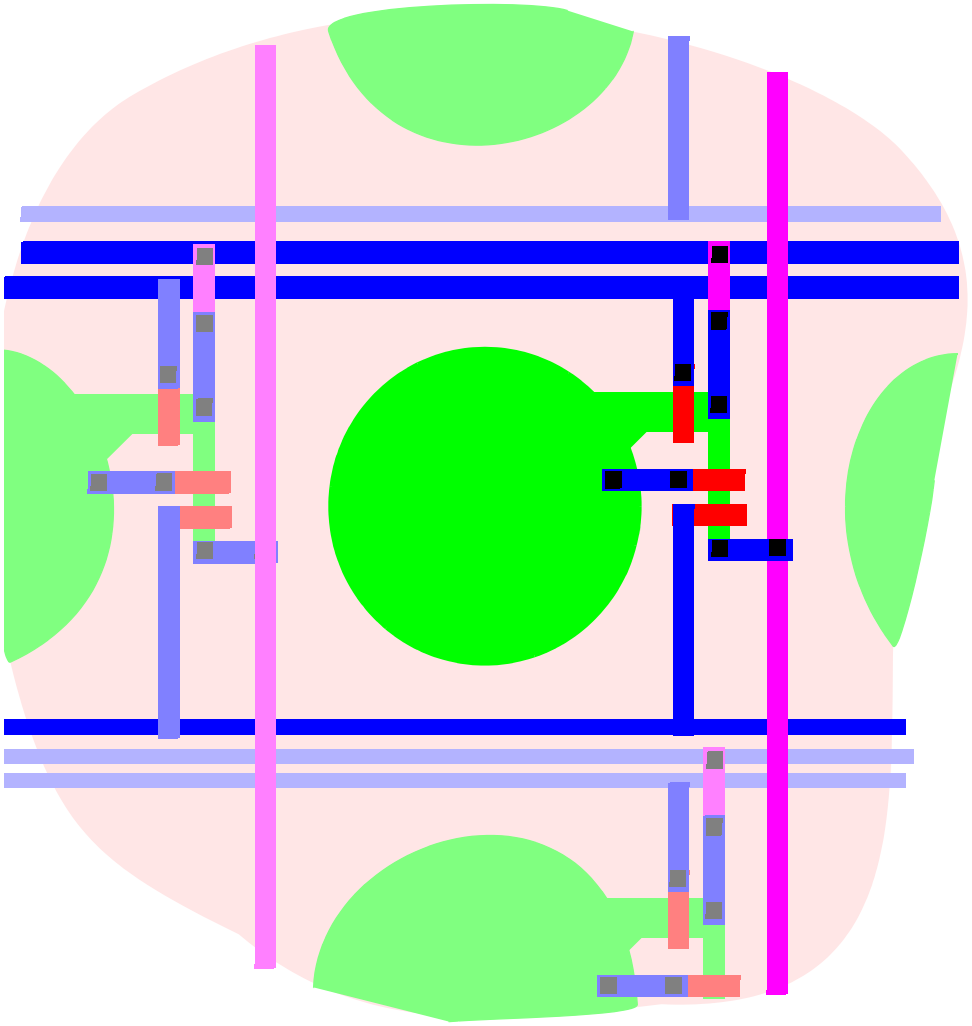
$$v_{ut} = \frac{g_{m1}v_{in} - g_{m1}v_{out} - g_{mb1}v_{out}}{g_{d1} + g_{d2}} \tag{3.10}$$

Gives the amplification:

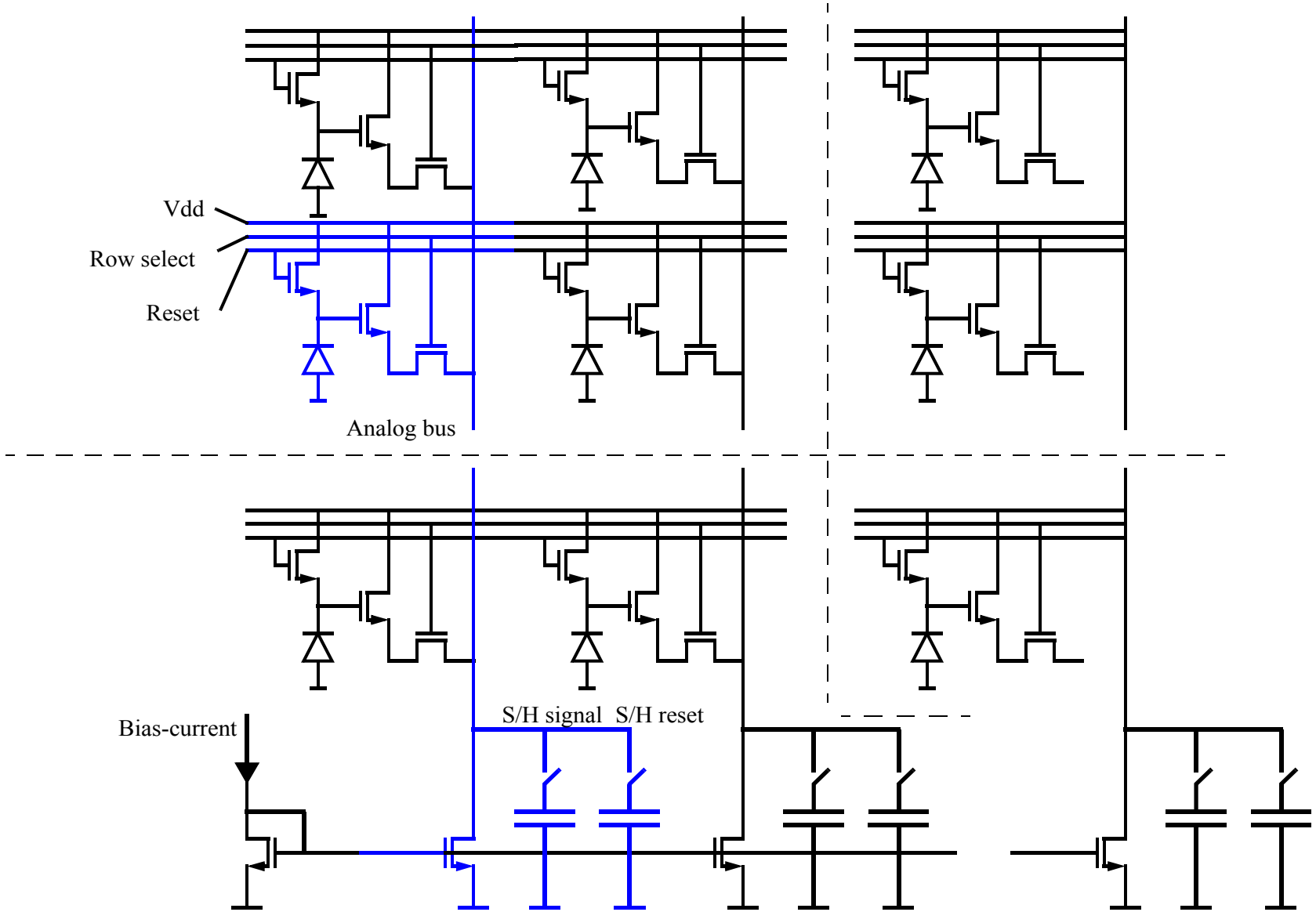
$$\frac{v_{ut}}{v_{inn}} = \frac{g_{m1}}{g_{m1} + g_{mb1} + g_{d1} + g_{d2}} \approx \frac{g_{m1}}{g_{m1} + g_{mb1}} < 1, \quad \text{typically 0.7-0.8} \tag{3.11}$$

Pixel Array

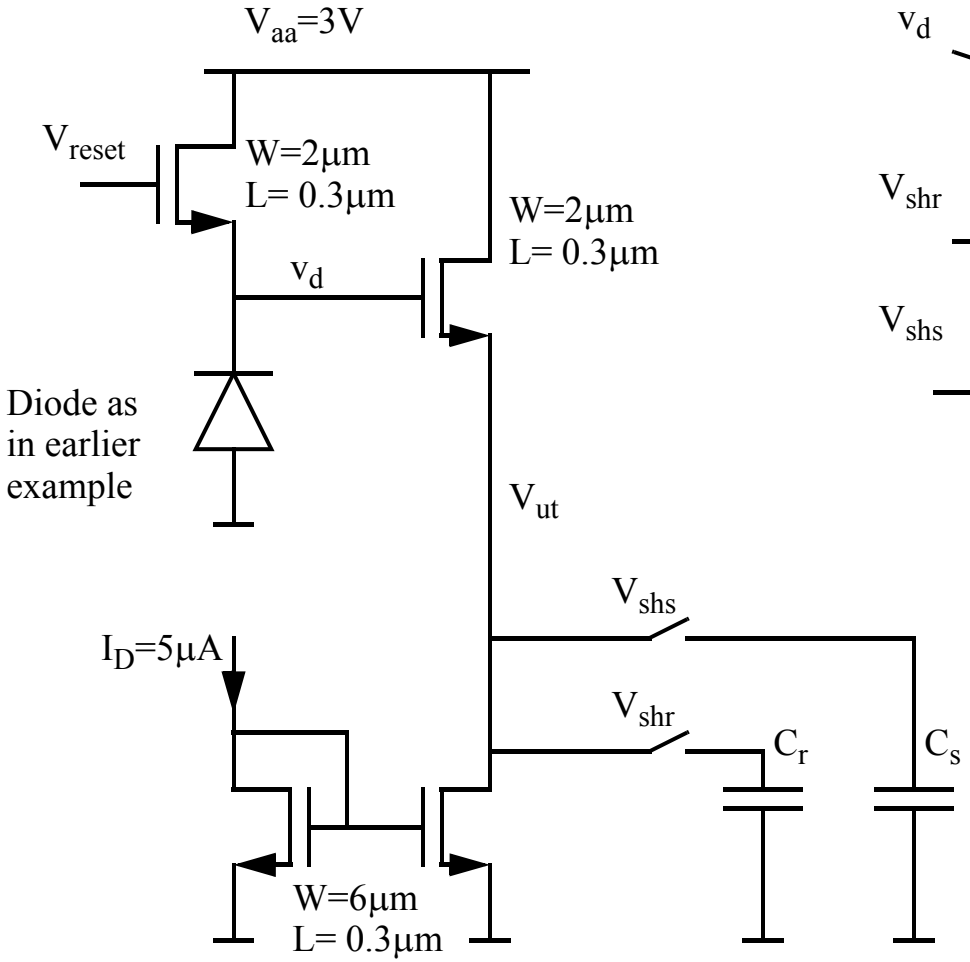


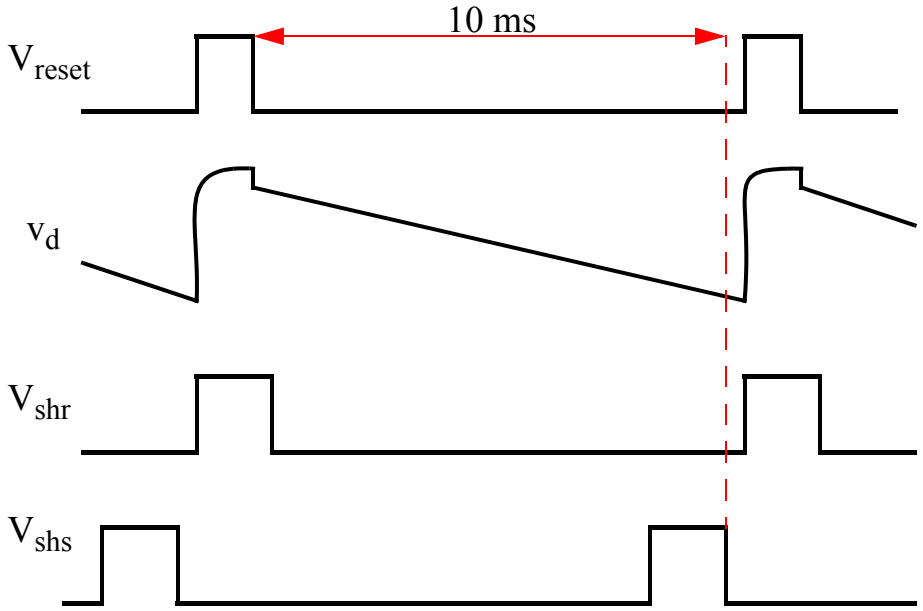


Pixel Array (cont.)



Example - Source Follower





V_{out} and sampled values of signal and reset?

$\mu C_{ox} = 150\ \mu A/V^2$
$V_{T0} = 0.7V$
$\Phi_F = 0.28\ V$
$\gamma = 0.2\ V^{1/2}$

APPENDIX 1: MOS TRANSISTOR MODEL

MOS-structure

(Metal Oxide Semiconductor)

The contact potential* Φ_{ms}, forms a depletion range at the Silicon surface (Similar to a PN junction).

- Majority carriers are depleted away from the surface.
- Gives band bending.
- At equilibrium, the distance between the conduction band E_c and the Fermi level is large. Therefore the carrier concentration in the conduction band is low.

Band bending:

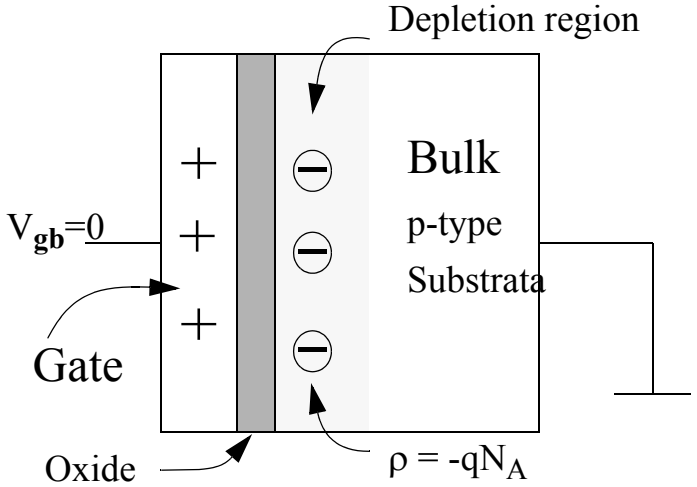
$$\Phi_S - \Phi_B = \frac{E_i \text{at the interface} - E_i \text{ in bulk}}{q}$$

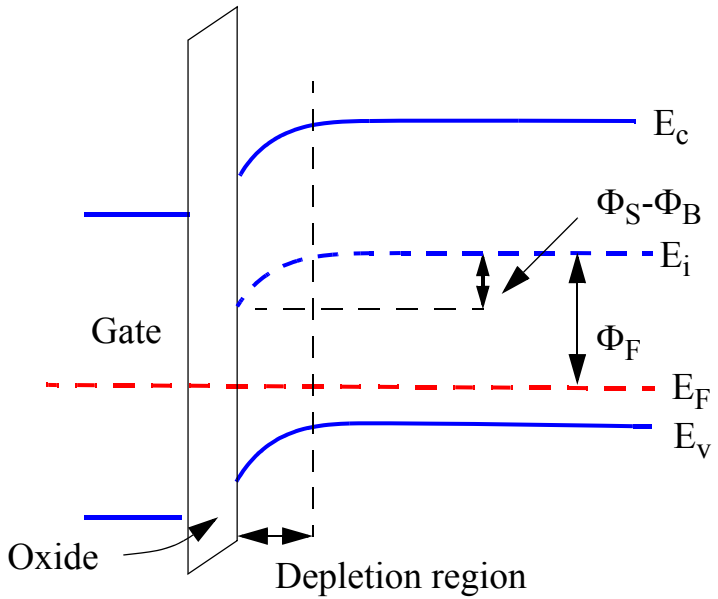
Potential difference between intrinsic Fermi level E_i and the actual Fermi level E_F:

$$\Phi_F = \frac{E_i - E_F}{q}$$

Band bending is changed by external voltage at the Gate. The system is then no longer in equilibration.

* Contact potential = the difference in electron escape energy divided by its charge q.





Positive Bias Voltage at the Gate

By increasing the band bending the distance E_c - E_F at the interface is reduced, and the minority carrier concentration increases.

When the total band bending corresponds to 2x the difference E_i-E_F, we have by definition strong inversion:

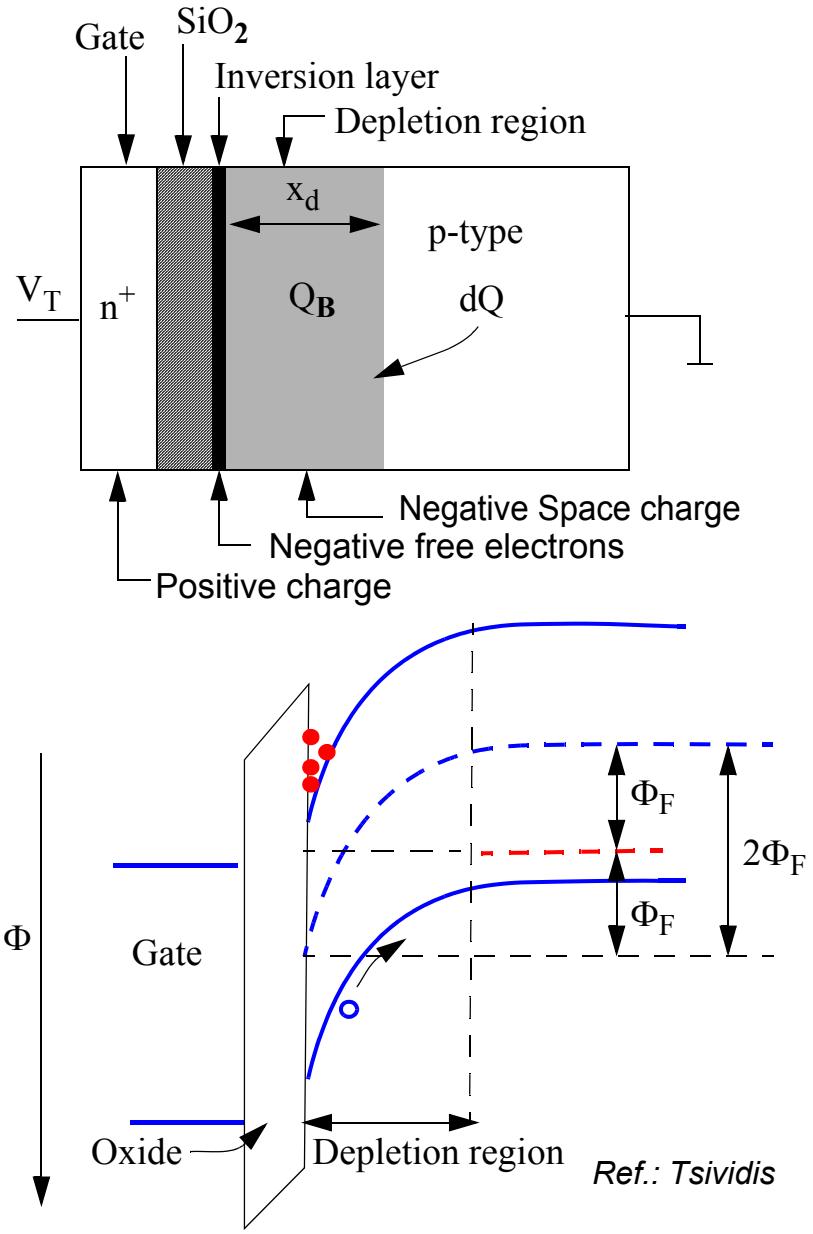
$$\Phi_S - \Phi_B = 2\Phi_F$$

Where Φ_S is the semiconductor surface potential and Φ_B is the bulk potential.

The electron density is then high compared to the dopant concentration and becomes the majority carriers, that is, a p-type semiconductor is inverted to a n-type close to the Si/SiO_2 interface. Similarly, a n-type is inverted to a p-type by adding a negative voltage on the Gate.

If the potential or band bending is further increased, only a small amount of space charges are uncovered. That is, a small increase of the depletion region, the charge is mainly added by generation of electrons. Thus, it is the inversion layer that constitute the charge contribution to the capacitor with oxide as dielectric.

The threshold voltage is defined as the voltage V_{GB} required to bring the surface just into strong inversion: $\Phi_S=2\Phi_F$.



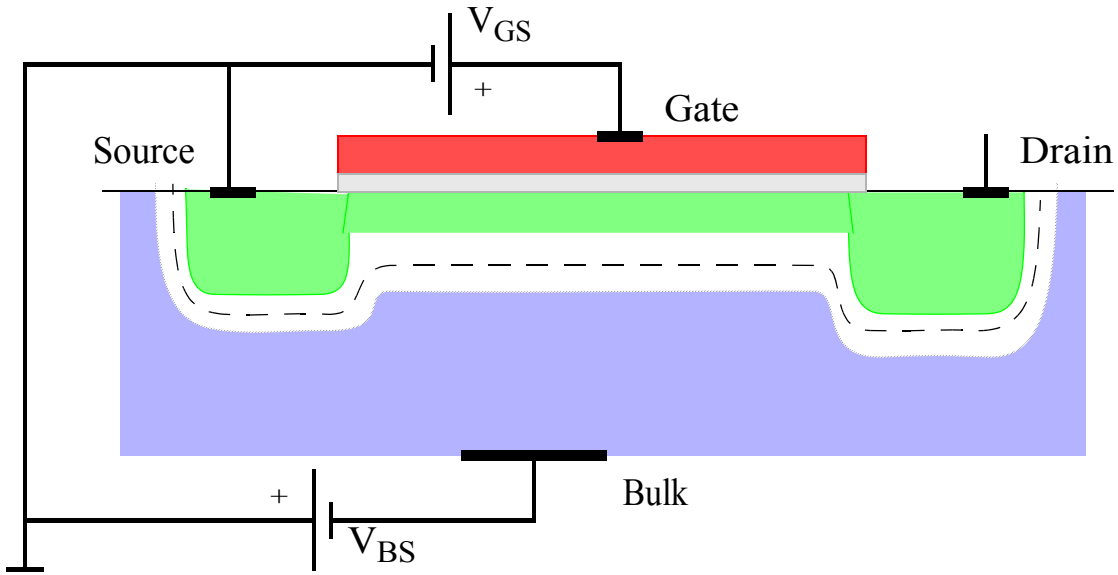
On a transistor with 4 terminals, the threshold voltage is the Gate-Source voltage, V_{GS}, that gives strong inversion.
If the Source voltage is connected to Bulk (grounded), V_{T0} is the threshold voltage at V_B=0.
The inversion layer forms a conduction channel underneath the gate between the Source and Drain regions.

Source-Bulk voltage, V_{BS}, changes the band bending and the charge Q_B in the depletion region (Source has contact to the channel).

The resulting threshold voltage can be written:

$$V_T = V_{T0} + \Delta V_T = V_{T0} + \gamma\left(\sqrt{\left|2\Phi_F\right| + V_{SB}} - \sqrt{\left|2\Phi_F\right|}\right)$$

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_{si}\varepsilon_0}}{C_{ox}} \qquad \textbf{(3.A1)}$$



Drain current in the linear region

$V_{ds} < V_{GS} - V_T$

The channel has a given resistivity. The current creates a voltage variation v(y) along the channel. A voltage higher than the threshold gives charge in the inversion layer.

Inversion layer charge:

$$Q_I(y) = -C_{ox}[v(y) - (V_{GS} - V_T)]$$

Current in the channel of width W:

$$I_D = WQ_I(y)\mu E = WQ_I(y)\mu\frac{dv}{dy}$$

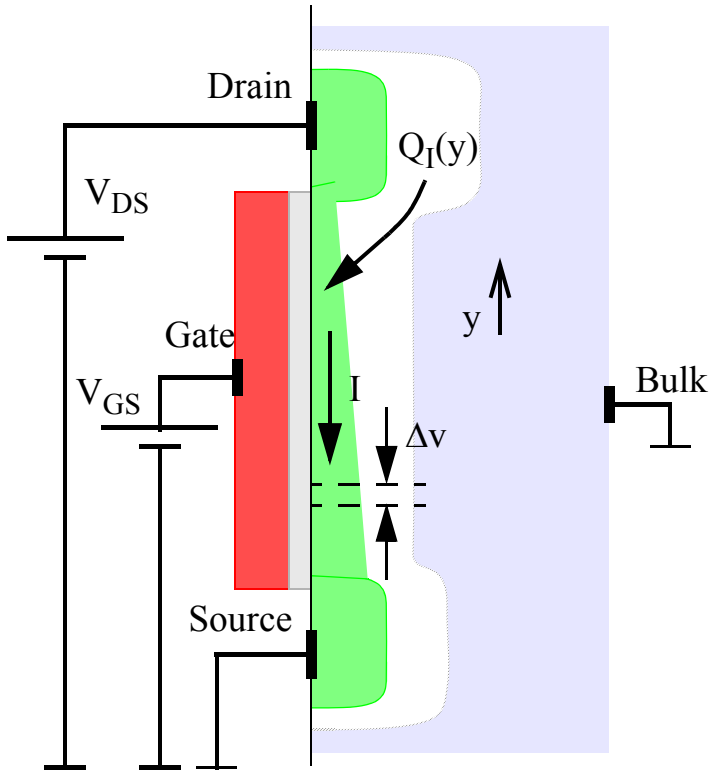
μ is the carrier mobility typically:
$\mu_n = 135\ \mu m^2/(V.ns)$, $\mu_p = 50\ \mu m^2/(V.ns)$

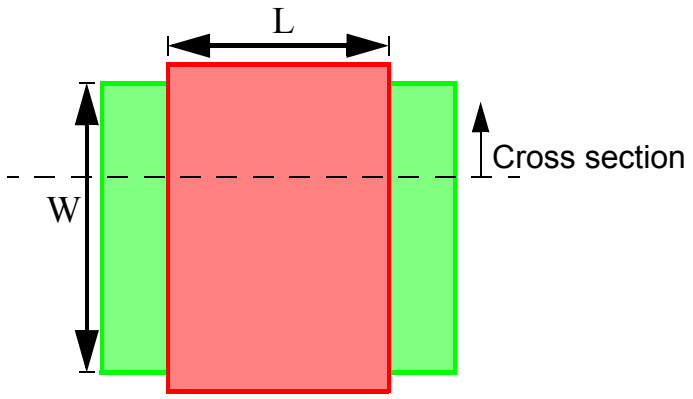
A change of variables and integration on both sides of the equation above gives:

$$Q_I(y) = Q_I(v(y)) \qquad v(y)\big|_{y=0} = 0 \qquad v(y)\big|_{y=L} = V_{DS}$$

$$\int_0^L I_D dy = W\mu C_{ox}\int_0^{V_{DS}} [V_{GS} - v - V_T]dv$$

$$I_D = \mu C_{ox}\frac{W}{L}\left[V_{GS} - V_T - \frac{1}{2}V_{DS}\right]V_{DS} \qquad \textbf{(3.A2)}$$





Drain current in saturated transistor

$V_{ds} > V_{GS} - V_T$

Charge concentration in the inversion layer at the pinch-off point must be zero:

$$Q_I(y1) = C_{ox}[V_{GS} - v(y1) - V_T] = 0$$

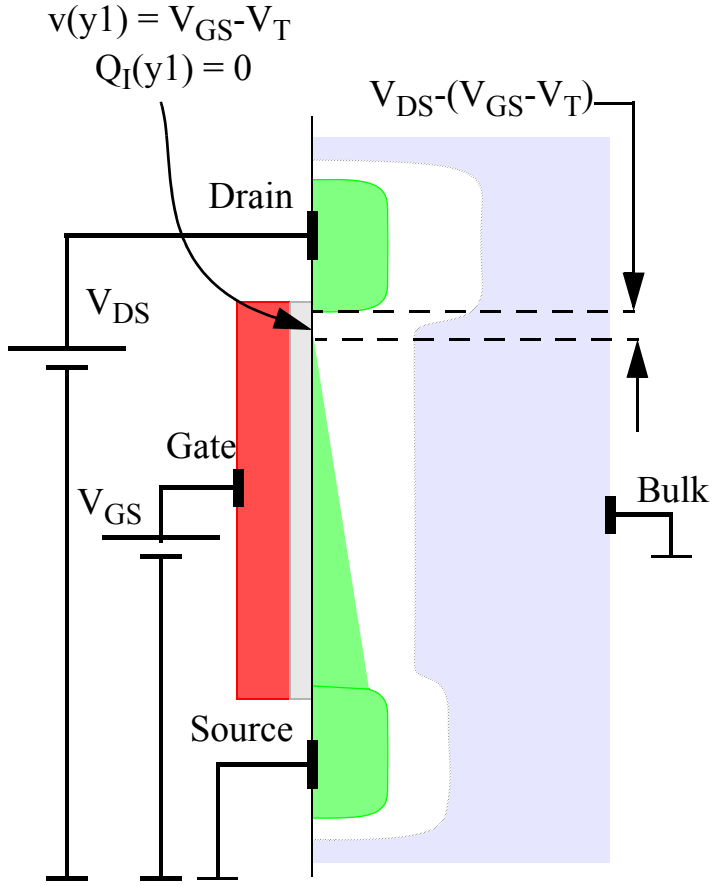
$$C_{ox}[V_{GS} - (V_{GS} - V_T) - V_T] = 0$$

We see that v(y1) must be equal to V_{GS}-V_T.

When V_{DS} increases beyond V_{GS}-V_T, the voltage increase appear between Drain and the pinch-off point; an increase in the field in that region. The potential difference between source and the pinch off point becomes $V_{GS} - V_T$ (Source is grounded) and is independent on V_{DS}.

Replacing V_{DS} with $V_{GS} - V_T$ inn i (3.A2):

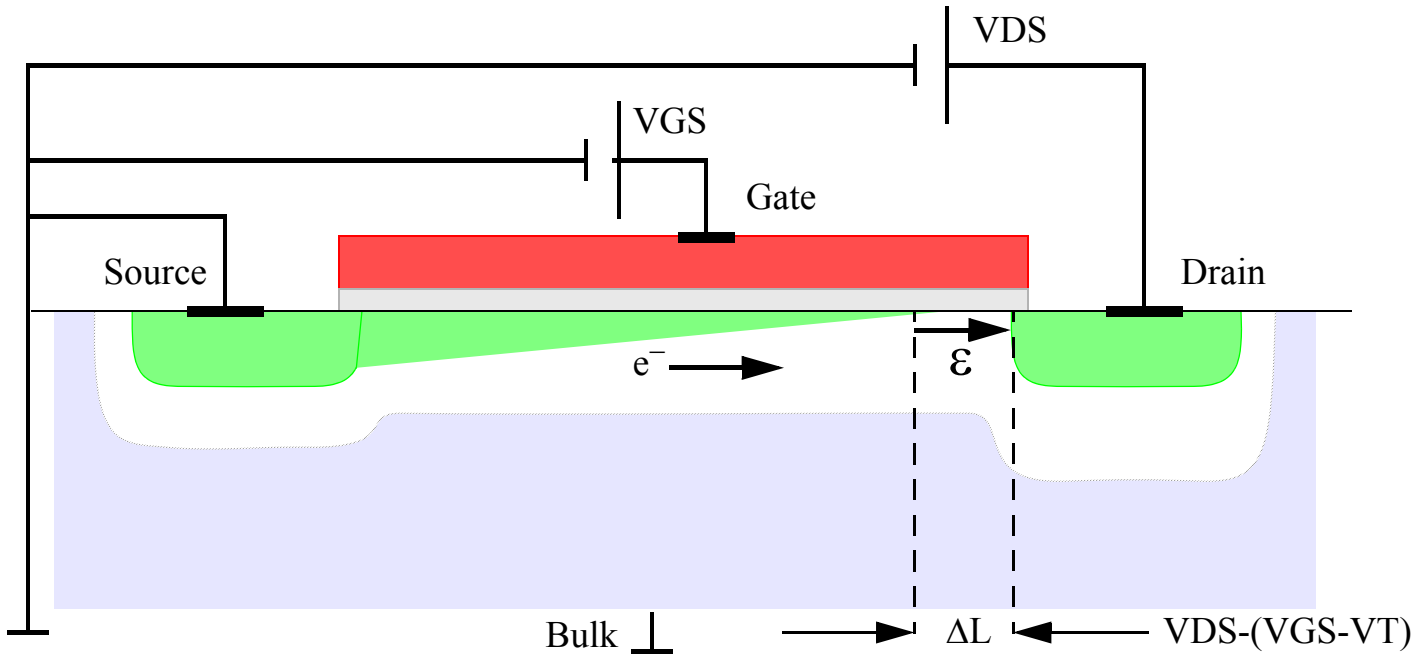
$$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}[V_{GS} - V_T]^2 \qquad \textbf{(3.A3)}$$



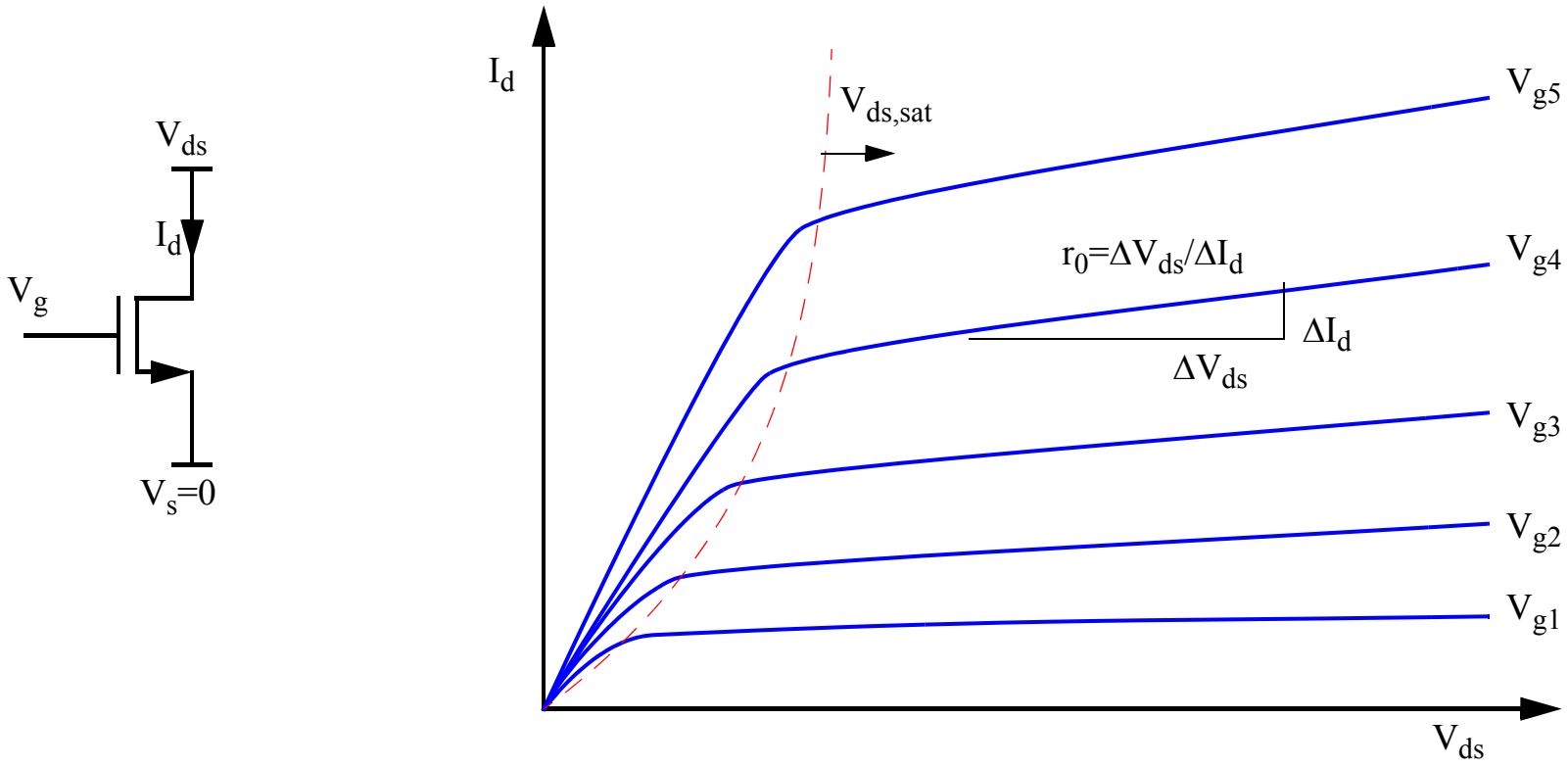
Channel length modulation.

In saturation, the channel length is shortened with increasing V_{DS}. The shortening increases the current because the current is limited by diffusion in the inversion layer along the channel, not by the field across the region between Drain and Pinch off point. The carriers are driven fast across this region. The effect is important for short channels.

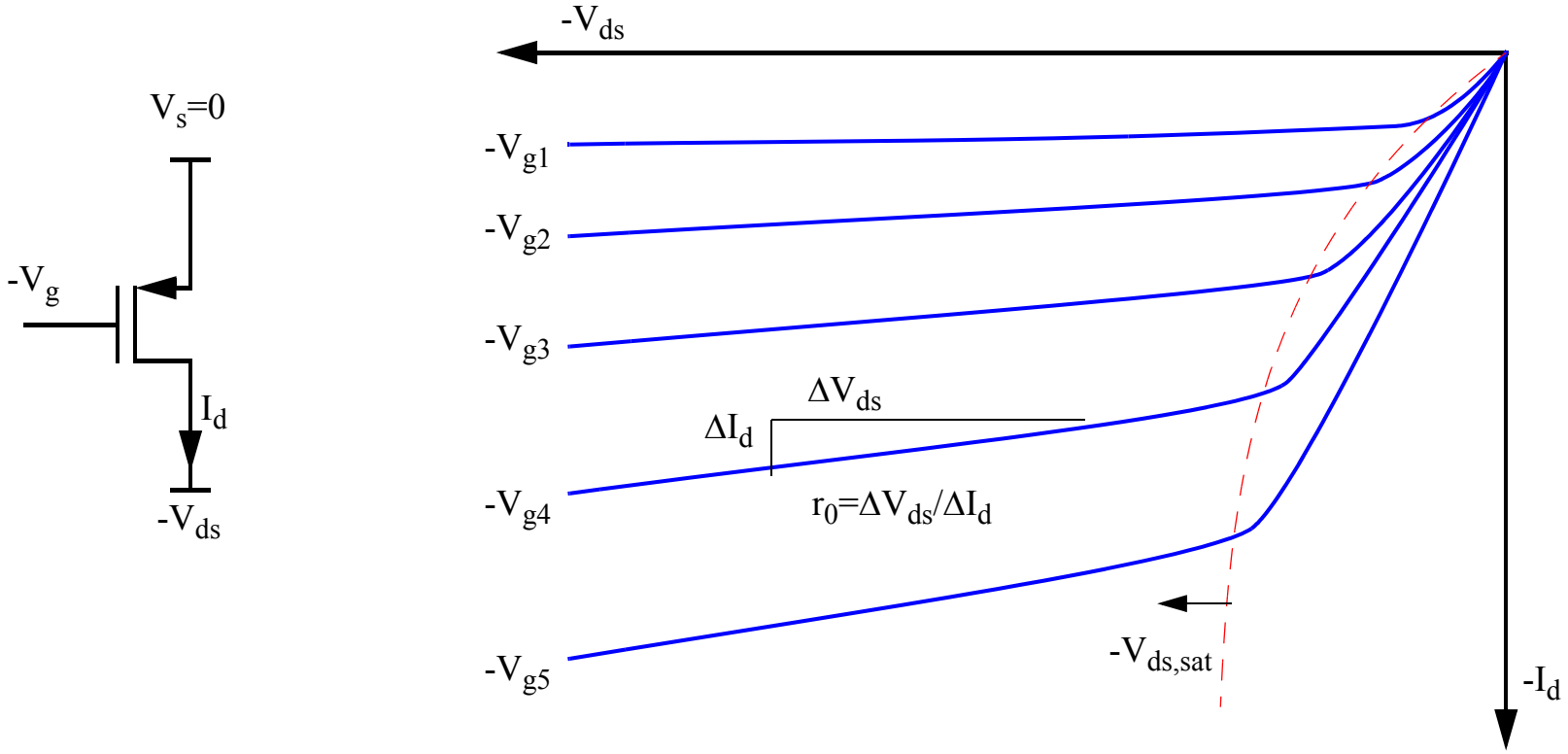
$$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}[V_{GS} - V_T]^2(1 + \lambda V_{DS}) \qquad \textbf{(3.A4)}$$



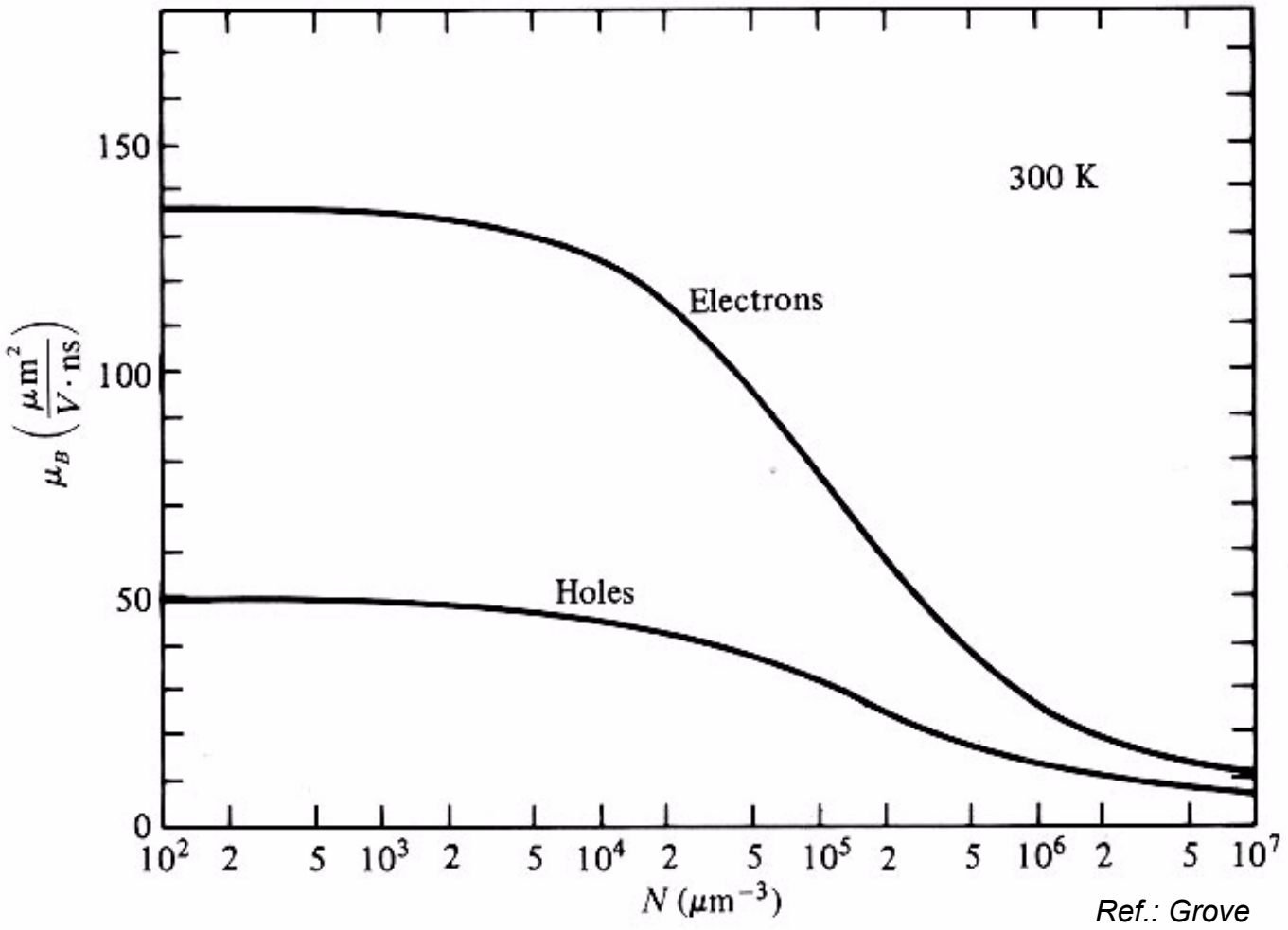
Output characteristics for NMOS



Output characteristics for PMOSt



Mobility as a function of doping concentration



Ref.: Grove

Small signal parameters:

Transconductans at constant V_{SB}, $V_{DS} > V_{GS} - V_T$. (Differentiate (3.A3))

$$g_m = \frac{dI_d}{dV_{gs}} = 2\frac{\mu C_{ox}}{2}\frac{W}{L}[V_{gs} - V_T] = \sqrt{\left(2\mu C_{ox}\frac{W}{L}\right)\left(\frac{\mu C_{ox}}{2}\frac{W}{L}\right)[V_{gs} - V_T]^2} = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \qquad \textbf{(3.A5)}$$

Bulk transconductans at constant V_{GS}, $V_{DS} > V_{GS} - V_T$ (Differentiate (3.A3) with V_T given by (3.A1))

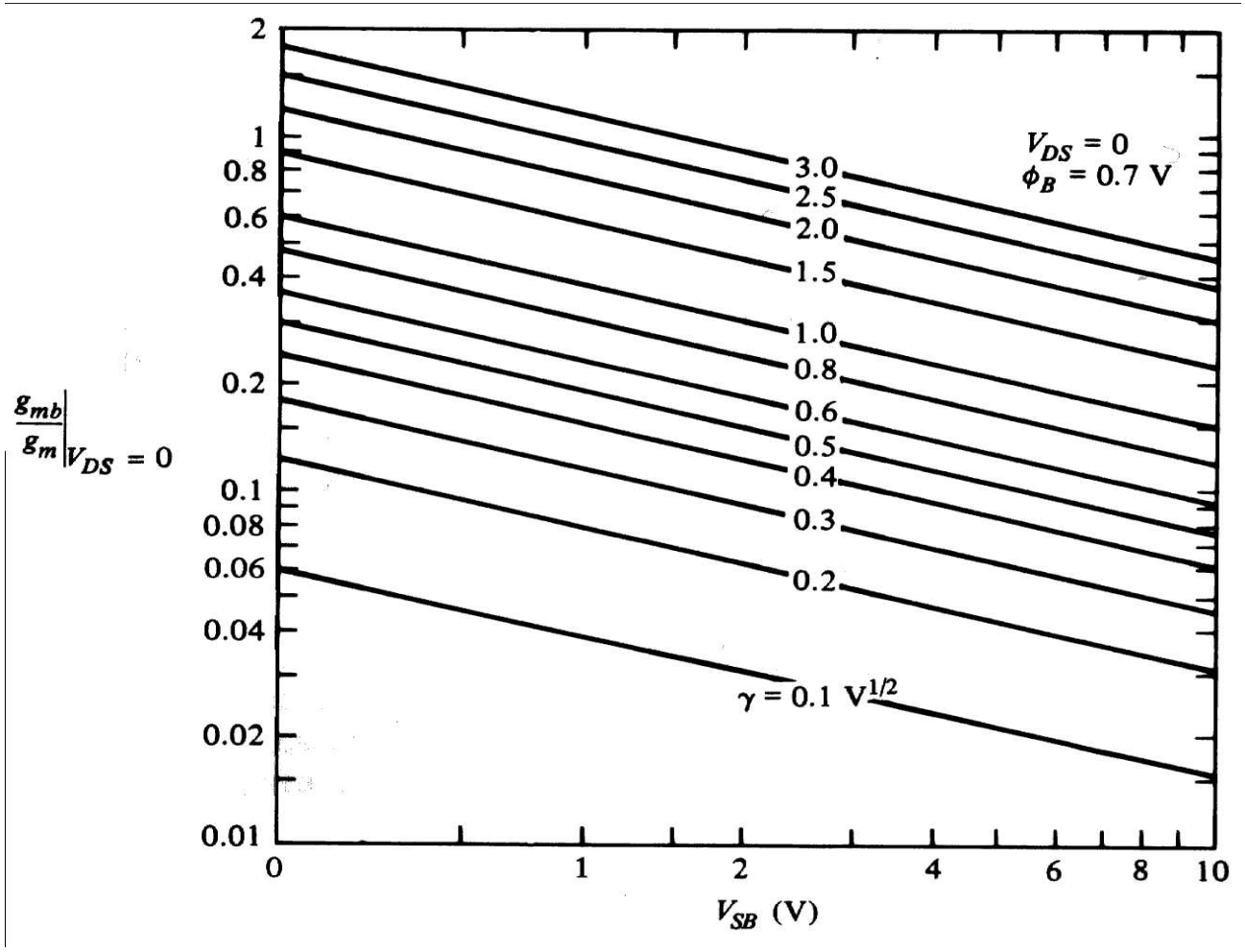
$$g_{mb} = \frac{dI_d}{dV_{sb}} = \frac{dI}{dV_T}\frac{dV_T}{dV_{sb}} = 2\frac{\mu C_{ox}}{2}\frac{W}{L}[V_{gs} - V_T]\frac{\gamma}{\sqrt{|2\Phi_F| + V_{sb}}} = \frac{\gamma\ gm}{\sqrt{|2\Phi_F| + V_{sb}}} \qquad \textbf{(3.A6)}$$

Output conductance (differentiate (3.A2) and (3.A4)

$$g_d = \frac{dI_d}{dV_{ds}} = \mu C_{ox}\frac{W}{L}[V_{gs} - V_T - V_{ds}] \qquad V_{ds} < V_{gs} - V_T \qquad \textbf{(3.A7)}$$

$$g_d = \frac{dI_d}{dV_{ds}} = \frac{\lambda I_{DS}}{(1 + \lambda V_{DS})} \approx \lambda I_{DS} \qquad V_{ds} \geq V_{gs} - V_T \qquad \textbf{(3.A8)}$$

The ratio g_{mb} to g_m



Ref.: Grove

Capacitance

For $V_{ds} < V_{gs}-V_T$:

$$C_{gc} = C_{ox}WL + 2C_{ovl}W \quad \textbf{(3.A9)}$$

$$C_{cb} = \frac{\varepsilon_{si}}{x_d}WL \quad \textbf{(3.A10)}$$

For $V_{ds} > V_{gs}-V_T$:

$$C_{gs} = \frac{2}{3}C_{ox}WL + C_{ovl}W \quad \textbf{(empiric)} \quad \textbf{(3.A11)}$$

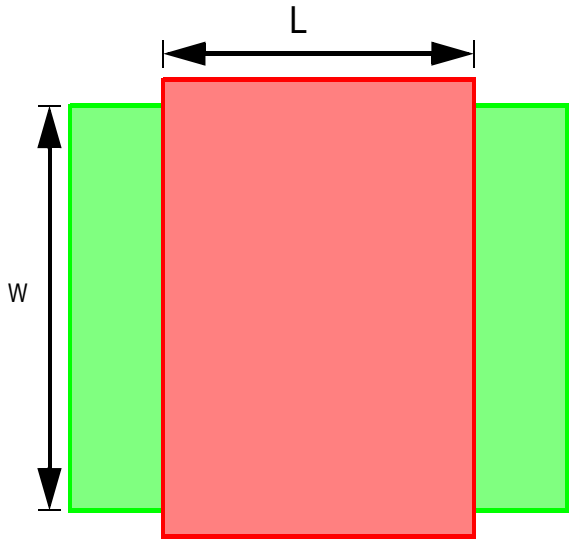
$$C_{gd} = C_{ovl}W \quad \textbf{(3.A12)}$$

Source - Drain junction capacitance (used in SPICE level=3):

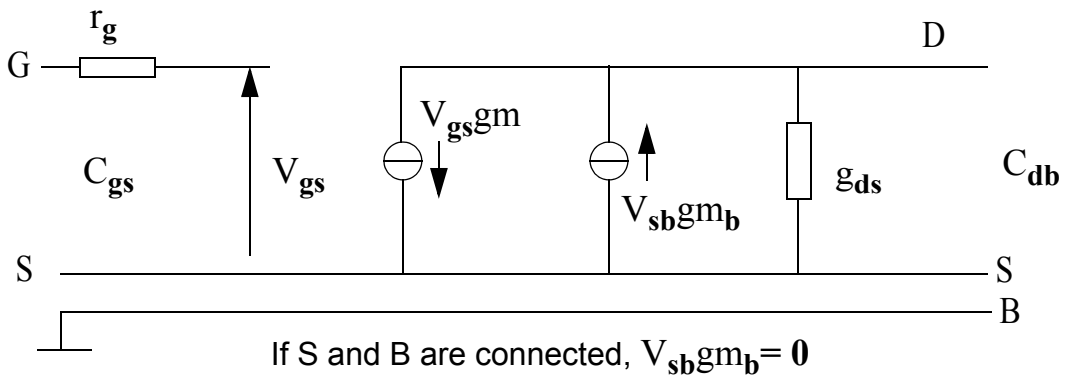
$$C_j = A \cdot CJ\left[1 - \frac{V_j}{PB}\right]^{-MJ} + P \cdot CJSW\left[1 - \frac{V_j}{PB}\right]^{-MJSW} \quad \textbf{(3.A13)}$$

A= area, P=perimeter

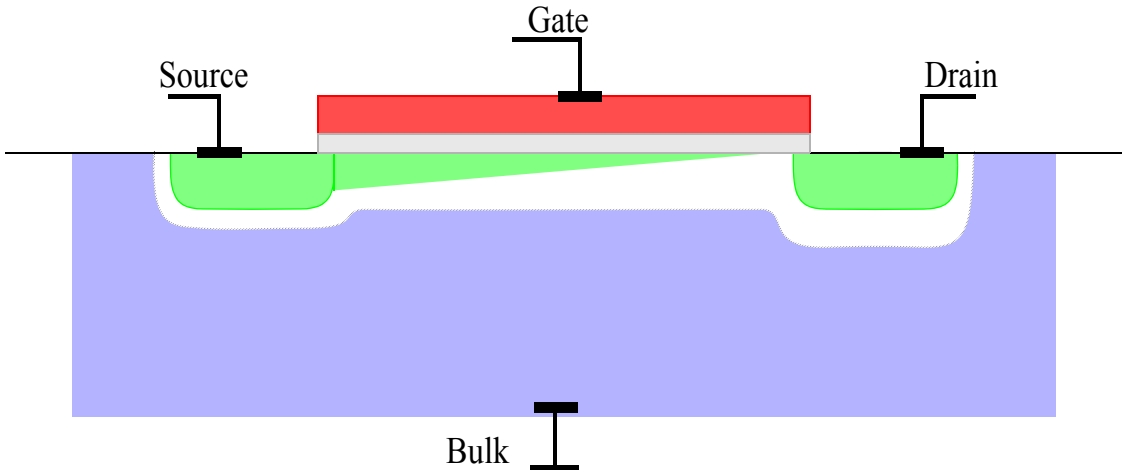
Small signal equivalent



Common Source equivalent



If S and B are connected, $V_{sb}gm_b = 0$

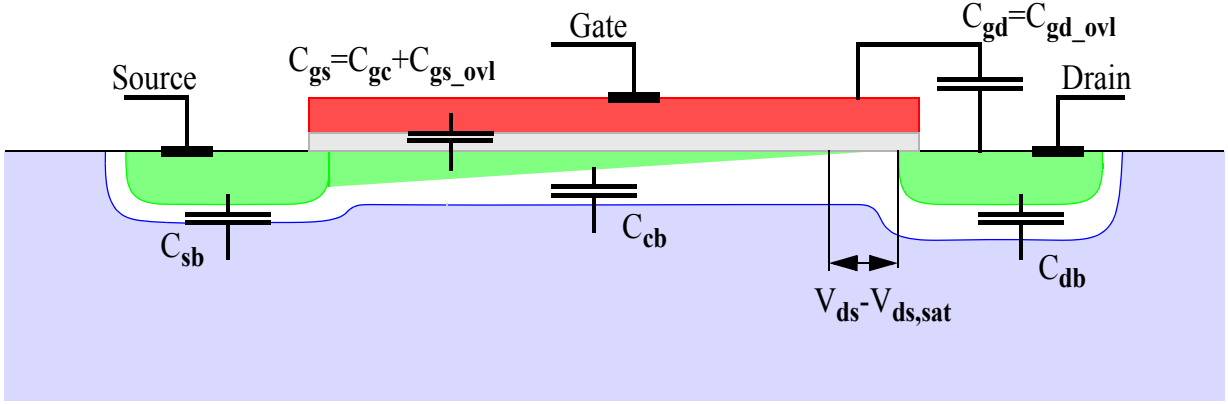


$$g_m = \frac{dI_d}{dV_{gs}} = \sqrt{2\mu C_{ox}\frac{W}{L}I_d}$$

$$g_{mb} = \frac{dI_d}{dV_{sb}} \approx \sqrt{2\mu C_{chbulk}\frac{W}{L}I_d}$$

$$g_{ds} = \frac{dI_d}{dV_{ds}} \approx \lambda I_d$$

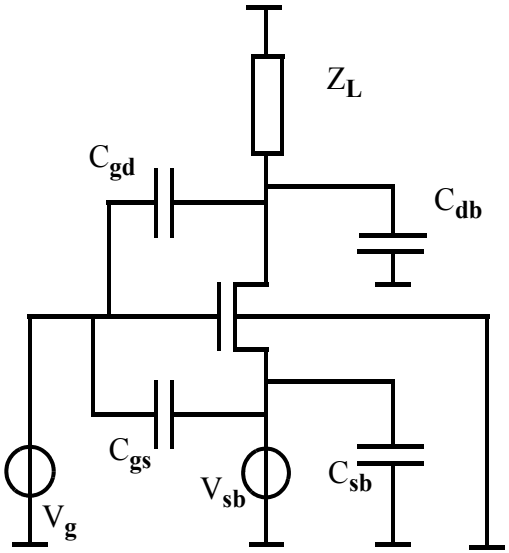
Small signal equivalent (cont.)



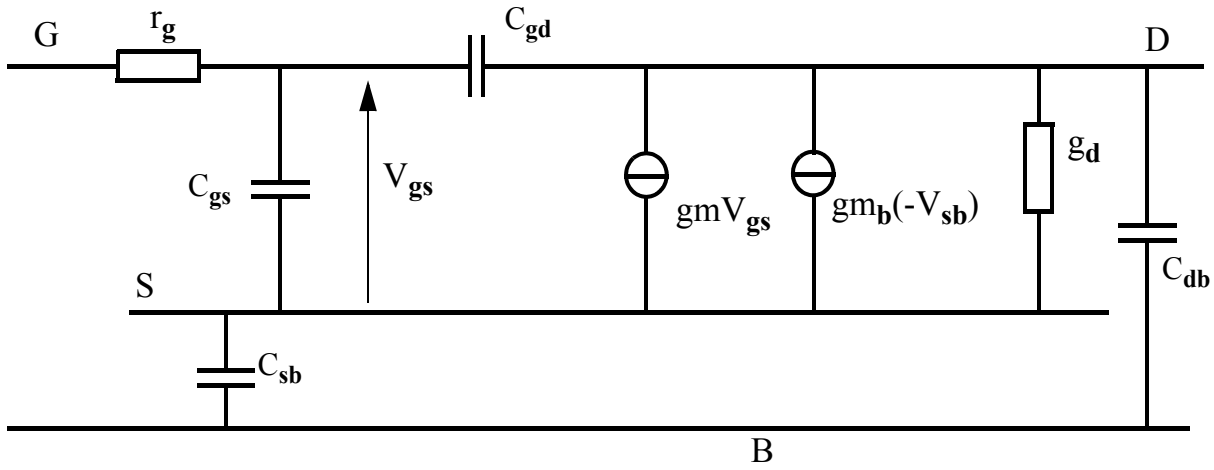
$$C_{gs} = \frac{2}{3}C_{ox}WL + C_{gsovl}$$

$$C_{gd} = C_{gdovl}$$

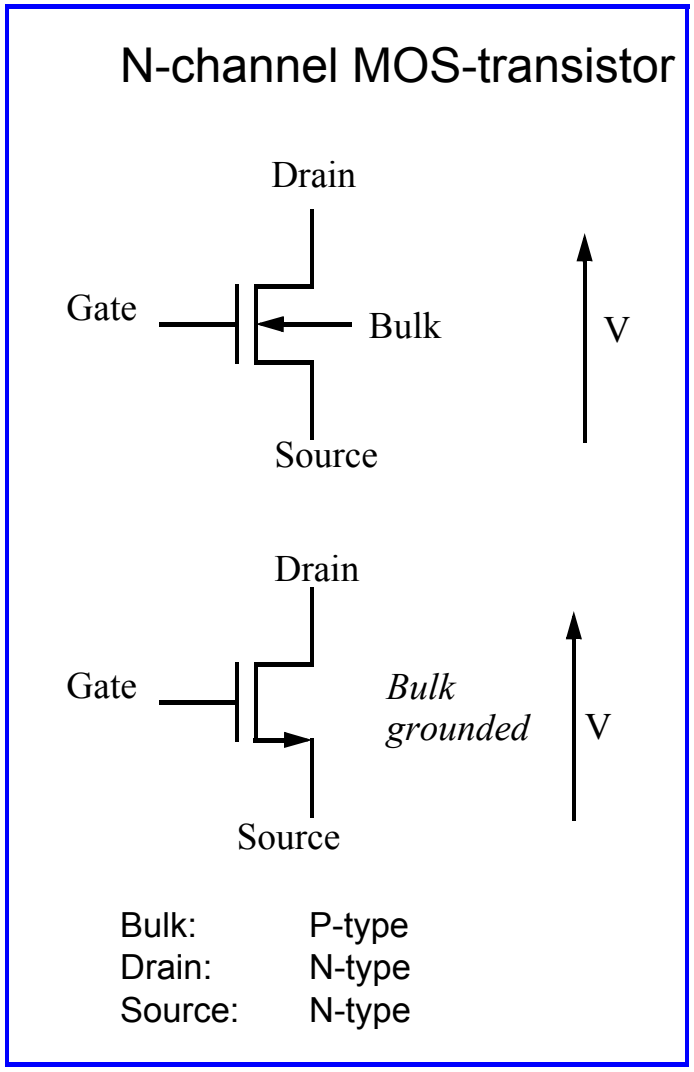
$$C_{db} = \text{Junction}$$

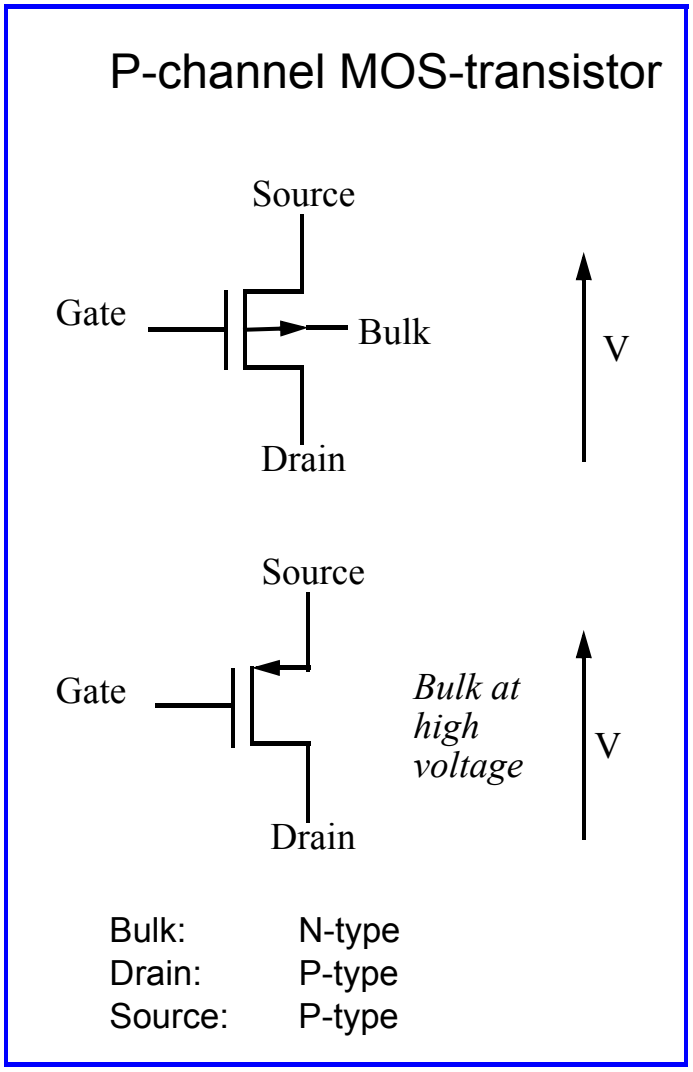


$V_{gs}=V_g-V_{sb}$



Transistor symbols





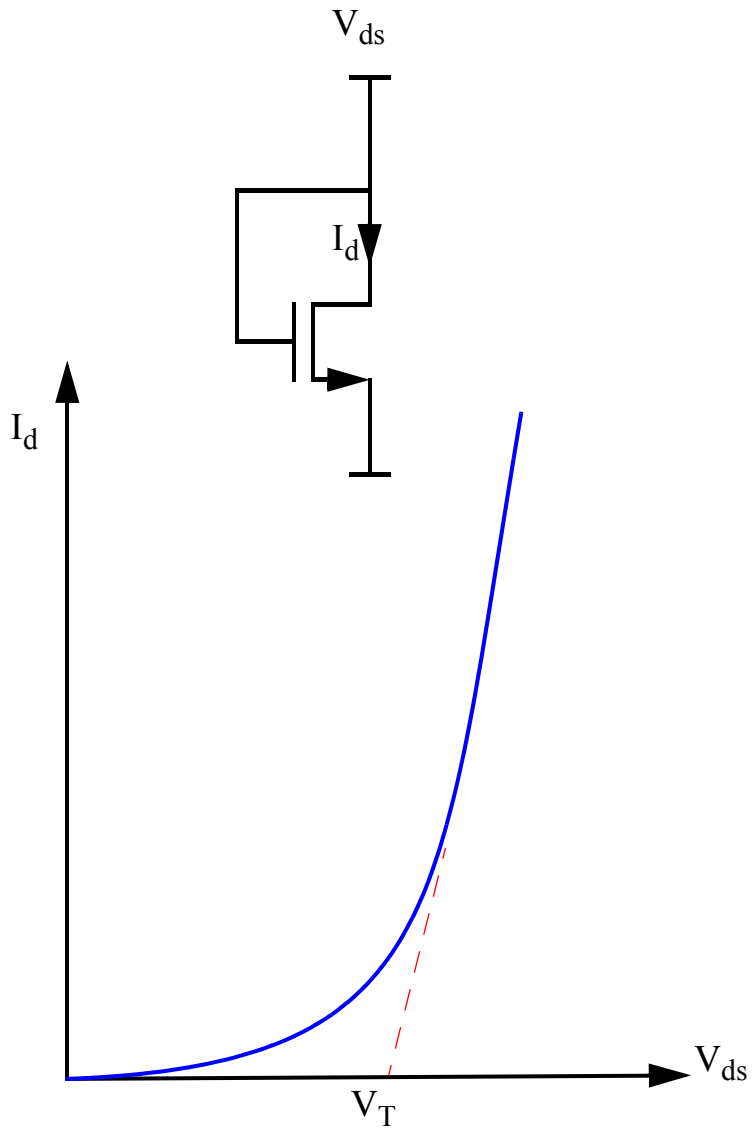
Diode connected transistor

Given that the transistor is in strong inversion,

$$V_{GS} \geq V_T \quad ,$$

it will always be saturated when $V_{GS}=V_{DS}$ (connected)

because the condition: $V_{DS} \geq V_{GS} - V_T$ must be met



Input conductance:

$$g_{inn} \equiv \frac{dI_d}{dV_{ds}} = \frac{dI_d}{dV_{gs}} = g_m = \frac{1}{r_{inn}} \qquad \textbf{(3.A14)}$$

Current mirrors

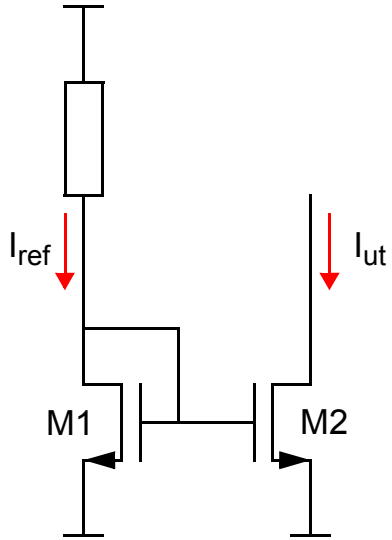
- M1 is always saturated because $V_{ds} = V_{gs} > V_{gs} - V_T$
- Assuming M2 saturated as well

Applying the expression for the drain current:

$$I_d = \frac{\mu_0 C_{ox}}{2}\frac{W}{L}(V_{gs} - V_T)^2(1 + \lambda V_{ds})$$

gives the output current:

$$I_{ut} = \frac{\frac{\mu_0 C_{ox}}{2}\frac{W_2}{L_2}(V_{gs} - V_T)^2(1 + \lambda V_{ds2})}{\frac{\mu_0 C_{ox}}{2}\frac{W_1}{L_1}(V_{gs} - V_T)^2(1 + \lambda V_{ds1})} I_{ref} = \frac{W_2 L_1 (1 + \lambda V_{ds2})}{L_2 W_1 (1 + \lambda V_{ds1})} I_{ref} \qquad \textbf{(3.A15)}$$



Ideally for long channels (λ=0), and when L_1=L_2:

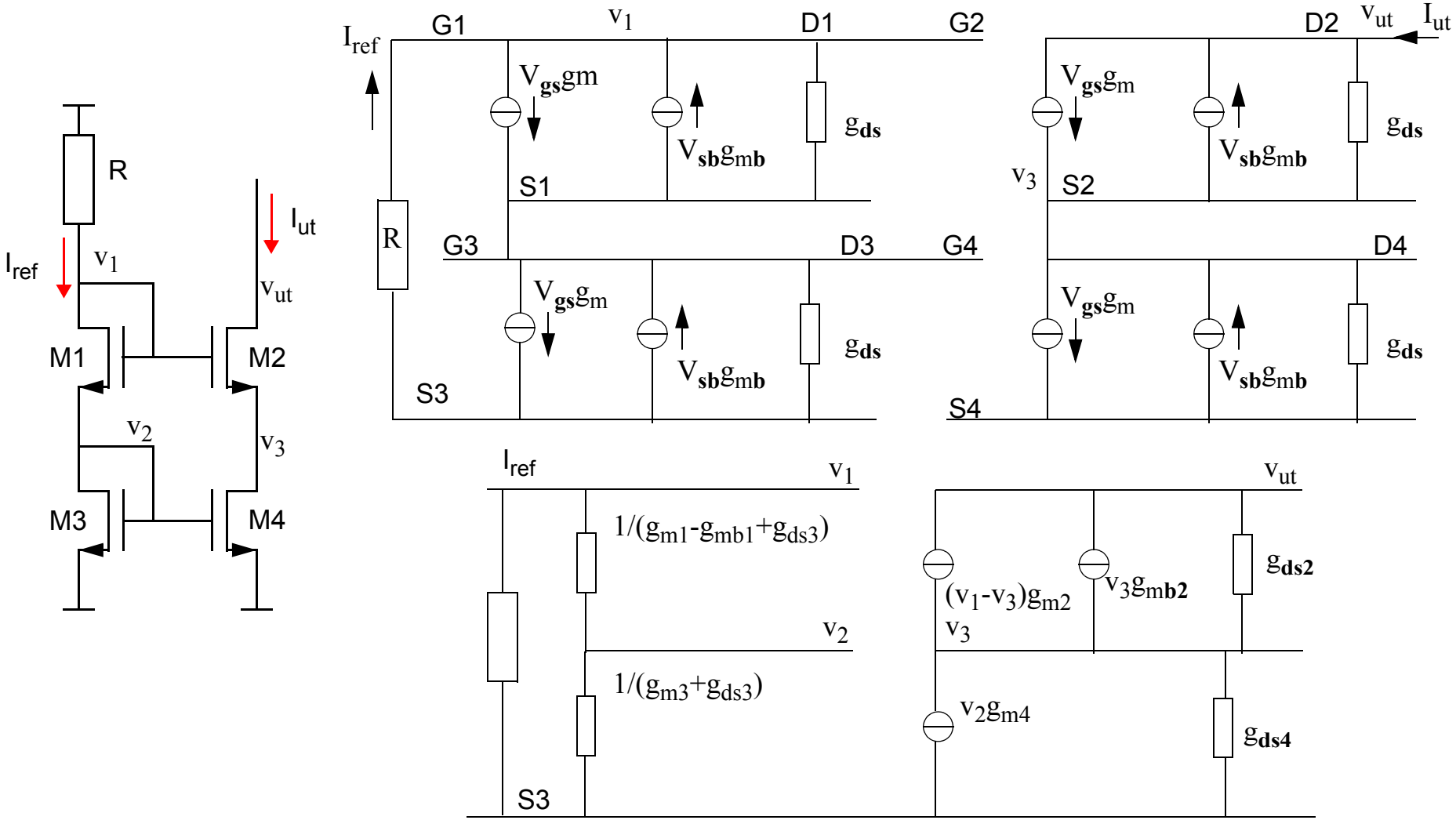
$$I_{ut} = \frac{W_2}{W_1} I_{ref}$$

The simple expression above is inaccurate for short channels due to the final output resistance for M2. Therefore:

$$r_{ut} = \frac{1}{g_{M2}} = \frac{1}{\frac{dI_{d2}}{dV_{ds2}}} = \frac{1}{\frac{\mu_0 C_{ox}}{2}\frac{W}{L}(V_{gs} - V_T)^2 \lambda} = \frac{(1 + \lambda V_{ds})}{\lambda I_d} \approx \frac{1}{\lambda I_d} \qquad \textbf{(3.A16)}$$

Cascoded current mirrors

Have high output resistance



Output resistance $r_{ut} = dv_{ut} / di_{ut}$

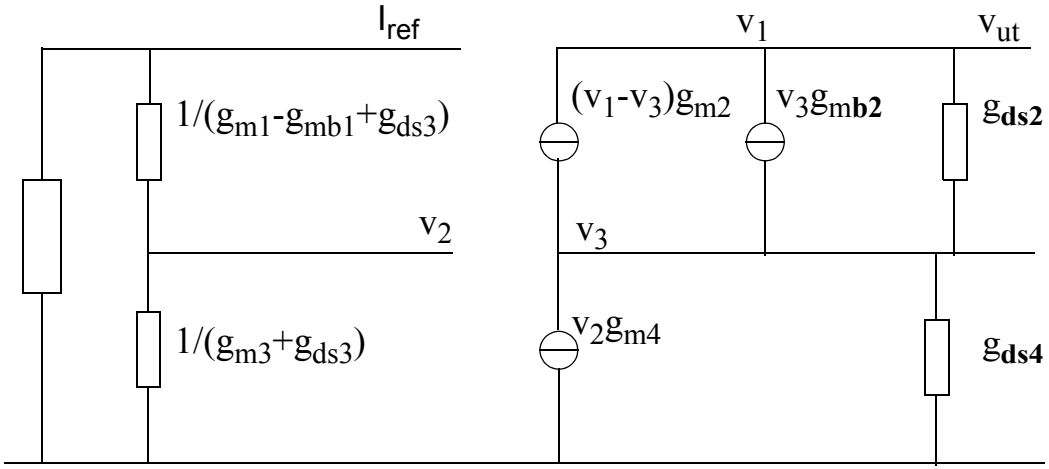
The DC voltages v_1=v_2=0 is zero in a small signal equivalent circuit:

$$i_{ut} - g_{m2}(v_1 - v_3) + g_{mb2}v_3 - g_{ds2}(v_{out} - v_3) = 0 \qquad (a)$$

$$g_{ds4}v_3 + g_{m4}v_2 - g_{m2}(v_1 - v_3) + g_{ds2}(v_3 - v_{ut}) + g_{mb2}v_3 = 0 \qquad (b)$$

Solving (b) for v_3 and replacing v_3 in (a). Reorganizing gives:

$$r_{ut} = \frac{v_{ut}}{i_{ut}} = \frac{g_{m2} + g_{mb2} + g_{ds2} + g_{ds4}}{g_{ds2}g_{ds4}} \approx \frac{g_{m2}}{g_{ds2}g_{ds4}} = \frac{g_{m2}}{g_{ds2}}\frac{1}{\lambda I_{ds}} \qquad \textbf{(3.A17)}$$



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