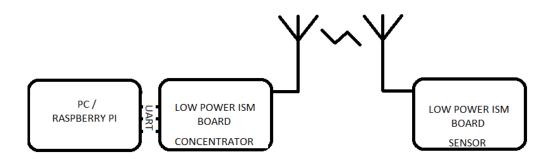
Low Power ISM (It is mandatory to read the entire document should you choose this assignment)

Each Low Power ISM board consists of a microcontroller (MCU), which execute the programmed logic, the sensors and circuits connected to the microcontroller, and an ISM radio running at 868MHz, transmitting and receiving data packets to and from other Low Power ISM boards.

Unique board addresses are generated from the microcontroller production data, and are used as radio addresses.

A complete setup consists of two or more Low Power ISM boards. Only difference between a concentrator board, and a sensor board is the way they are powered, and the code uploaded to the microcontroller.



One board, the concentrator, is communicating to a higher level system through UART (serial port), and the rest of the Low Power ISM boards are battery powered sensor boards, and communicate to the higher level system via the concentrator

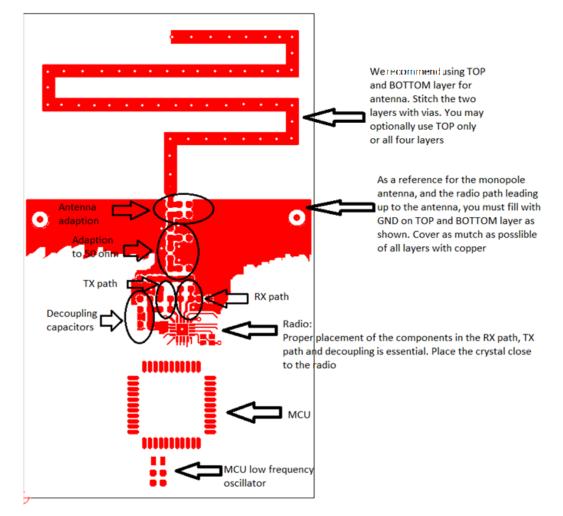
We provide a complete demo setup with where a Raspberry Pi receives data from, and control several Low Power ISM boards, log the data in a database, and display the data on a web page.

You can have a copy of all code, and build a similar system based on the boards you make.

Your assignment will be the following:

- 1) Create a schematic drawing based on the schematics "low_power_ism_v2.pdf" attached at the end of this document
- 2) Including the USB connector is optional
- 3) The rest of the schematics shall be copied as is
- 4) You are encouraged to add a small design of your own either connecting to one of the inputs EXT_1 or EXT_2, to the output EXT_3 or to the I2C bus connecting the microcontroller and the humidity sensor
- 5) Create a layout
- 6) Assemble at least two boards (Assembly day at ELAB)
- 7) Verify that the boards are functional or find eventual errors (Assembly day at ELAB)





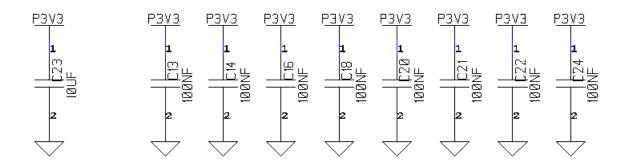
Antenna Layout (MAKE AN EXACT COPY USING A TEMPLATE):

You may set the grid to 1mm while drawing the template for the antenna.

	L1	9.0 mm	Y	43.0 mm
	L2	18.0 mm	X1	63.0 mm
L1 L2	L3	3.0 mm	X2	25.0 mm
+L5	L4	38.0 mm	w	2.0 mm
262	L5	1.0 mm		

Decoupling capacitors:

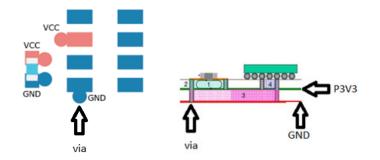
On the POWER page in the schematics, you will find all the P3V3 decoupling capacitors:



All devices using P3V3, shall have a decoupling capacitor placed close to its VCC/GND pins.

You are creating four layer boards, where two copper layers inside the board are reserved for power and ground and should cover the entire board, excluding the antenna area.

All devices being supplied P3V3 should have a P3V3 copper layer and a GND copper layer directly beneath them. In this case, the best option for VCC and GND hook-up for both the device and the capacitor, is by using VIA's directly into to the power layer beneath them through a minimal length, and thus minimal impedance, track.



Note that the via's connecting the capacitor to the inner power layers are located close to each other, and that the distance between the pads and the via's are as short as possible in order to minimize inductance

Excerpt from the si4455 layout guide:

The layout structure of the RF part of the Class-E Direct Tie type matching network is shown in Figure 2.

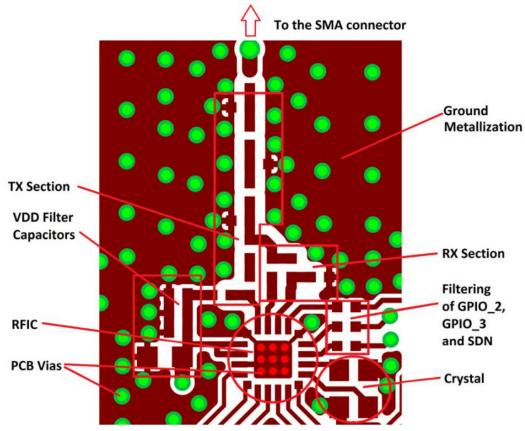


Figure 2. Layout Structure of the RF Part of the Class-E Direct Tie Type Matching Network for Si4455

3.1. Layout Design Guidelines for Si4455 RF IC

Some general rules for designing an RF-related layout for good RF performance:

- Use as large continuous ground plane metallization as possible
- Avoid the separation of the ground plane metallization
- Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins
- Avoid using long and/or thin transmission lines for connecting the components or else, due to its distributed parasitic inductance, some de-tuning effects can occur
- Avoid placing the nearby inductors in the same orientation to reduce the coupling between them
- Use tapered line between transmission lines with different width (i.e., different impedance) to reduce the internal reflections
- Avoid using loops and long wires to obviate resonances

Ensure good VDD filtering by using bypass capacitors (especially at the range of the operating frequency) Layout design guidelines for using the Si4455 RF IC:

The choke inductor (LC) should be placed as close to the TX pin of the RF IC as possible (even if this

means the RX is further away) in order to reduce the series parasitic inductance which increases the voltage peak at the internal drain pin.

- The trace parasitics are very critical in case of the connection of LR2; therefore, the shortest traces possible should be used for connecting LR2 to the TX side.
- The L0 C0 elements should be placed as close to each other as possible, because these elements are the resonant tank of the Class-E matching which has a very strong effect on the RF performance.
- The neighboring matching network components should be placed as close to each other as possible in order to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- By connecting CM1 to the GND metal at the other side of the matching network, the suppression of the double-frequency harmonic could increase even by 5 dB by reducing the coupling between stages of the low pass filter.
- If space allows, the parallel inductor in the RX path (LR1) should be perpendicular to the nearby inductors in the TX path as this will reduce TX to RX coupling.
- Increase the grounding effect in the thermal straps used with capacitors. In addition, thicken the trace near the GND pin of these capacitors. This will minimize series parasitic inductance between the ground pour and the GND pins. Additional vias placed close to the GND pin of capacitors (thus connecting it to the bottom layer GND plane) will further help reduce these effects.

Figure 3 demonstrates the positioning and orientation of the LC, L0, C0, LR1, LR2, and CM1 components on the 4355-PRXB434M (4355CPRXB434M) pico board.

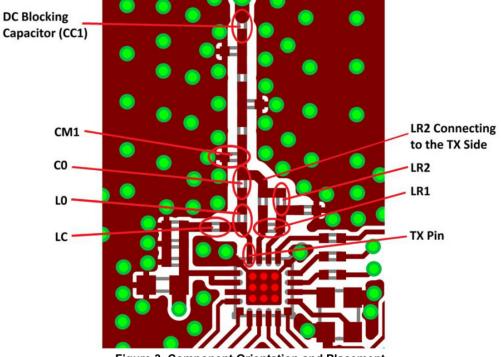
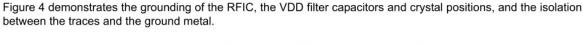
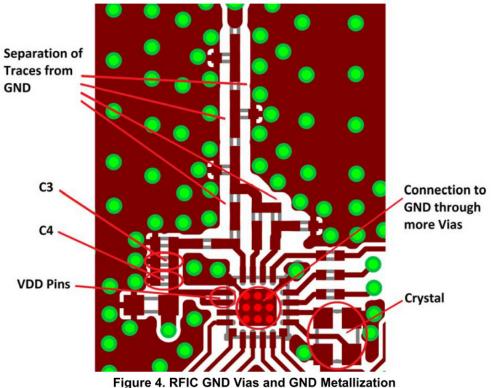


Figure 3. Component Orientation and Placement

- The smaller VDD bypass capacitors (C4 and C3) should be kept as close to the VDD pins as possible.
- The exposed pad footprint for the paddle of the RF IC should use as many vias as possible to ensure good grounding and heatsink capability. In the reference designs there are 9 vias, each with a 12 mil diameter. The paddle ground should also be connected to the top layer GND metal, if possible, to further improve RF grounding; this may be accomplished with diagonal trace connections through the corners of the RFIC footprint.
- The crystal should be placed as close to the RFIC as possible to ensure wire parasitic capacitances are kept as low as possible; this will reduce any frequency offsets that may occur.
- Use at least 0.5 mm separation between traces/pads to the adjacent GND pour in the areas of the matching networks; this will minimize the parasitic fringe capacitance and reduce the detuning effects.





- To achieve good RF ground on the layout, it is recommended to add large, continuous GND metallization on the top layer in the area of the RF section (at a minimum). Better performance may be obtained if this is applied to the entire PCB. To provide a good RF ground, the RF voltage potentials should be equal along the entire GND area as this helps maintain good VDD filtering and also provides a good ground plane for a monopole-type antenna. Gaps ideally should be filled with GND metal and the resulting sections on the top and bottom layers should be connected with as many vias as possible.
- The area under the matching network (on the bottom layer) should be filled with ground metal as it will help reduce/remove the unwanted radiated emissions. Board routing and wiring should not be placed in this region to prevent coupling effects with the matching network. It is also recommended that the GND return path between the GND vias of the TX LPF/Match and the GND vias of the RFIC paddle should not be blocked in any way; the return currents should see a clear unhindered pathway through the GND plane to the back of the RFIC.
- Use 50 Ω grounded coplanar lines where possible for connecting the SMA connector (or the antenna directly) to the matching network to reduce sensitivity to PCB thickness variation. This method will also reduce unwanted radiations and coupling effects. The interconnections between the elements are not considered to be transmission lines as their lengths are much lower than the wavelength and thus their impedance is not critical. As a result, their recommended width is the smallest possible (i.e., equal to the width of the pad of the applied components). In this way, the parasitic capacitances to the ground can be minimized. For the 4455-PCExxDxxxM (4455CPCExxDxxxM) pico board, the only route where the 50 Ω coplanar transmission line is used is between the output of the matching networks and the SMA connector.

How do to make a track/route with 50ohm impedance:

f	119-960 MHz		
Т	0.018-0.035 mm		
Er	4.6		
н	1.5 mm	0.26 m	
G	0.25 mm 0.64 mm		
W	1.26 mm	0.45 mm	
*Note: For the 4-layer PCBs, the thickness between the top and the next inner layer should be taken into account.			

Table 1. Parameters for 50 Ω Grounded Coplanar Lines

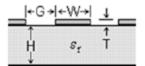
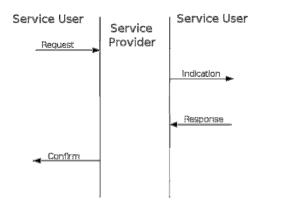


Figure 7. Grounded Coplanar Line Parameters

Communication model for UART and radio messages



UART and radio messages

AES encrypted data **(Data only encrypted when transmitted over the air)**

Current implementation has four different messages:

0x30, Status indication:

		byte
Start of message	0xAF	0
Message id	0x30	1
Senders address	MSB	2
Senders address	LSB	3
Senders message counter	MSB	4
Senders message counter	LSB	5
		6
GPIO input		7
GPIO output status		8
		9
		10
Temperature	MSB	11
Temperature	LSB	12
Humidity	MSB	13
Humidity	LSB	14
		15
		16
CRC-CCITT	MSB	17
CRC-CCITT	LSB	18
End of message	0x5F	19

The sensors send indications to the higher level system (address 0x0000) periodically, when they wake up, and wait a few second for a response before entering sleep again.

0x31 response to a status indication:

When the higher level system receives a status indication from one of the sensors, via the concentrator, it should respond, via the concentrator, with a message where the message id is set to 0x31, and with the address of the sensor in the address fields.

0x33, GPIO set request:

		byte
Start of message	0xAF	0
Message id	0x33	1
Senders address	MSB	2
Senders address	LSB	3
Senders message counter	MSB	4
Senders message counter	LSB	5
		6
GPIO output mask		7
GPIO output values		8
		9
		10
		11
		12
		13
		14
		15
		16
CRC-CCITT	MSB	17
CRC-CCITT	LSB	18
End of message	0x5F	19

0x34 confirmation on GPIO set request:

A GPIO set request is confirmed with a status indication, where the message id is set to 0x34.

Refer to the code for more details.

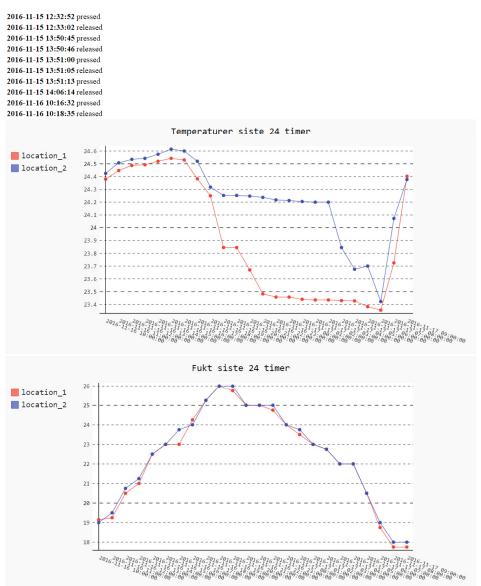
If you decide to use the boards you have made in a setup with a Raspberry Pi, your home server/computer or any other system supporting a UART connection and the possibility to run python scripts, we can provide you with the necessary files to generate a web page similar to this:



Aloha!

Time and date: 2016-11-17 09:52:02

Button status for board with address 0x2075:



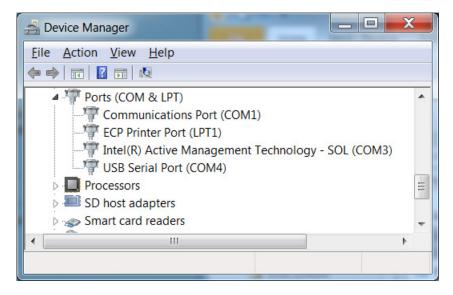
Instructions for setting up a Raspberry Pi :



If you wish to connect your concentrator board to a Windows/Linux machine, you could optionally use this cable, which is pin-compatible with the concentrator pin-out:

http://www.digikey.com/product-detail/en/ftdi-future-technology-devices-international-ltd/TTL-232R-3V3/768-1015-ND/1836393

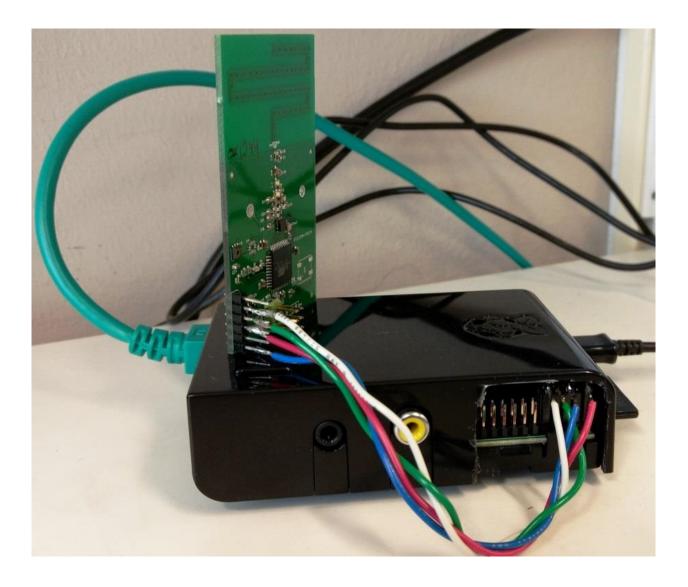
On a windows machine, you would have to look in "Device Manager" to find the correct COM port to use (COM4) in the example below:



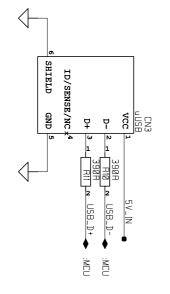
In python you would then connect to the concentrator like this:

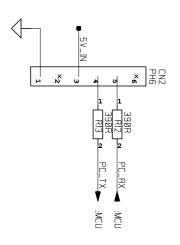
ser = serial.Serial('COM4', 9600, timeout=0.01)

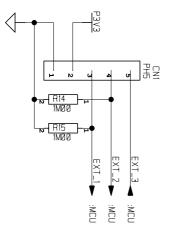
In recent Debian based Linux distributions, you should find a new port like /dev/ttyUSB0 when you plug in the USB/UART translator.



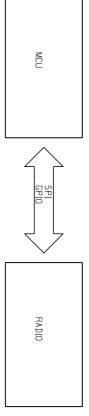
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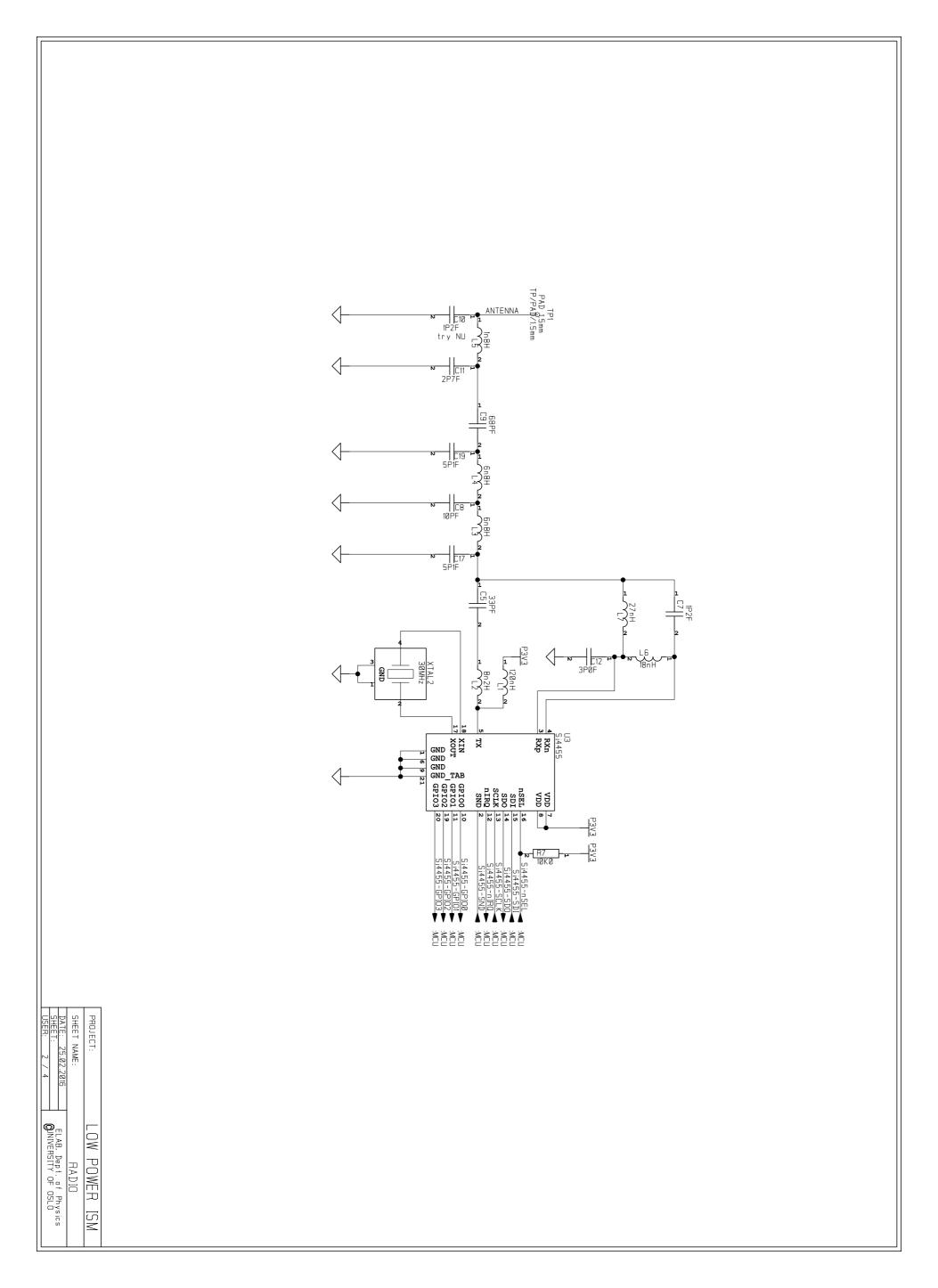








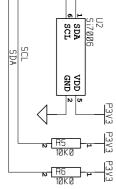
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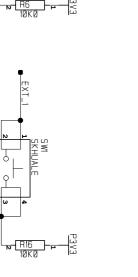


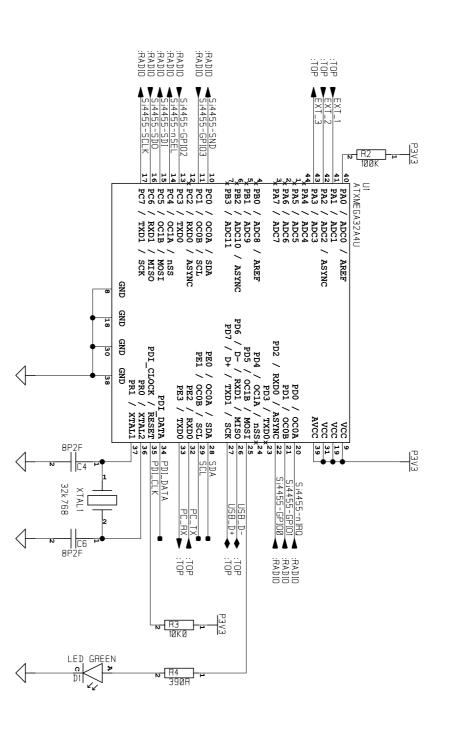




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● PDI_CLK PDI_DATA The second secon

