University of Oslo
Faculty of Mathematics and Natural Sciences

Final Exam in: INF4411/3410, fall 2017
Date of exam: 27-Nov-2016
Time: 09:00-13:00
This examination paper consists of 6 page(s)
Permitted materials: All printed and written including approved (!) calculator

Make sure that your copy of this examination paper is complete before answering.

Read Carefully:

This is the final exam of INF4410 and INF3410, fall 2017. It will contribute 60% towards the final grade, while the other 40% are contributed by the mandatory labs 2 and 3 of the course. The task 2 under chapter 3 is *RESERVED for INF4411 ONLY!* Students that are registered as bachelor students in INF3410 shall *NOT* solve this task! No extra points will be given if they should solve the task!

It is recommended that you read all the tasks before starting with the exam. A good strategy thereafter is to start with the tasks you feel most comfortable with and leave the most difficult ones for last.

It is also recommended to read through all the tasks once more after you have finished, to make sure you have not overlooked anything.

Start a new page for every task you are answering and write your ID-number and task number on the top of all pages you submit. If you use several pages per task also mark the page number next to the task number. Make sure to answer all questions and follow all instructions. Clearly mark your final answers and results (all that are explicitly asked for or instructed to find in a task) with a double underline. Document your deduction of those results and any assumptions you may have had to make.

Note that you may not hand in the original task papers that you are holding now, i.e. do not write any results here but use exclusively the separate sheets of paper that you are going to hand in.

Each question is graded indicating the weight when grading.

Chapter 1

Task 1 (2p): Derive the Thévenin equivalent (drawn on the right of the figure) of the circuit on the left of figure 1, i.e. find the values of the DC voltage, the peak-to-peak amplitude and output resistance in point 1.

Table 1.5 MOSFET parameters representative of various CMOS technologies and used for rough hand calculations in this text.

	0.8 μm		0.35 μm		0.18 μm		45 nm	
Technology	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
μC_{ox} ($\mu A/V^2$)	92	30	190	55	270	70	280	70
V_{t0} (V)	0.80	–0.90	0.57	–0.71	0.45	–0.45	0.45	–0.45
$\lambda \cdot L$ (μm/V)	0.12	0.08	0.16	0.16	0.08	0.08	0.10	0.15
C_{ox} ($fF/\mu m^2$)	1.8	1.8	4.5	4.5	8.5	8.5	25	25
t_{ox} (nm)	18	18	8	8	5	5	1.2	1.2
n	1.5	1.5	1.8	1.7	1.6	1.7	1.85	1.85
θ (1/V)	0.06	0.135	1.5	1.0	1.7	1.0	2.3	2.0
m	1.0	1.0	1.8	1.8	1.6	2.4	3.0	3.0
$C_{ov}/W = L_{ov}C_{ox}$ (fF/μm)	0.20	0.20	0.20	0.20	0.35	0.35	0.50	0.50
$C_{db}/W \approx C_{sb}/W$ (fF/μm)	0.50	0.80	0.75	1.10	0.50	0.55	0.45	0.50

Table 1.5
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Table 1: Typical process parameters

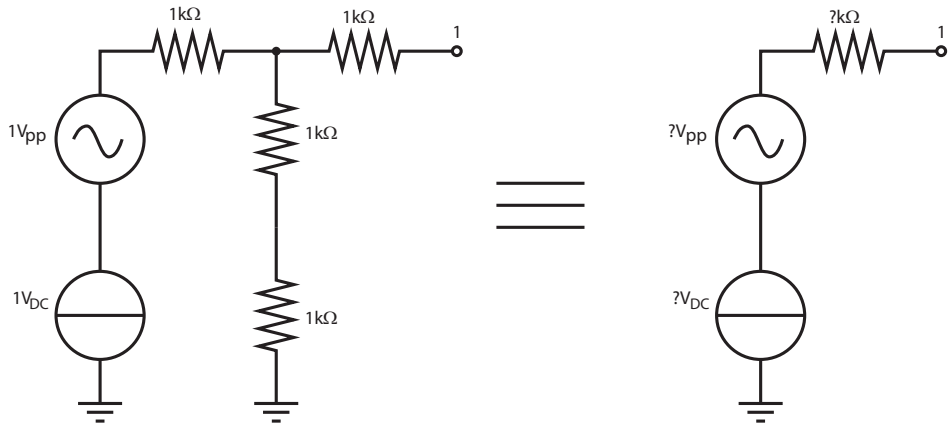


Figure 1: Circuit for finding Thévenin equivalent in task 1

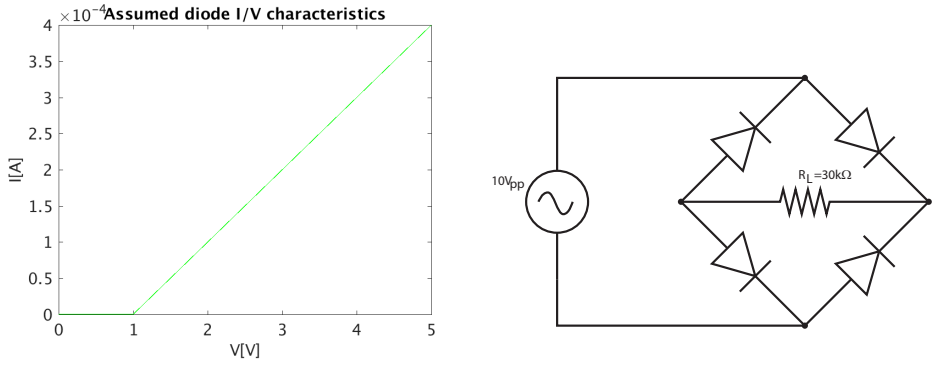


Figure 2: Left: diode model to be used for task 2. Right: Full wave rectifier with resistive load

Chapter 3 (only for INF4411!)

The task 2 of chapter 3 is mandatory for students having registered as master students to course INF4411, and are NOT(!) to be solved for bachelor students registered to course INF3410. No extra point are to be gained for bachelor students registered to course INF3410 by solving this task under chapter 3!

Task 2 (only INF4411, 4p): Assume the diode I/V relationship shown on the left of figure 2. Note that in contrast to the 'constant-voltage-drop-model' in the book, this model shows a resistive behaviour once the threshold is reached. The right side of figure 2 shows a full wave rectifier. The input shall be 10Vpp, i.e. the difference of the two terminals goes from +5V to -5V. The period of the sine wave voltage source is 1s. Sketch the voltage accross $R_L = 30\text{k}\Omega$ over a period of 4 seconds. What's the peak-to-peak value of that voltage?

Chapter 5

Task 3 (3p): You want to use a NFET transistor with the 0.8μm process parameters described in table 1 in its Triode region. Its source is connected to Gnd and the gate voltage V_{GS} at a fixed voltage. What minimal V_{GS} do you need such that the transistor remains operating in the Triode region for drain voltages V_{DS} of up to 3.0V? What transistor dimension $\frac{W}{L}$ is required if the equivalent drain-source resistance for drain voltages close to Gnd (!) should be $10\text{k}\Omega$?

Chapter 6

Task 4 (2p): For the NMOS CS amplifier with a load resistor as depicted in figure 3, using the parameters of a 0.18μm process as given in table 1, and a width of $W = 1.8\mu$m, a length of $L = 0.36\mu$m, a load resistance of $R_D = 20\text{k}\Omega$, and a Vdd of 1.2V, determine its 'active' region, i.e. the coordinates of points A and B in the graph. (Ignore any channel length modulation effect and slope factor $n = 1$!)

Task 5 (2p): The book does not explain how to find the coordinates of B in *weak inversion*. (Note: you can say that point A does not make sense in weak

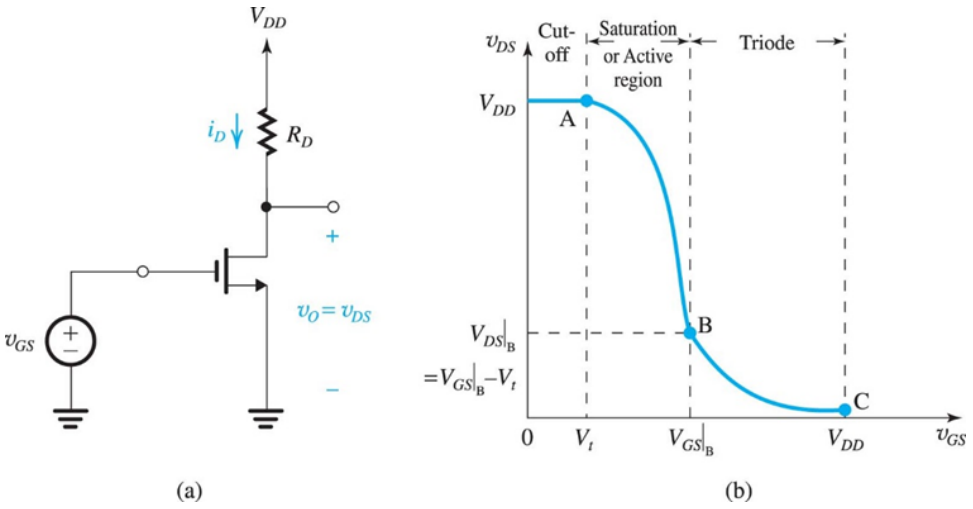


Figure 3: (a) An NMOS amplifier and (b) its voltage transfer characteristics

inversion or that it would be to the right of point B.) Deduce an expression for $V_{GS|B}$ and $V_{DS|B}$ in dependence of R_D, Vdd and transistor parameters in weak inversion! Assume that the rule for weak inversion for the transistor to stay in its active region/saturation applies: $V_{sat} \approx 4V_T$ where $V_T \approx 26$mV is the thermal voltage! (Ignore any channel length modulation effect and slope factor $n = 1$!)

Chapter 7

Task 6 (3p): Given the current steering circuit in figure 4 and using the parameters of the 0.18μm process in table 1 and a supply of Vdd=1.2V, you shall design the circuit such that I_{ref} is 30μA. The widths W of both transistors shall be equal and the lengths L of both transistors shall be equal, thus $I_2 = I_{ref}$. L shall be 540nm. What is the minimum width W that you can choose such that the voltage swing on the output (i.e. the drain of Q_2) shall be at least from 0.6V to Vdd? For that W, what resistance R do you need? (Ignore any channel length modulation effect and slope factor $n = 1$!)

Chapter 8

Task 7 (3p): Figure 5 shows a transconductance amplifier receiving but the same common mode input V_{CM} on both inputs. Assume that all transistors have the same width W and the same length L and that they operate in strong inversion. Derive an expression for the minimum and maximum V_{CM} in dependency of V_{OVn},V_{OVp}, Vdd, I, V_{tn}, and V_{tp} (i.e. no other variables, but you might not need *all* of these), such that all transistors remain in the active region of operation. Note that we shall define V_{OVn} to be the overdrive voltage of Q_1 and Q_2 and V_{OVp} the overdrive voltage of Q_3 and Q_4 when all transistors are in the active region/saturation.

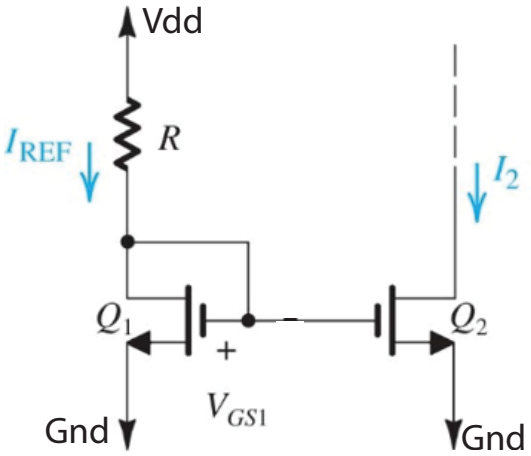


Figure 4: Current steering circuit for task6

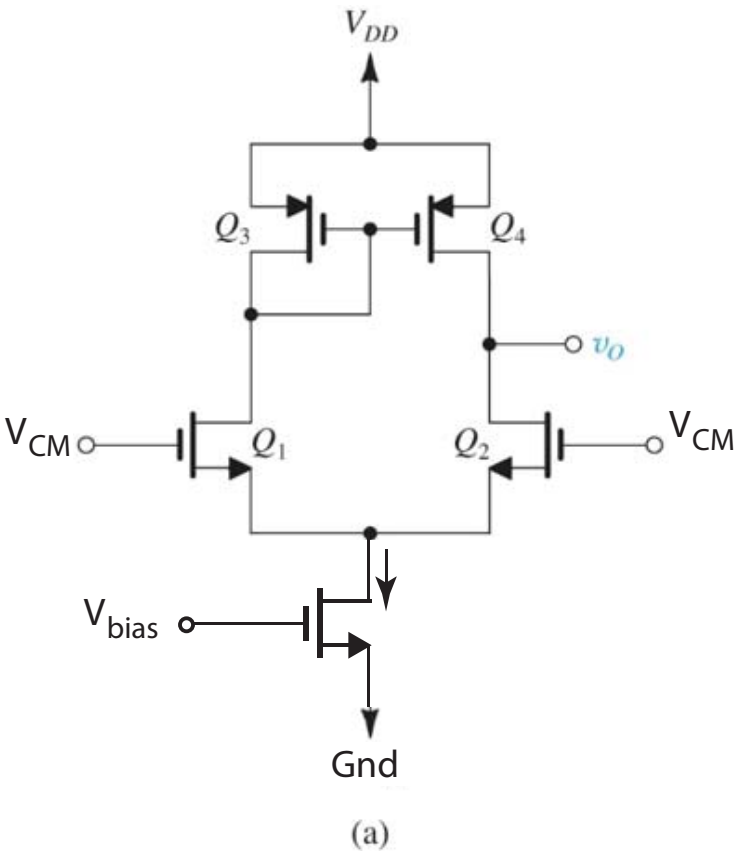


Figure 5: Transconductance amplifier with current mirror for common mode input range determination in task 7

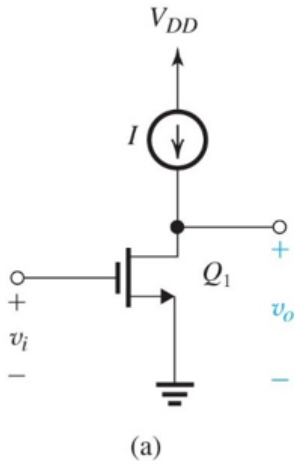


Figure 6: CS amplifier with ideal current source

Chapter 9

Task 8 (4p): Design a CS gain stage using an nFET and the parameters of the 0.18μm process from table 1 (but assume $n = 1.0$ and $C_{gd} = 0$!) with a gain-bandwidth product of 10MRad (i.e. $10^7/(2\pi)$Hz), a DC gain $A_0 = 100$ and a drain current $I_D = 10\mu$A. Make the following assumptions: 1) there is a load capacitance $C_L = 10$pF at the output and the input signal source is an ideal voltage source, i.e. the signal source has zero output resistance and C_L is dominating the frequency behaviour, 2) an ideal current source as load providing I_D, i.e. only r_o of the nFET sets the total resistive load (like in figure 6) . Determine the length L of the transistor.

Chapter 15

Task 9 (4p): Compute the propagation delays for high to low t_{PHL} and low to high t_{PLH} transitions of an inverter using the parameters of the 0.18μm process from table 1, a Vdd of 1.2V, and the method in the book on pages 1265 to 1267, i.e. where an average current is deduced from the current at the start of the transistion when the drain voltage is at the power rail, and the current at the end of the transistion when the drain voltage is at Vdd/2. Assume that all transistors have width $W = 540$nm and length $L = 180$nm and that the inverter drives an identical inverter.

Transfer Functions and Bode Plots

Task 10 (2p): Sketch the Bode plot for transfer function:

$$A(s) = 100\frac{1 - \frac{s}{10^7}}{(1 + \frac{s}{10^4})^2}$$

Let it cover the interval $\omega \in [10^0, 10^9]$ on the x-axis.