University of Oslo
Faculty of Mathematics and Natural Sciences

Final Exam in: INF4411/3410, fall 2017
Date of exam: 27-Nov-2016
Time: 09:00-13:00
This examination paper consists of * page(s)
Permitted materials: All printed and written including approved (!) calculator

Make sure that your copy of this examination paper is complete before answering.

Read Carefully:

This is the final exam of INF4410 and INF3410, fall 2017. It will contribute 60% towards the final grade, while the other 40% are contributed by the mandatory labs 2 and 3 of the course. The task * under chapter 3 is *RESERVED for INF4411 ONLY!* Students that are registered as bachelor students in INF3410 shall *NOT* solve this task! No extra points will be given if they should solve the task!

It is recommended that you read all the tasks before starting with the exam. A good strategy thereafter is to start with the tasks you feel most comfortable with and leave the most difficult ones for last.

It is also recommended to read through all the tasks once more after you have finished, to make sure you have not overlooked anything.

Start a new page for every task you are answering and write your ID-number and task number on the top of all pages you submit. If you use several pages per task also mark the page number next to the task number. Make sure to answer all questions and follow all instructions. Clearly mark your final answers and results (all that are explicitly asked for or instructed to find in a task) with a double underline. Document your deduction of those results and any assumptions you may have had to make.

Note that you may not hand in the original task papers that you are holding now, i.e. do not write any results here but use exclusively the separate sheets of paper that you are going to hand in.

Each question is graded indicating the weight when grading.

Chapter 1

Task * (*p): Derive the Thévenin equivalent (drawn on the right of the figure) of the circuits A and B on the left of figure 1, i.e. find the values of the DC voltage, the peak-to-peak amplitude and output resistance in point 1 for both case A and B.

Solution:

Table 1.5 MOSFET parameters representative of various CMOS technologies and used for rough hand calculations in this text.

	0.8 μm		0.35 μm		0.18 μm		45 nm	
Technology	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
μC_{ox} ($\mu A/V^2$)	92	30	190	55	270	70	280	70
V_{t0} (V)	0.80	–0.90	0.57	–0.71	0.45	–0.45	0.45	–0.45
$\lambda \cdot L$ (μm/V)	0.12	0.08	0.16	0.16	0.08	0.08	0.10	0.15
C_{ox} ($fF/\mu m^2$)	1.8	1.8	4.5	4.5	8.5	8.5	25	25
t_{ox} (nm)	18	18	8	8	5	5	1.2	1.2
n	1.5	1.5	1.8	1.7	1.6	1.7	1.85	1.85
θ (1/V)	0.06	0.135	1.5	1.0	1.7	1.0	2.3	2.0
m	1.0	1.0	1.8	1.8	1.6	2.4	3.0	3.0
$C_{ov}/W = L_{ov}C_{ox}$ (fF/μm)	0.20	0.20	0.20	0.20	0.35	0.35	0.50	0.50
$C_{db}/W \approx C_{sb}/W$ (fF/μm)	0.50	0.80	0.75	1.10	0.50	0.55	0.45	0.50

Table 1.5
© John Wiley & Sons, Inc. All rights reserved.

Table 1: Typical process parameters

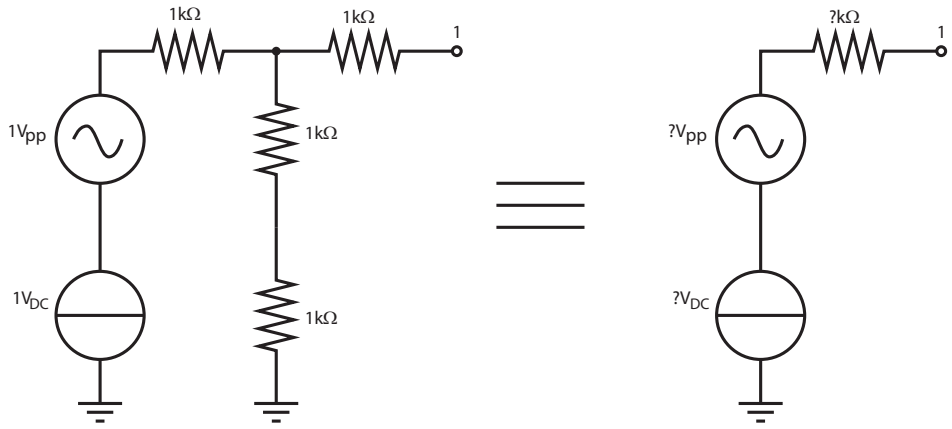


Figure 1: Circuit for finding Thévenin equivalent in task 1

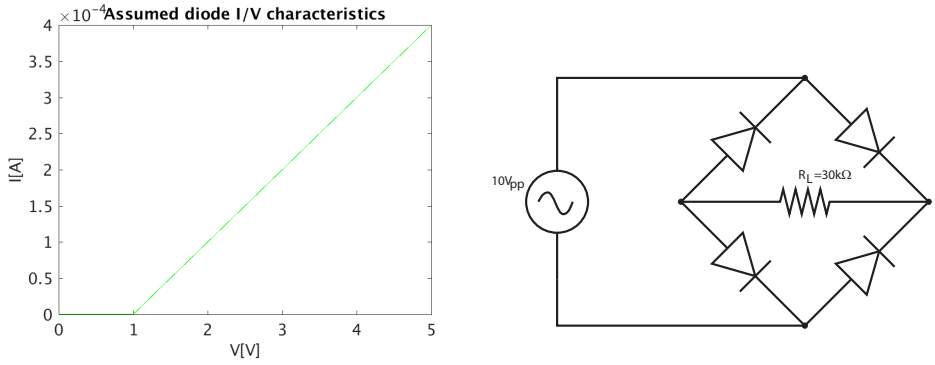


Figure 2: Left: diode model to be used for task *. Right: Full wave rectifier with resistive load

voltage is down-divided by 2/3. Output resistance is

$$(1\text{k}\Omega||2\text{k}\Omega) + 1\text{k}\Omega = (1000 * 2000)/(1000 + 2000) + 1000 = 1.67\text{k}\Omega = 5/3\text{k}\Omega$$

Chapter 3 (only for INF4411!)

The task * of chapter 3 is mandatory for students having registered as master students to course INF4411, and are NOT(!) to be solved for bachelor students registered to course INF3410. No extra point are to be gained for bachelor students registered to course INF3410 by solving this task under chapter 3!

Task * (only INF4411, *p): Assume the diode I/V relationship shown on the left of figure 2. Note that in contrast to the 'constant-voltage-drop-model' in the book, this model shows a resistive behaviour once the threshold is reached. The right side of figure 2 shows a full wave rectifier. The period of the sine wave voltage source is 1s. Sketch the voltage across $R_L = 30\text{k}\Omega$ over a period of 4 seconds. What's the peak-to-peak value of that voltage?

Solution: The diode 'subtract' 1V each from the voltage that the load resistor R_L sees and then act as 10kΩ resistors leading to a resistive division where 3/5 of the voltage is across R_L. So the maximum voltage accross is 3*3/5V=1.8V. The waveform is depicted in figure 3.

Chapter 5

Task * (*p): You want to use a NFET transistor with the 0.8μm process parameters described in table 1 in its Triode region. Its source is connected to Gnd and the gate voltage V_{GS} at a fixed voltage. What minimal V_{GS} do you need such that the transistor remains operating in the Triode region for drain voltages V_{DS} of up to 3.0V? What transistor dimension $\frac{W}{L}$ is required if the equivalent drain-source resistance for drain voltages close to Gnd (!) should be 10kΩ?

Solution: V_{tn} is 0.8V and V_{OV} needs to be 3.0, so V_{GS} needs to be 3.8V.
Then for small V_{DS}:

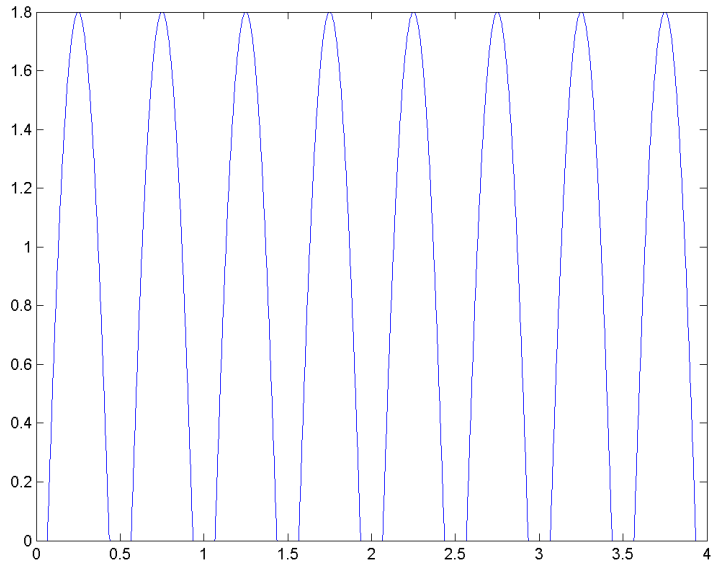


Figure 3: solution plot

$$
\begin{aligned}
r_{ds} &= 1e4\Omega \\
&= \frac{1}{k_n V_{OV}} \\
&= \frac{1}{\mu C_{ox} \frac{W}{L} V_{OV}} \\
&= \frac{1}{92e-6 * \frac{W}{L} * 3.0} \\
&\Rightarrow \\
\frac{W}{L} &= \frac{1}{92e-6 * 1e4 * 3.0} \\
&= 0.36
\end{aligned}
$$

With the wrong process, 0.18um:

$$
\begin{aligned}
\frac{W}{L} &= \frac{1}{270e-6 * 1e4 * 3.00} \\
&= 0.1235
\end{aligned}
$$

Chapter 6

Task * (*p): For the NMOS amplifier with a load resistor as depicted in figure 4, using the parameters of a 0.18μm process as given in table 1, and a width of $W = 1.8\mu$m, a length of $L = 0.36\mu$m, a load resistance of $R_D = 20$kΩ, and

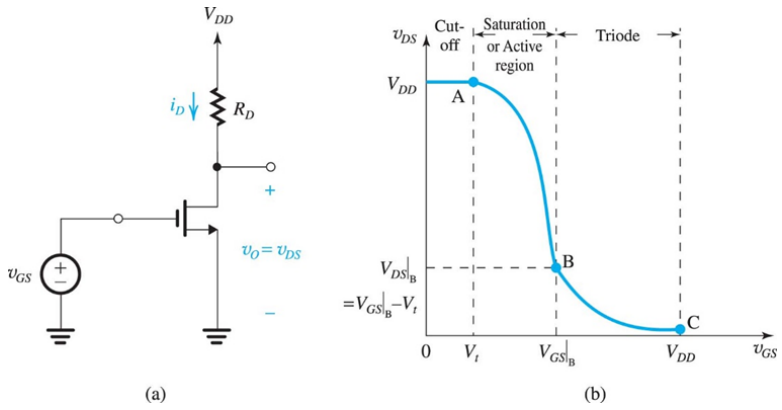


Figure 4: (a) An NMOS amplifier and (b) its voltage transfer characteristics

a Vdd of 1.2V, determine its 'active' region, i.e. the coordinates of points A and B in the graph. (Ignore any channel length modulation effect and slope factor $n = 1$!)

Task * (*p): The book does not explain how to find the coordinates of B in *weak inversion*. (Note: you can say that point A does not make sense in weak inversion or that it would be to the right of point B.) What is the minimum resistance R_D to ensure that the transistor (with the above parameters) operates still in weak inversion as your reach point B? Deduce an expression for $V_{GS|B}$ and $V_{DS|B}$ in dependence of R_D, Vdd and transistor parameters in weak inversion! Hint: The current a transistor supplies at the exact transition between weak and strong inversion, i.e. when $V_{OV} = 0$, is approximately $\frac{I_S}{2} = k_n {V_T}^2$ where $V_T \approx 26$mV is the thermal voltage. (Ignore any channel length modulation effect and slope factor $n = 1$!)

Solution:
A is at (V_{tn}, Vdd) i.e. $(0.45\text{V}, 1.2\text{V})$
B:

$$I = (Vdd - V_{OV})\frac{1}{R_D} = \frac{1}{2}k_n V_{OV}^2$$
$$\Rightarrow$$
$$(Vdd - V_{OV}) = R_D\frac{1}{2}k_n V_{OV}^2$$
$$0 = R_D\frac{1}{2}k_n V_{OV}^2 + V_{OV} - Vdd$$
$$V_{OV} = \frac{-1 \pm \sqrt{1 + 2R_D k_n Vdd}}{k_n R_D}$$

Keep only the positive result:

$$k_n = 5 * 270e - 6$$
$$R_D = 2e4$$
$$k_n R_D = 27$$
$$V_{OV} = (sqrt(2 * 27 * 1.2 + 1) - 1)/27 = 0.2634\text{V}$$

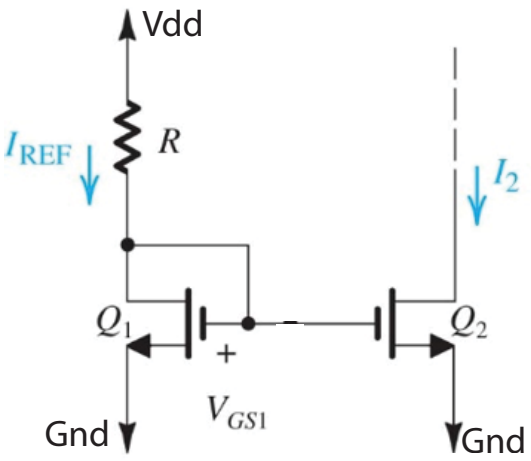


Figure 5: Current steering circuit for task*

And

$$V_{DS|B} = V_{OV} = 0.2634V$$
$$V_{GS|B} = V_{tn} + V_{OV} = 0.7134V$$

For the second task, in weak inversion $V_{DS} \approx 4V_T = 104mV$ so $V_{DS|B} = 104\text{mV}$

$$I = 2k_n V_T^2 e^{V_{OV|B}} = (Vdd - 4V_T)\frac{1}{R_D}$$
$$V_{OV|B} = \ln(Vdd - 4V_T) - \ln(R_D 2k_n V_T^2)$$

And minmum R_D:

$$(Vdd - 4V_T)\frac{1}{R_D} = k_n {V_T}^2$$
$$R_D = \frac{Vdd - 4V_T}{k_n {V_T}^2}$$
$$= 1.096/5/250e-6/26e-3^2 = 1.297\text{M}\Omega$$

Chapter 7

Task * (*p): Given the current steering circuit in figure 5 and using the parameters of the 0.18μm process in table 1 (at the start of the exam sheets), but neglecting the slope factor n (i.e. $n = 1$) and channel length modulation with a supply of Vdd=1.2V, you shall design the circuit such that I_{ref} is 30μA. The two width W of the two transistors shall be equal and the two lengths L of both transistors shall also be equal, thus $I_2 = I_{ref}$. L shall be 540nm. What is the minimum width W that you can choose such that the voltage swing on the output (i.e. the drain of Q_2) shall be at least from 0.6V to Vdd? For that W, what resistance R do you need?

Solution: V_{OV} needs to be at least 0.6V for a minimum width transistor. So $V_{GS} = 1.05$ and thus the voltage drop on R is $V_R = 0.15$. So $R = 0.15/30e{-}6 = 5\text{k}\Omega$

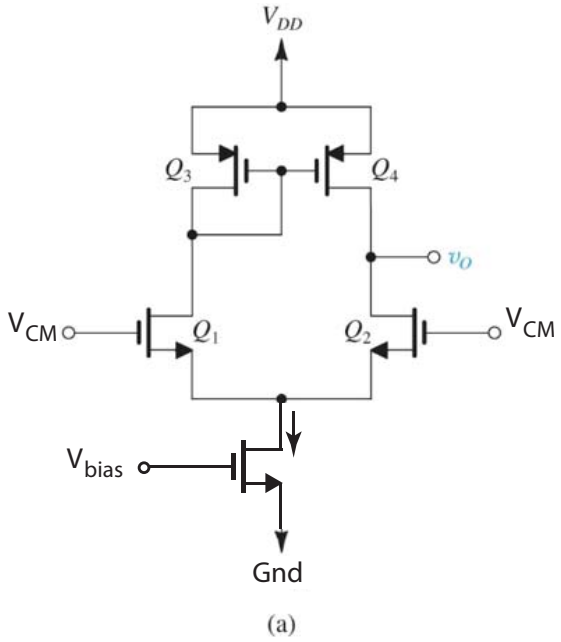


Figure 6:

$$
\begin{aligned}
I_D &= \frac{1}{2} k_n V_{OV}^2 \\
&\Rightarrow \\
k_n &= \frac{2I_D}{V_{OV}^2} = 2 * 30e-6/0.6^2 = 1.67e-4e-5 \\
&= \frac{W}{L} \mu C_{ox} \\
&\Rightarrow \\
W &= Lk_n/\mu C_{ox} = 540e-9 * 1.67e-4/270e-6 = 5.56e-8 = 334nm
\end{aligned}
$$

Chapter 8

Task * (*p): Figure 6 shows a transconductance amplifier receiving but the same common mode input V_{CM} on both differential inputs. Assume that all transistors have the same width W and the same length L and that they operate in strong inversion. Derive an expression for the minimum and maximum V_{CM} in dependency of V_{OV}, Vdd, I, V_{tn}, and V_{tp} (i.e. no other variables, but you might not need *all* of these), such that all transistors remain in the active region of operation. Note that we shall define V_{OV} to be the overdrive voltage of Q_1 and Q_2 when all transistors are in saturation.

Solution: For the minimum one has to consider that it needs to be one V_{GS} above the overdrive voltage required on the bias-transistor, and with the same dimensions as the others this needs to be $\sqrt{2}$ bigger than V_{OV} on Q_1 and Q_2

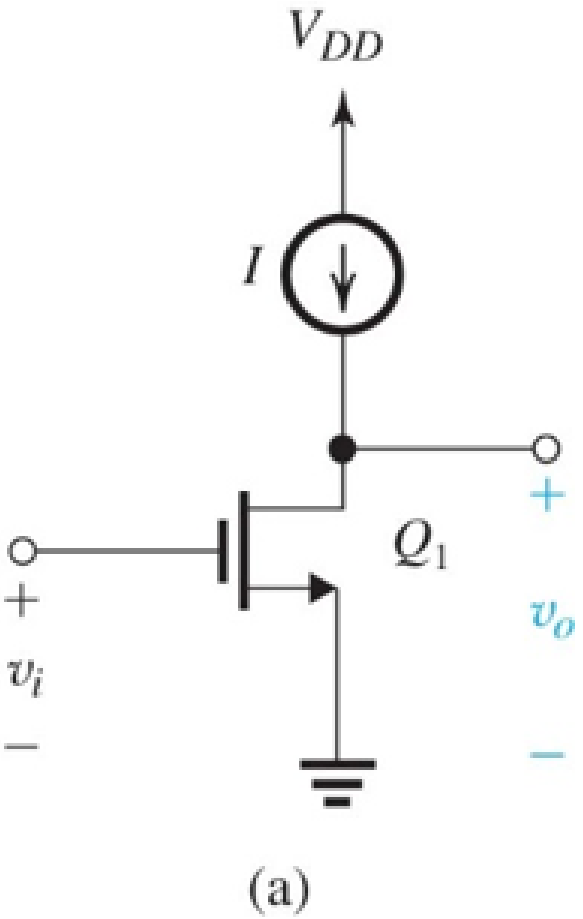


Figure 7: CS amplifier with ideal current source

$$V_{cmMin} = \sqrt{2}V_{OV} + V_{OV} + V_{tn}$$

For the maximum one has to consider the minimum voltage accross the diode connected transistor in the current mirror, i.e. $V_{OVp} + V_{tp}$. Then the V_{CM} cann be V_{tn} above that such that the source of Q_1 is still V_{OVn} below that

$$V_{cmMax} = Vdd - V_{OVp} - V_{tp} + V_{tn}$$

Chapter 9

Task * (*p): Design a CS gain stage using an nFET and the parameters of the 0.18μm process from table 1 (but assume $n = 1.0$ and $C_{gd} = 0$!) with a gain-bandwidth product of 10MRad (i.e. $10^7/(2\pi)$Hz), a DC gain $A_0 = 100$ and a drain current $I_D = 10\mu$A. Make the following assumptions: 1) the load capacitance is $C_L = 10$pF and the input signal source is an ideal voltage

source, i.e. the signal source has zero output resistance and C_L is dominating the frequency behaviour, 2) an ideal current source as load providing I_D, i.e. only r_o of the nFET sets the total load (like in figure 7) . Determine the length L of the transistor.

With dominant C_L the book gives the time unity gain frequency as $\frac{g_m}{2\pi(C_L+C_{gd}}$
Conditions for GBWP, i.e. ω_t:

$$\begin{aligned} C_{gd} &= 0.2e-9*W \\ \omega_t &= \frac{g_m}{C_L+C_{gd}} \mid C_{gd} \text{ is likely negligible} \\ g_m = k_n V_{OV} &= \mu C_{ox}\frac{W}{L}V_{OV} = \sqrt{2k_n I_D} \\ \omega_t &= \frac{\sqrt{2k_n I_D}}{C_L} \end{aligned}$$

Conditions for A_0:

$$\begin{aligned} r_o &= \frac{1}{\lambda I_D} \\ 100 &= A_0 = g_m r_o = \frac{1}{\lambda I_D} * \sqrt{2k_n I_D} = \frac{L}{L\lambda}\sqrt{\frac{2k_n}{I_D}} \\ A_0 &= \frac{L}{L\lambda}\sqrt{\frac{2k_n}{I_D}} \end{aligned}$$

Combining the two:

$$\begin{aligned} \frac{\omega_t C_L}{\sqrt{I_D}} &= \sqrt{2k_n} \\ A_0\sqrt{I_D}\frac{L\lambda}{L} &= \sqrt{2k_n} \\ A_0\sqrt{I_D}\frac{L\lambda}{L} &= \frac{\omega_t C_L}{\sqrt{I_D}} \\ A_0 I_D\frac{L\lambda}{L} &= \omega_t C_L \\ L &= A_0 I_D \frac{L\lambda}{\omega_t C_L} \\ &= 100*10e-6*0.08e-6/(1e7*10e-12) = 800\text{nm} \end{aligned}$$

Simpler is to realize that

$$\frac{\omega_t}{A_0} = \omega_H = \frac{1}{C_L r_o}$$

From that and $r_o = \frac{1}{\lambda I_D} = \frac{L}{L\lambda I_D}$ you can get the symbolic result ($L = A_0 I_D \frac{L\lambda}{\omega_t C_L}$) directly

From $\omega_t = \frac{\sqrt{k_n I_D}}{C_L}$ it follow that $k_n = \frac{\omega_t^2 C_L^2}{I_D} = 1e7^2 * 10e-12^2/10e-6 = 1e-3$
check:
I=10e-6; L=8e-7; kn=1e-3;
wt=sqrt(kn*I)/10e-12=1e7 OK A0=L/0.08e-6*sqrt(kn/I)=100 OK

Chapter 15

Task * (*p): Compute the propagation delays for high to low t_{PHL} and low to high t_{PLH} transitions of an inverter using the parameters of the 0.18μm process from table 1, a Vdd of 1.2V, and the method in the book on pages 1265 to 1267, i.e. where an average current is deduced from the current at the start of the transistion when the drain voltage is at the power rail and the current at the end of the transistion when the drain voltage is at Vdd/2. Assume that all transistors have width W = 540nm and L = 180nm and that the inverter drives an identical inverter and that the capacitance of the wire C_W is negligible.

solution:
Capacitance:

$$\begin{aligned}
C &= C_{go,total} + 2C_{gdi,total} + C_{dbni} + C_{dbpi} \\
&= 2C_{ox}WL + 4 * W\frac{C_{ov}}{W} + 4 * W\frac{C_{ov}}{W} + W\frac{C_{dbn}}{W} + W\frac{C_{dbp}}{W} \\
&= 2 * 8.5e-3 * 540e-9 * 180e-9 + 4 * 540e-9 * 0.35e-9 + 4 * 540e-9 * 0.35e-9 + \\
&\quad 540e-9 * 0.55e-9 + 540e-9 * 0.50e-9 \\
&= 2 * 8.2620e-16 + 4 * 1.8900e-16 + 4 * 1.8900e-16 + 2.9700e-16 + 2.7000e-16 \\
&= 3.73\text{fF}
\end{aligned}$$

Average current:

$$\begin{aligned}
i_{DN}(E_{HL}) &= \frac{1}{2}k_n(Vdd - V_{tn})^2 = 1/2 * 3/1 * 270e-6 * 0.75^2 = 228\mu\text{A} \\
i_{DN}(M_{HL}) &= k_n\left[(Vdd - V_{tn})\left(\frac{Vdd}{2}\right) - \frac{1}{2}\left(\frac{Vdd}{2}\right)^2\right] = 3/1 * 270e-6 * (0.75 * 0.6 - 1/2 * 0.6^2) = 219\mu\text{A} \\
I_{av,HL} &= (228e-6 + 219e-6)/2 = 223.5\mu\text{A} \\
t_{PHL} &= \frac{C * Vdd}{2I_{av,HL}} = 3.73e-15 * 1.2/2/223.5e-6 = 10.01\text{ps} \\
i_{DP}(E_{LH}) &= \frac{1}{2}k_p(Vdd - V_{tp}) = 1/2 * 3/1 * 70e-6 * 0.75^2 = 59\mu\text{A} \\
i_{DP}(M_{LH}) &= k_p\left[(Vdd - V_{tp})\left(\frac{Vdd}{2}\right) - \frac{1}{2}\left(\frac{Vdd}{2}\right)^2\right] = 3/1 * 70e-6 * (0.75 * 0.6 - 1/2 * 0.6^2) = 57\mu\text{A} \\
I_{av,LH} &= (59e-6 + 57e-6)/2 = 58\mu\text{A} \\
t_{PLH} &= \frac{C * Vdd}{2I_{av,LH}} = 3.73e-15 * 1.2/2/58e-6 = 38.59\text{ps}
\end{aligned}$$

Directly from (15.50-51) in the book:

$$\begin{aligned}
\alpha_n &= 2/\left(\frac{7}{4} - \frac{3V_{tn}}{\text{Vdd}} + \left(\frac{V_{tn}}{\text{Vdd}} +\right)^2\right) \\
&= 2/(7/4 - 3 * 0.45/1.2 + (0.45/1.2)^2) \\
&= 2.6122
\end{aligned}$$

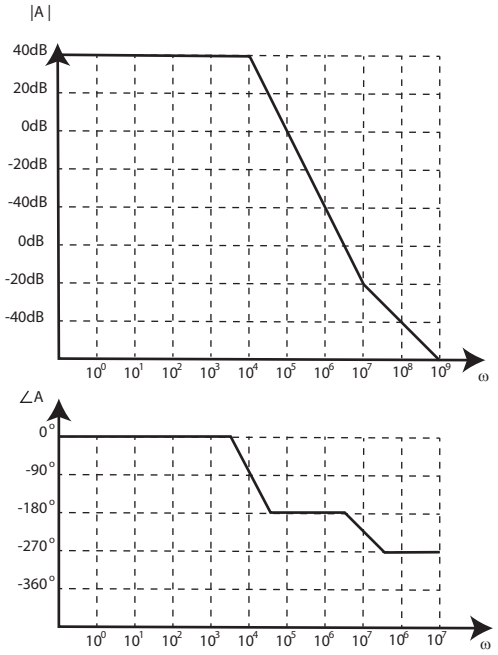


Figure 8: Solution Bode plot

$$\begin{aligned} t_{PHL} &= \frac{\alpha_n C}{k_n \text{Vdd}} \\ &= 2.6122 * 3.73e-15/3/270e-6/1.2 \\ &= 10.02\text{ps} \end{aligned}$$

Directly from (15.52-53) in the book:

$$\begin{aligned} \alpha_p &= 2/\left(\frac{7}{4} - \frac{3V_{tp}}{\text{Vdd}} + \left(\frac{V_{tp}}{\text{Vdd}}+\right)^2\right) \\ &= 2/(7/4 - 3 * 0.45/1.2 + (0.45/1.2)^2) \\ &= 2.6122 \end{aligned}$$

$$\begin{aligned} t_{PHL} &= \frac{\alpha_n C}{k_n \text{Vdd}} \\ &= 2.6122 * 3.73e-15/3/70e-6/1.2 \\ &= 38.67\text{ps} \end{aligned}$$

Transfer Functions and Bode Plots

Task * (*p): Sketch the Bode plot for transfer function:

$$A(s) = 100\frac{1 - \frac{s}{10^6}}{(1 + \frac{s}{10^4})^2}$$

Let it cover the interval $\omega \in [10^0, 10^9]$ on the x-axis.