University of Oslo
Faculty of Mathematics and Natural Sciences

Final Exam in: INF4411/3410, fall 2018
Date of exam: 30-Nov-2018
Time: 09:00-13:00
This examination paper consists of 7 page(s)
Permitted materials: All printed and written including approved (!) calculator

Make sure that your copy of this examination paper is complete before answering.

Read Carefully:

This is the final exam of INF4410 and INF3410, fall 2018. It will contribute 60% towards the final grade, while the other 40% are contributed by the mandatory labs 2 and 3 of the course. The task 3 under chapter 3 is *RESERVED for INF4411 ONLY!* Students that are registered as bachelor students in INF3410 shall *NOT* solve this task! No extra points will be given if they should solve the task!

It is recommended that you read all the tasks before starting with the exam. A good strategy thereafter is to start with the tasks you feel most comfortable with and leave the most difficult ones for last.

It is also recommended to read through all the tasks once more after you have finished, to make sure you have not overlooked anything.

Start a new page for every task you are answering and write your ID-number and task number on the top of all pages you submit. If you use several pages per task also mark the page number next to the task number. Make sure to answer all questions and follow all instructions. Clearly mark your final answers and results (all that are explicitly asked for or instructed to find in a task) with a double underline. Document your deduction of those results and any assumptions you may have had to make.

Note that you may not hand in the original task papers that you are holding now, i.e. do not write any results here but use exclusively the separate sheets of paper that you are going to hand in.

Each question is graded indicating the weight when grading.

Chapter 1

Task 1 (4p): Write down the Kirchhoff equations (sum of currents into a node is 0A) for nodes v_{O1}, v_{x2}, v_{O2} and the 2 transfer functions (preferably in root form for A) but for B) just in a reasonably simplified form) of the two circuits in figure 1.

Table 1.5 MOSFET parameters representative of various CMOS technologies and used for rough hand calculations in this text.

	0.8 μm		0.35 μm		0.18 μm		45 nm	
Technology	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
μC_{ox} ($\mu A/V^2$)	92	30	190	55	270	70	280	70
V_{t0} (V)	0.80	–0.90	0.57	–0.71	0.45	–0.45	0.45	–0.45
$\lambda \cdot L$ (μm/V)	0.12	0.08	0.16	0.16	0.08	0.08	0.10	0.15
C_{ox} ($fF/\mu m^2$)	1.8	1.8	4.5	4.5	8.5	8.5	25	25
t_{ox} (nm)	18	18	8	8	5	5	1.2	1.2
n	1.5	1.5	1.8	1.7	1.6	1.7	1.85	1.85
θ (1/V)	0.06	0.135	1.5	1.0	1.7	1.0	2.3	2.0
m	1.0	1.0	1.8	1.8	1.6	2.4	3.0	3.0
$C_{ov}/W = L_{ov}C_{ox}$ (fF/μm)	0.20	0.20	0.20	0.20	0.35	0.35	0.50	0.50
$C_{db}/W \approx C_{sb}/W$ (fF/μm)	0.50	0.80	0.75	1.10	0.50	0.55	0.45	0.50

Table 1.5
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Table 1: Typical process parameters

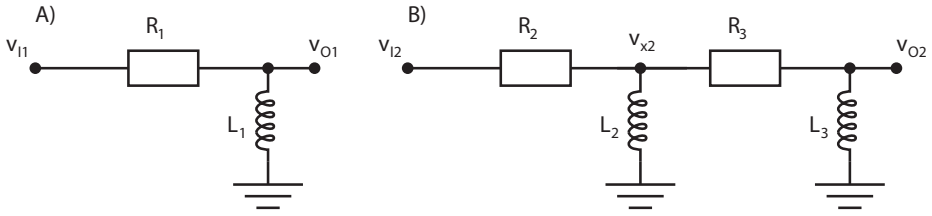


Figure 1: Two RL filters

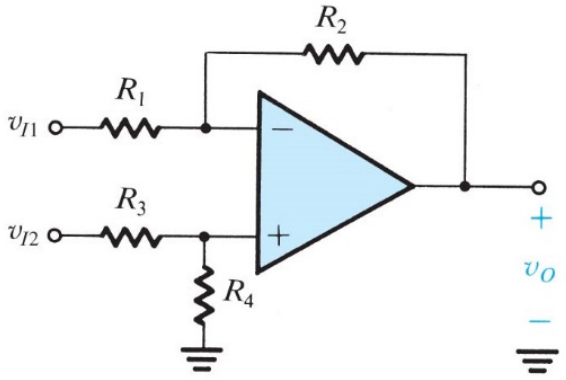


Figure 2: Differential amplifier

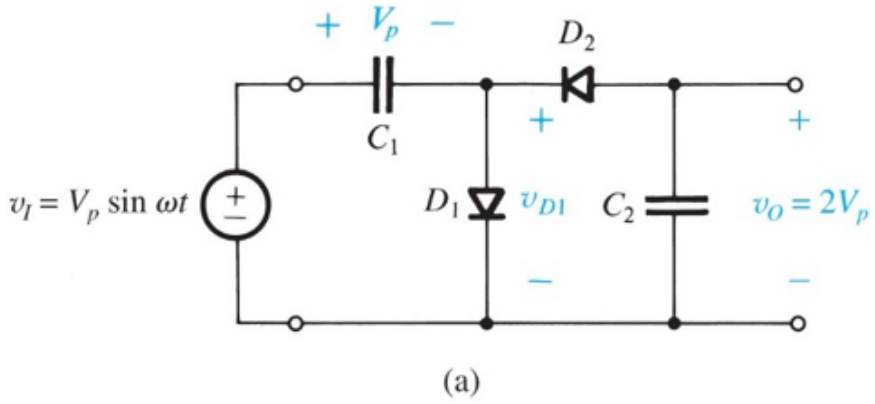


Figure 3: Figure 3.36 from the book: Voltage doubler.

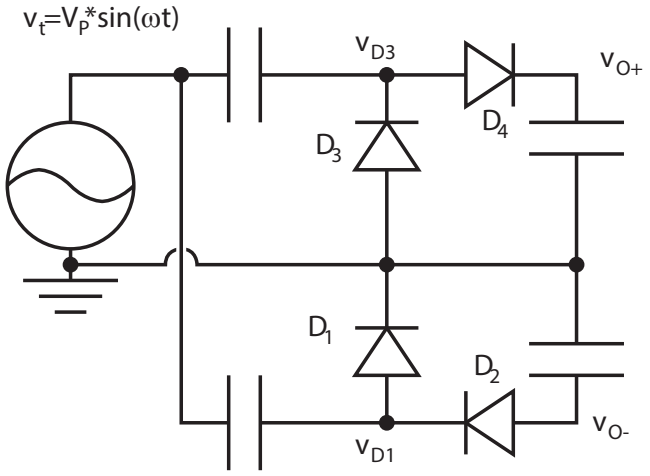


Figure 4: Rectifier derived from voltage doubler

Chapter 2

Task 2 (3p): Consider that the differential amplifier in figure 2 uses the following resistor values: $R_1 = 1\text{k}\Omega, R_2 = 2\text{k}\Omega, R_3 = 3\text{k}\Omega, R_4 = 4\text{k}\Omega$. What function does it implement exactly? Write out the function of the output in dependency of the two inputs $v_O = f(v_{I2}, v_{I1})$.

Chapter 3 (only for INF4411!)

The task 3 of chapter 3 is mandatory for students having registered as master students to course INF4411, and are NOT(!) to be solved for bachelor students registered to course INF3410. No extra point are to be gained for bachelor students registered to course INF3410 by solving this task under chapter 3!

Task 3 (only INF4411, 3p): Figure 3 depicts a voltage doubler as described in

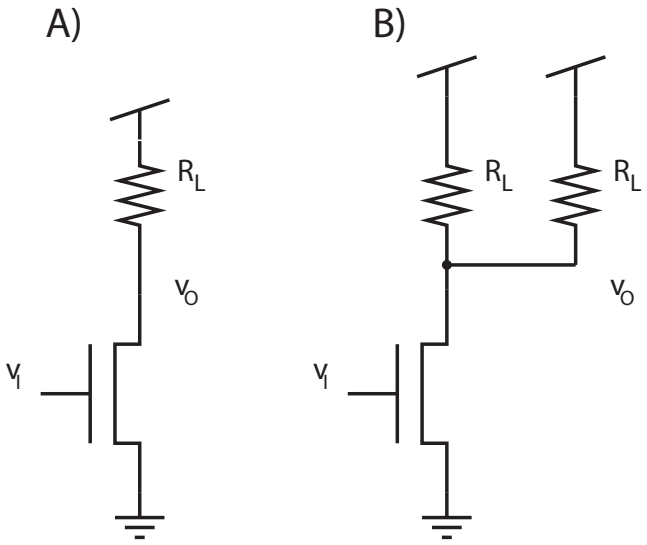


Figure 5: Two CS gain stages with different loads.

the book. Consider the diodes to be ideal, i.e. non-conducting for negative voltages and zero resistance for positive voltages. In **steady state** the output is $-2V_P$ where V_P is the amplitude, i.e. half the peak-to-peak voltage. Now consider the circuit in figure 4 that is an extension of the voltage doubler. Can you sketch the voltages v_{D1}, v_{D3} and v_O together with the input v_t (all referenced to Gnd!) over one cycle of the input signal, again in **steady state** (i.e. not from start-up (!!!) but after the voltages have become stable from one cycle to the next)?

Chapter 5

Task 4 (3p) A particular NMOS transistor is operated in its saturation region at a constant v_{GS}. i_D is found to be 100μA for $v_{DS} = 1V$ and 110μA for $v_{DS} = 2V$. Find the corresponding values for r_o, V_A, and λ.

Chapter 6

Task 5 (2p): Consider the two CS amplifiers in figures 5 A) and B). Both circuits shall be operating in strong inversion and the two NMOS transistors are identical. If the DC offset V_I of the input v_I in subfigure A) is V_{IA} (i.e. the input that sets the output voltage nicely in the linear range at $\frac{\text{Vdd}}{2}$), what is the correct DC offset V_{IB} in subfigure B) as a function of V_{IA} and the NMOS threshold voltage v_{tn}?

Task 6 (2p): A NMOS CS amplifier with a total resistive load $R_D = r_o||R_L$ has a small signal gain of -20V/V at the point of operation $V_{GS} = 0.9V$. It is implemented in the 0.35μm process of table 1 and has W/L=1. What is the size of R_D?

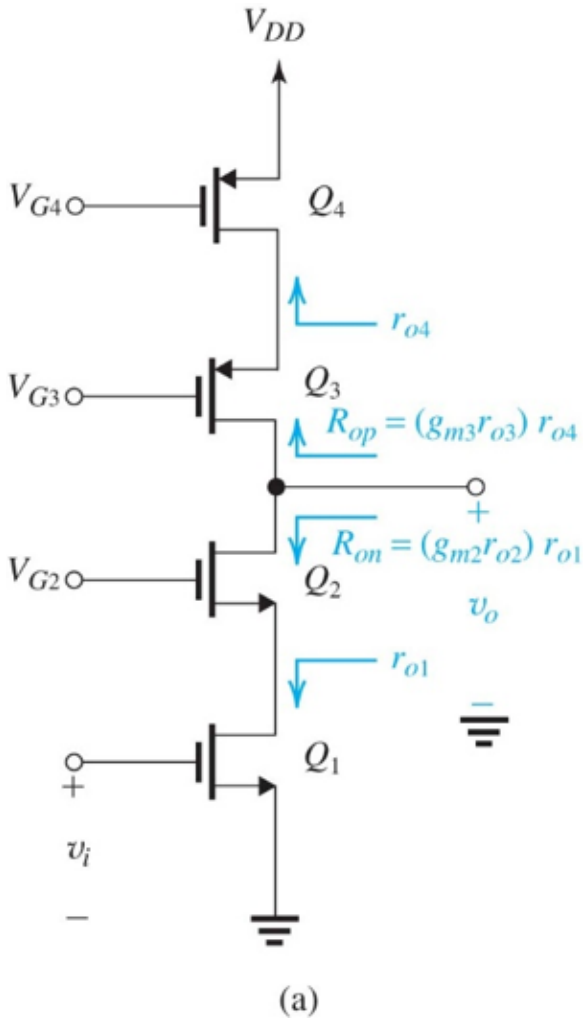


Figure 6: Telescopic cascode gain stage with cascode current source load.

Chapter 7

Task 7 (3p): A telescopic cascode gain stage with cascode current source load depicted in figure 6 is implemented with the 0.35μ process in table 1 and all transistors have a W/L=0.5. Vdd is 3.3V and the input DC offset is $V_I = 0.8V$. What is the correct bias for V_{G4} such that the output is approximately in the middle of the linear range at Vdd/2? What is the maximum value for V_{G3} and the minimum value for V_{G1} such that all transistors remain in saturation for the output being at Vdd/2?

Chapter 8

Task 8 (4p): A current-mirror loaded NMOS differential amplifier (figure 7) is constructed in 0.35μm technology with the parameters from table 1. The bias current source is implemented with an NMOS transistor with double the W/L of the other transistors. The length L of all transistors is 1μm and the width W of the transistors in the current-mirror and differential pair is also 1μm,

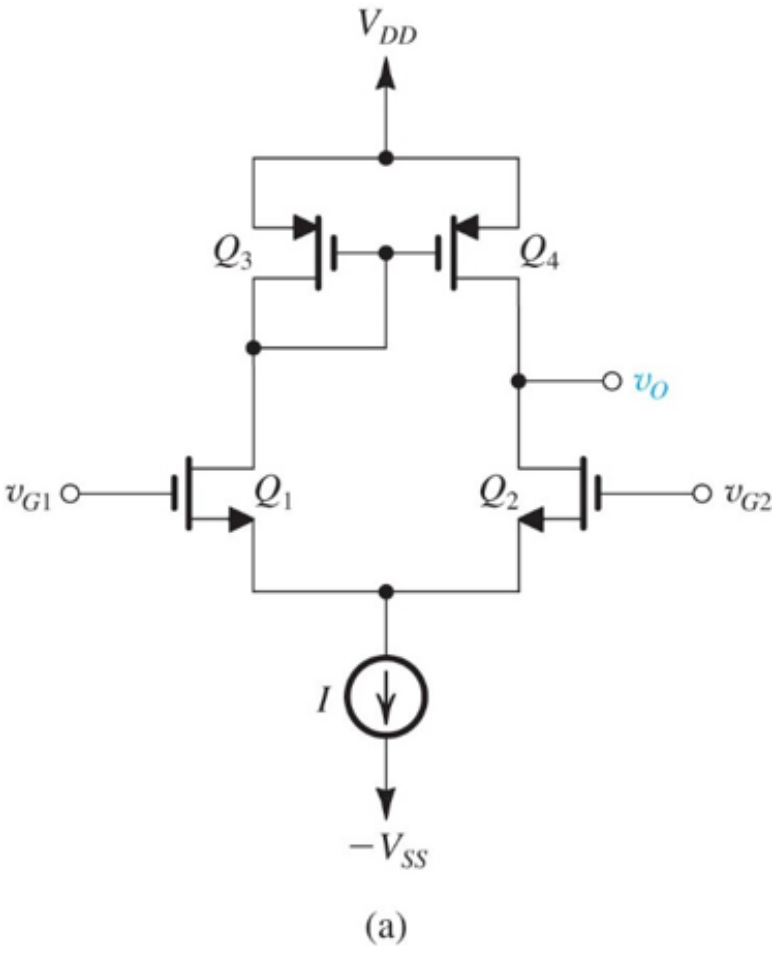


Figure 7: Differential amplifier with current mirror load. Consider the bias current source to be implemented with a NMOS transistor as well with W/L being double that of the NMOS transistors in the differential pair.

while the bias transistor has a width of 2μm. If V_{OV} of the bias transistor is 0.3V, what is the output resistance R_{SS} of the bias transistor, the common mode current gain G_{mcm} of the differential pair transistors, the current gain A_m of the current mirror, and finally the common mode voltage gain A_{cm} of the circuit?

Chapter 9

Task 9 (5p): For an NMOS CS-amplifier with a single PMOS transistor current source load using 0.35μm technology with parameters from table 1 the width W and length L of both transistors shall be 1μm. V_{ov} of the NMOS transistor is 0.2V. Compute the DC gain A_0, the -3dB cutoff frequency ω_H and the unity gain frequency ω_t without any load at the output and with a signal source output resistance R_{sig} that is the same as the total output resistance R_O of the circuit. Use the Miller approach to derive an equivalent capacitance C_{eq} at the input node from the capacitance between input and output. Only take C_{gs} and C_{gd} into account.

Chapter 15

Task 10 (3p): Progressing from 0.18μm technology to 45nm technology, using the parameters of table 1, give a well founded and explained estimate on how the propagation delay of an inverter changes. Use the simple model from the book equations (15.54) to (15.57) (repeated below) for your argument:

$$t_{PHL/PLH} = 0.69 R_{N/P} C \quad (15.54, 15.55)$$

$$R_N \approx \frac{12.5}{(W/L)_n} \text{k}\Omega \quad (15.56)$$

$$R_P \approx \frac{30}{(W/L)_p} \text{k}\Omega \quad (15.57)$$

Chapter 10/Transfer Functions and Bode Plots

Task 11 (1p): Consider a amplifier with a transfer function $A(s)$ that has two poles at the same frequency ω_{p1}:

$$A(s) = A_0 \frac{1}{(1 + \frac{s}{\omega_{p1}})^2}$$

Where is its unity gain frequency ω_t in terms of A_o and ω_{p1}?

Task 12 (3p): For the transfer function in the previous task let us assume that A_0 =80dB and the two poles are at frequency ω_{p1} =1MRad/s. Now let's introduce another single pole at frequency ω_{p2} with the aim to reduce the previous unity gain frequency ω_t by a factor 2 to $\omega_t' = \frac{\omega_t}{2}$. At what frequency is that pole? Draw the Bode magnitude plot and think of the problem graphically at first. That might then help you to find a numerical solution. Hint: it might help to label both axes in the $\log_{10}$-domain, i.e. also for the gain instead of dB.