IN3170/4170, Spring 2023

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Excerpt of Wester/Harris Chapter 9: Static and Dynamic Logic

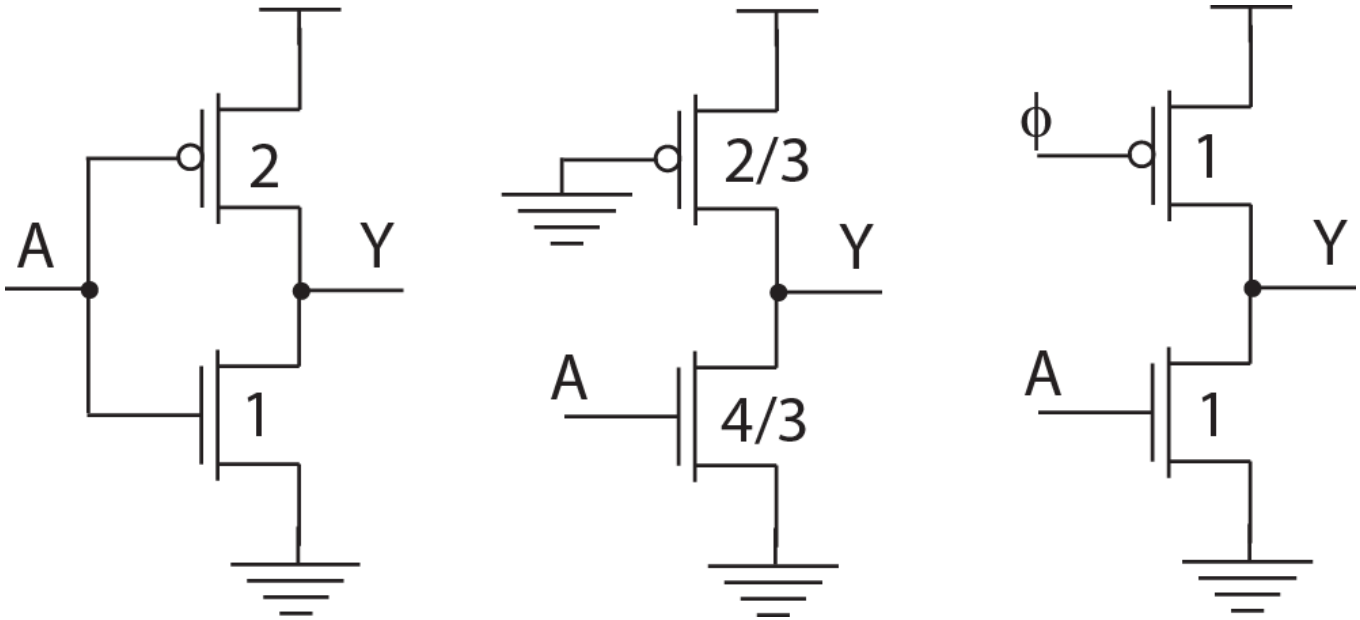
Content

Dynamic Logic Circuits

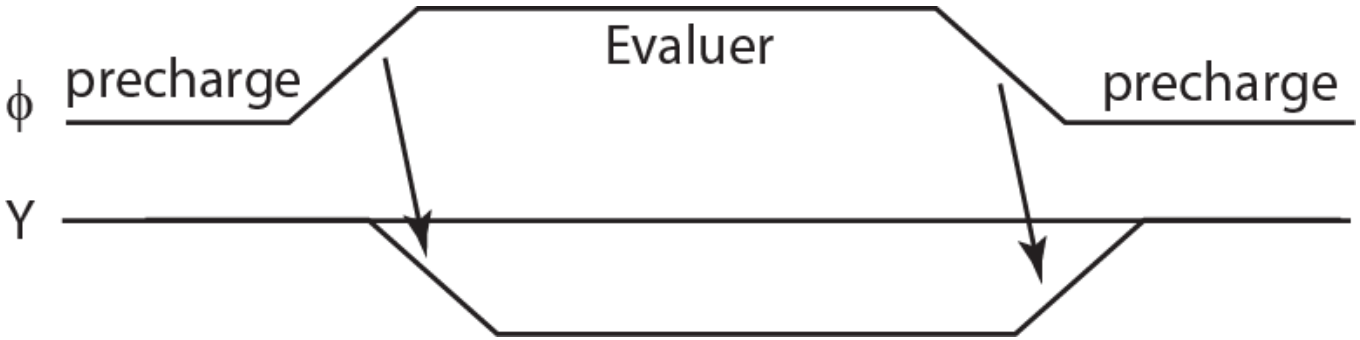
Content

Dynamic Logic Circuits

Static vs. Dynamic logic



Complementary-, pseudo nMOS, and dynamic inverter.



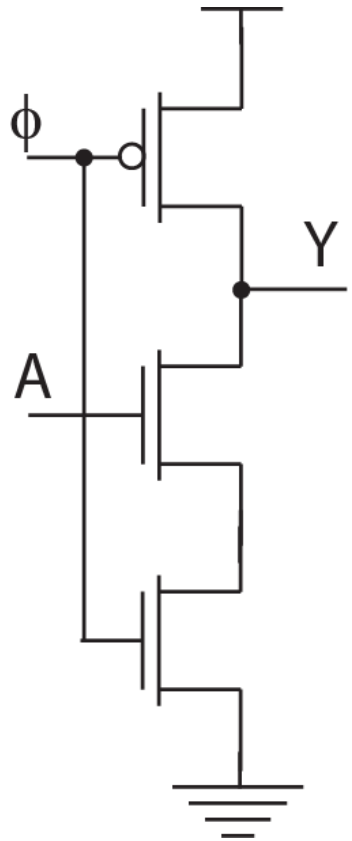
Clocking and evaluation of dynamic logic

Static vs. Dynamic Logic

Dynamic Logic:

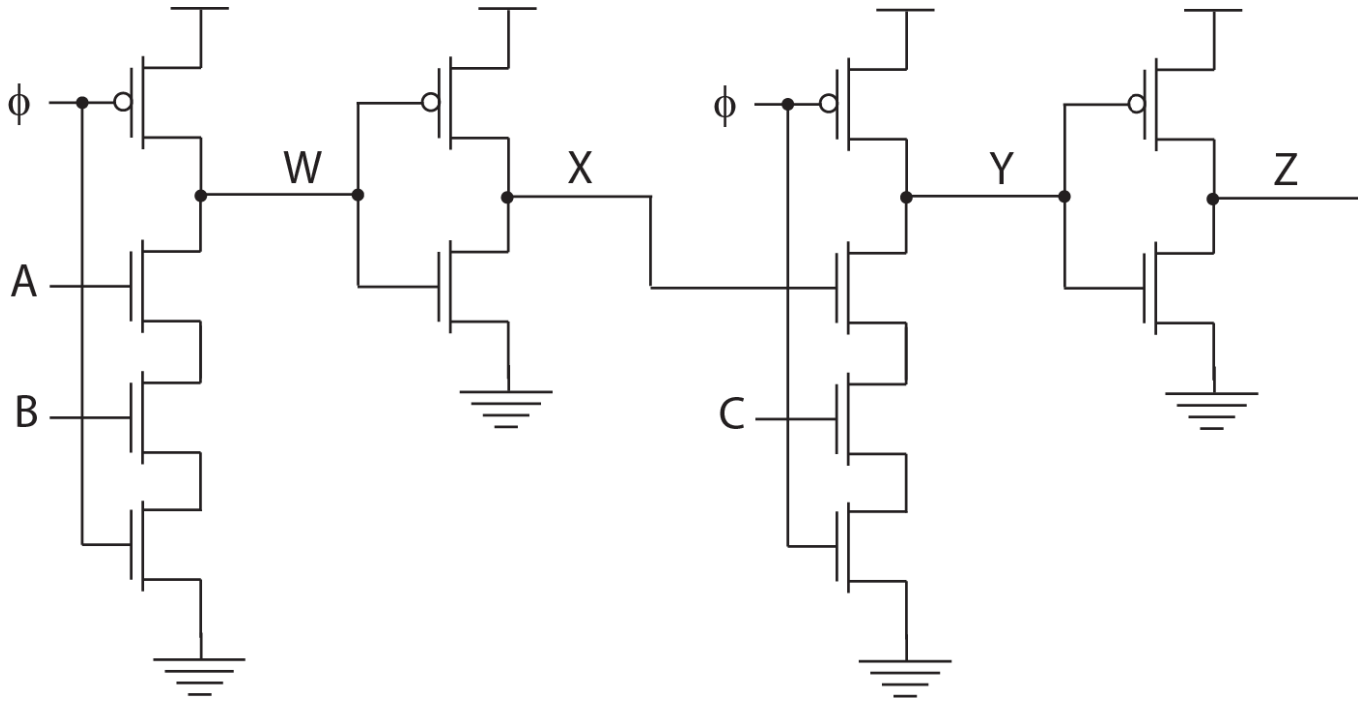
+ Only PDN with nFETs: less than half the input capacitance and still the same driving force
+ The above means more speed and less power* consumption and less layout space
- Timing/synchronization is critical (inputs, leakage etc.)
- Noise is critical
- May need clock staggering
- Charge retained in other nodes than the output node may come into play in evaluation phase
- Will always switch and might induce cross current in precharge phase: more power* consumption

Footed Dynamic Logic



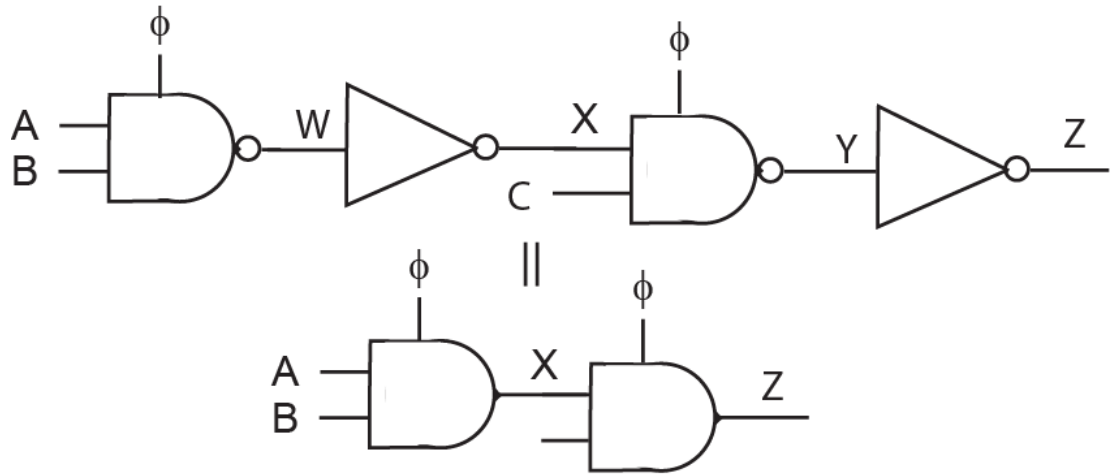
+ Avoids danger of cross current. - More load and slower

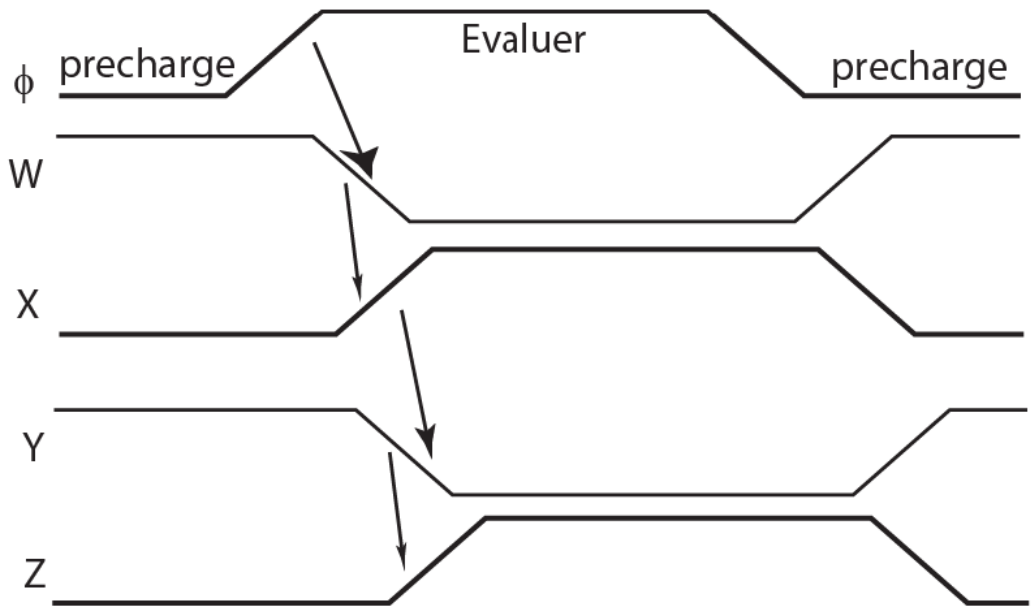
Domino Logic



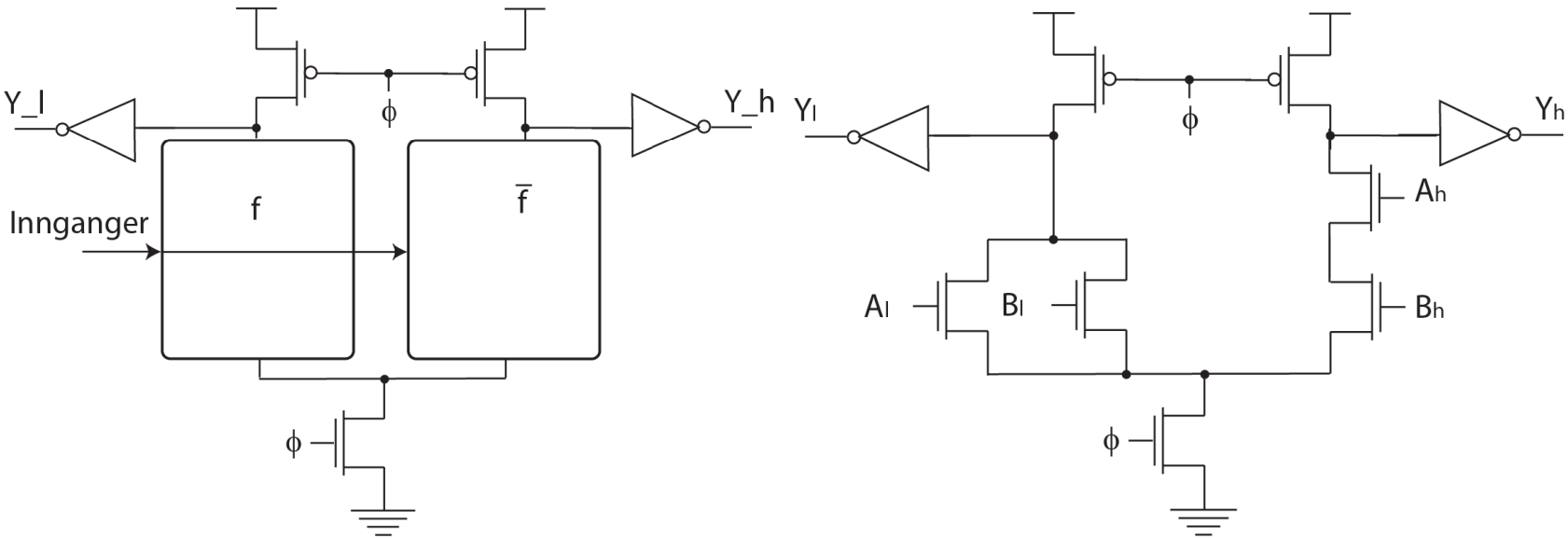
+ A dynamic logic style with no need for clock staggering and less timing dependency. Foot not really necessary. - Slower.

Domino Logic Example



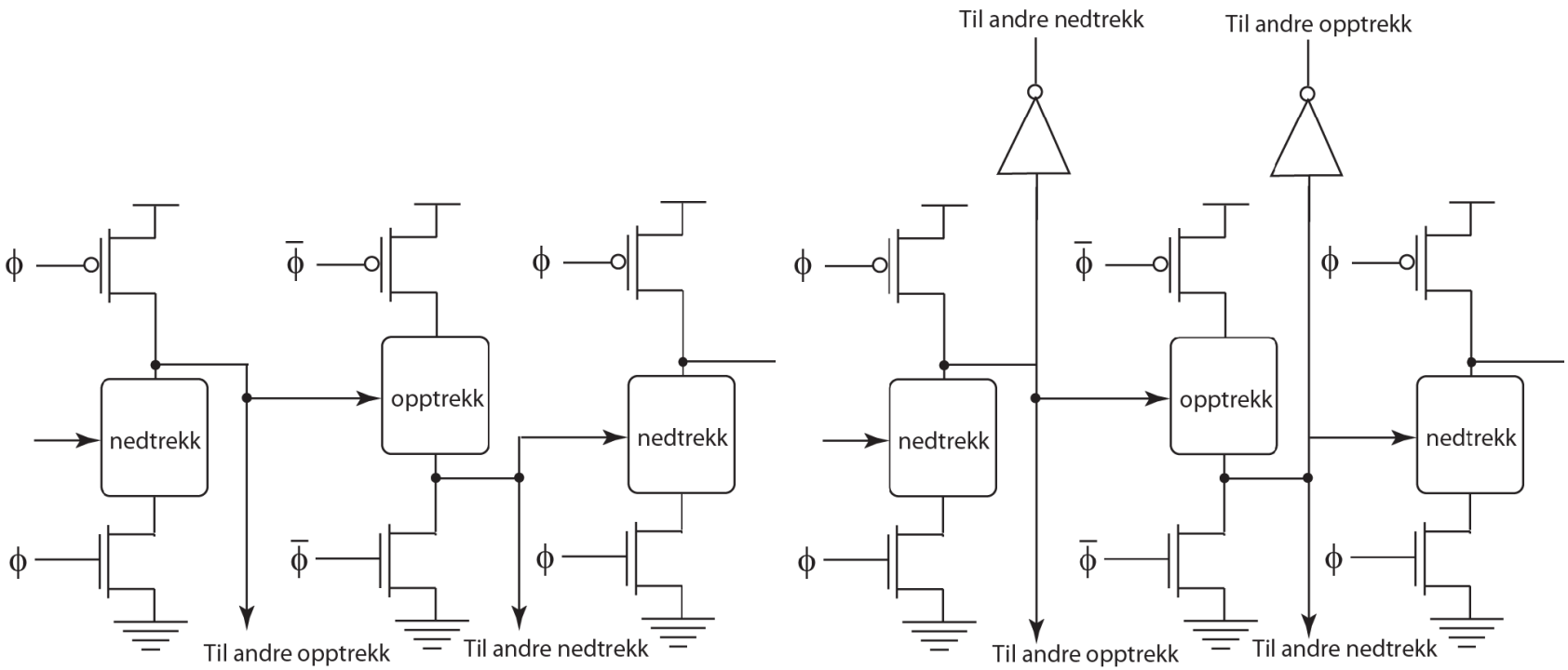


Dual-Rail Domino Logic



Can be used in asynchronous circuits signaling completion of a combinational operation.

NP Domino Logic



+ Better speed. - More layout space (pFETS).