IN3170, spring 2023, mandatory laboratory exercise 3: Transconductance amplifier (deadline 10-May-2022, 14:15!)

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change log	
19-Apr-2023	Changed description on how to determine the maximum common mode voltage. NOTE: in this new text there is now also a new request for an explanation of the circuits behaviour as V_{CM} increases beyond its upper limit!
2-May-2023	For task 2 clarified the measurment of the output range, looking at it's lower limit as the amplifier's inputs are set to sinks the maximum current, and determining the upper limit, as the amplifier is set to source the maximum current.

Abstract

This third lab puts your engineering skills to the test by giving you the deceptively simple task to tune and get the most out of a 5 transistor transconductance amplifier. Using the circuit simulation tool in Cadence, you are to try and improve it' gain bandwidth product (GBP) while trying to maintain a reasonable output voltage range and power consumption. Parameters you can use to tune your circuit are the widths and lengths of the transistor and the bias voltage (which sets the bias current) of the differential pair.

This is the third in a series of three lab tasks that will be graded and will count 40% towards the final grade. The first lab, however, will only be 'pass' or 'fail'. The students are required to pass this lab assignment to be admitted to the exam. The deadline in the title is a hard deadline! Do not miss it! Plan to submit well ahead of the deadline! We will use devilry.ifi.uio.no for submission of you lab report.

1 Report and Group Assignments

1.1 Requirements for the Lab Report (read carefully!)

You are required to execute the tasks and answer all the questions posed below and to submit a report on your work. The report needs to be explaining clearly what you have done, how you have done it, what the results were and what you conclude from them. A good basic rule for any scientific writing is that a document should provide sufficient detail for someone reading it to be able to replicate the results that are presented. Make sure to answer all (explicit and implicit) questions! Supply the report with drawings of the circuits (including the values of the components and parameters you used where appropriate, e.g. bias voltages/currents, component sizes etc.) and measurement setups! Show your measurements in graphs! Use labels in the schematics that you draw, such as M_1, M_2 (M is often used fro labelling CMOS transistors), $opamp_1$, I_1, V_1 etc. You should then use those labels in your text, since it is much easier to write: 'transistor M_1 in figure 1' than 'the transistor third from the top and second from the left in the righthand side circuit in figure 1'. **MANDATORY when assembling a circuit in the lab (so very much for this lab)**: Include a photograph of your circuit into the report!

1.2 Graded Mandatory Group Assignments

Note that this is part of the course's exam and strict rules apply as described in the document https://www.uio.no/english/studies/examinations/compulsory-activities/mn-ifi-mandatory.html . The page explains the significance of mandatory assignments in a course and in particular group assignments. It also specifies your responsibility to not plagiarize anybody else's work and that you are required to conduct and understand your own experiments and obtain your own results, while you are still allowed and encouraged to exchange advice and experiences also between groups.

Each group must deliver a written lab report using the Devilry online submission system **before** the **hard** deadline indicated in the title. Note that you can submit multiple times and the last submission before the deadline will be graded, so it might be a good idea to plan to submit preliminary versions well before the deadline. The points given for this lab assignment will determine if the lab assignment is accepted or rejected. You will need to pass this lab assigment in order to be admitted to the exam. The next two lab assignments will be weighted as 20% of the total score of the course, i.e. your final grade.

Each task is labelled with how many points it will contribute towards the score.

2 Lab Rules

2.1 Safety

Voltages over 40 Volt can in some cases be harmful, even though it usualy requires more than that. The lab equipment is thus not able to provide voltages higher than 36V. Do not use equipment other than that provided in the lab! If a part of the skin is covered with a conductive fluid or is pierced and exposed to such voltages, a current could bypass the "insolator" of the skin and run through the body. If this current passes through the heart it can cause fibrillations or even cardiac arrest. Even higher more extreme currents could also give rise to internal burns. If this happens to anybody or something else happens in the lab, seek medical help immediately: heart fibrillations can last and cause trouble long after the incident. Also notify the person in charge of the lab.

Some electronic components can explode if they are exposed to high currents. This is important to remember when working with electrolytic capacitors. However, none of the capacitors provided in the lab are electrolytic capacitors. Never bring your own electronic components into the lab!

2.2 Conduct

Good routines are necessary to make the work in the lab effective and safe:

- Food and drinks are prohibited from every lab.
- In general everybody is responsible for keeping the lab tidy.
- Always turn off the power supply before you start adding and/or removing components.
- Use an ESD protection wrist strap when handling ICs and other sensitive components.(ESD: electrostatic discharge)
- Always clean up after using equipment and tools:
  - Turn off all equipment, except for lab computer.
  - Throw away cutoffs and vacuum clean the desk, chair, and floor if nessesary.
  - Place all components you have used back to their respective places. (Do this while you work, if you have a component you don't use anymore, put it back.)
- When you leave; the desk should be clean and ready for the next group.
- Read the information posters in the lab describing what to do in case of fire or medical emergency.

3 Task

3.1 Tools

For this lab you'll be using the circuit simulation tool in Cadence again. See lab 1 and the online guide to work with Cadence here: https://www.uio.no/studier/emner/matnat/ifi/IN3170/v23/materiale/oppstsettcadencehjemmefra.html. In particular you'll need to conduct ac simulations and Bode plots.

3.2 Tasks

For this exercise we'll be working with the current mirror loaded differential pair amplifier, also referred to as transconductance amplifier (as in the input is a voltage and the output is a current, since the output is high resistance and thus better at providing an output current). Compare figure 8.32 a) in the book (replicated here as Fig. 1). Use a nFET as current source for the differential pair.

Task 1 (4p), get it to work in dc: Implement a current mirror loaded differential pair amplifier using the default minimum transistor sizes in the schematics tool. Use an explicit 1pF load. Verify that the amplifier works and characterize it's gain and common mode input range using dc simulations. Choose a bias setting that put's the circuit into moderate inversion, i.e. in the transition between weak and strong inversion. Note the resulting power consumption that depends on that bias current, i.e. the bias current multiplied with the supply voltage Vdd.

To characterize the gain, sweep input V_{G1} and keep the other V_{G2} constant in the middle of the common mode input range (Here to start with, choose Vdd/2. See task 2 for a more precise derivation of the common mode range.). Compute the output slope ($\frac{\delta V_O}{\delta(V_{G1}-V_{G2})} = \frac{v_o}{v_{id}}$) at it's steepest point. Carefully note whether the circuit shows any significant offset, i.e. whether the steepest slope occurs not when the input difference is zero but at a certain offset. Make sure to note down that offset too!

Also note down the linear range of the amplifier, i.e. the input difference extrema at which the output markedly deviates from a straight line around the point of operation.

Task 2 (4p), analyze more dc: To determine the common mode input range, you may keep the output V_O open circuited and short the inputs V_{G1} and V_{G2} together. Let's call that voltage V_{CM}. Then sweep V_{CM} from Gnd to slightly above (why?) Vdd. You are outside the common mode range when any of the 5 transistor are no longer in their active region/saturation.

For the lower boundary of that common mode range, observe the total current through the circuit (e.g. at the drain of the bias transistor). When the current markedly drops, the bias transistor is no longer in saturation.

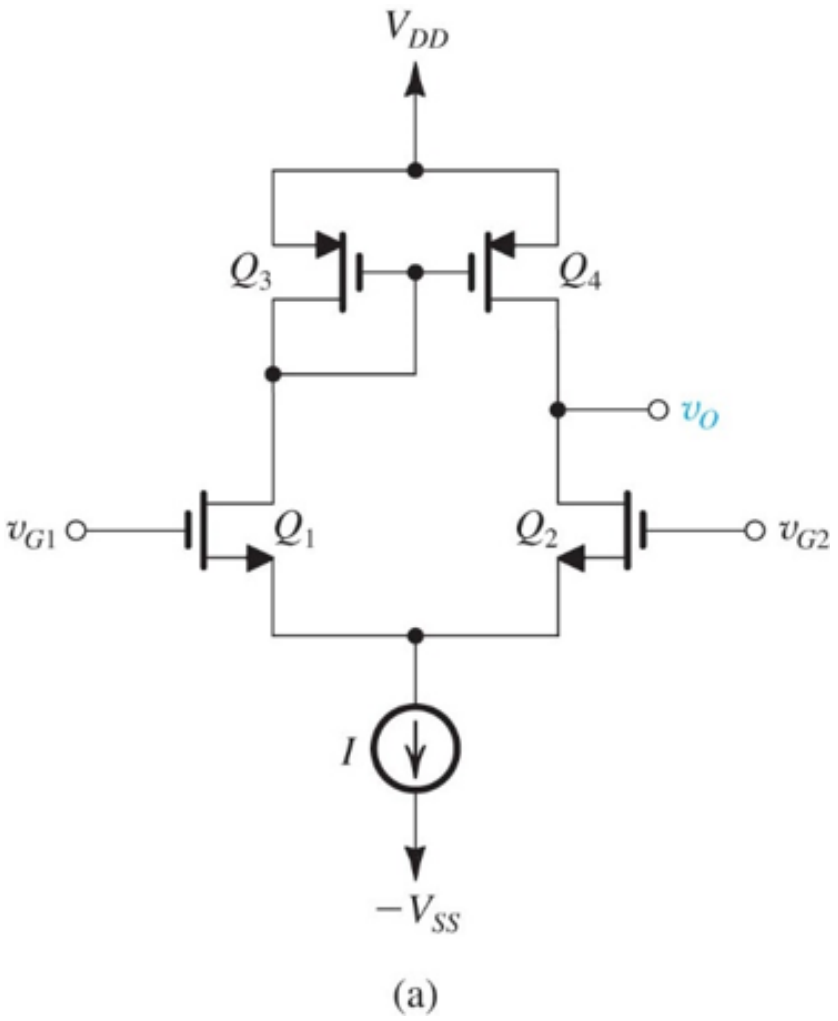


Figure 1: This is figure 8.32 a) from the book: the current mirror loaded CMOS differential pair

Note that with a minimum size bias transistor that has a relatively pronounced channel modulation effect (i.e. a small r_o) the difference between a drop still in saturation due to a decreasing V_{DS} and a slightly sharper drop due to the transistor being in the triode region (due to r_{ds}) might be subtle! This will be better observable if later on the transistor dimensions might be chosen for a higher r_o in the saturation region.

For the higher boundary it will be the input transistors of the differential pair that will go out of saturation and into the triode region. Observe their V_{DS} and make an estimate of their V_{sat} for your particular bias setting. The fact that you were instructed to choose a biassing in moderate inversion might help with that. Peculiarly, as this happens and V_{CM} goes above its upper limit the current through the input transistors does not diminish, despite the fact that they are now in the Triode region. Please explain why!

Also check out the output range limitation: set an input difference around a mid range common mode voltage (Note that the choice of the common mode voltage V_{CM} will have an influence!) just outside the linear range that would result in an output of very close to zero. Connect the output to a voltage source and make a DC sweep of that voltage source. The amplifier will want to pull the output low so will sink the entire bias I current from that voltage source. However, at some point when the output voltage becomes too low this current will rapidly decline or even become inverted. That will be the lower point of the output range. Repeat the same with the inputs chosen so the amplifier will attempt to drive the output high . Again sweep the output voltage and observe the output current. Now the entire bias current I (or even more when the input is very close to Gnd) will flow from the amplifier but as the Voltage becomes to close to Vdd, it will also start to decline more rapidly. This marks the upper limit of the output range. Those limits can also be discerned by looking at the open loop voltage output when sweeping the differential input (as done in task 1): They should approximately mark the limits of the linear output voltage range.

Task 3 (4p), analyze ac: Now conduct an ac-simulation and produce a Bode plot. Be very careful to set all DC values correctly to hit the point of operation, i.e. pay close attention to an eventual input offset encountered in task 1. Note the maximum gain at DC and compare it to what you got from the dc analysis in task 1. If the point of operation is set correctly, they should be the same. Note down the GBP, i.e. the product of the DC gain and the -3dB cut-off frequency.

Task 4 (8p), optimize GBP: Now try to change the transistor geometries and bias voltage to get a better gain-bandwidth trade off, i.e. a better GBP. You may increase L, W and the bias current for that to up to 20 times their starting values. Note that the point of operation also changes, so you will probably need to do a dc-sweep again to find it for each configuration!

When you have found a configuration with increased GBP, also determine the other DC-analysis properties from task 1 and 2 and check how much they have become affected, i.e. what's the cost of the increased GBP in terms of power consumption and/or output voltage swing and/or common mode input range? What's the cost in terms of extra layout space (let's take total gate area as an indication foir total layout space here)?