IN3170/4170, Spring 2023

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What to expect

Content

Why Transistor Level Design of Integrated Circuits?

Why Transistor Level Digital?

Why Analog?

Course Goal

Course Organization

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Why do an ASIC or transistor level GP IC design?

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Well, why not?

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- Inflexible and low level of reusability

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Alternatives?

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- Configurable FPGA, SW on CPU (pure digital)
- Microcontroller (digital, some with mixed signal options)

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So why bother?

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So why bother?

- Ultimate performance (speed, power)
- Ultimate miniaturization
- Reliability (fewer points of failure)
- Very cheap for high volume production (e.g. CPUs)
- For (Mixed-Signal) Systems-on-Chip (SoC)

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Why do a Digital transistor level design?

Why do a Digital transistor level design?

See previous arguments for and against ASIC
The most important is the small price per piece for high volume production particularly for large scale systems-on-chip (SoC), e.g. CPU, but also FPGAs, GPUs, Microcontrollers etc. (mostly not 'full custom' design but automated 'synthesis'), but real understanding on a single transistor level is required for the ultimate performance in speed, miniaturization, power consumption. Analogous in SW of where it's worth to program in Assembler.

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The world is analog

Analog electronics for sensor/actuator interfaces



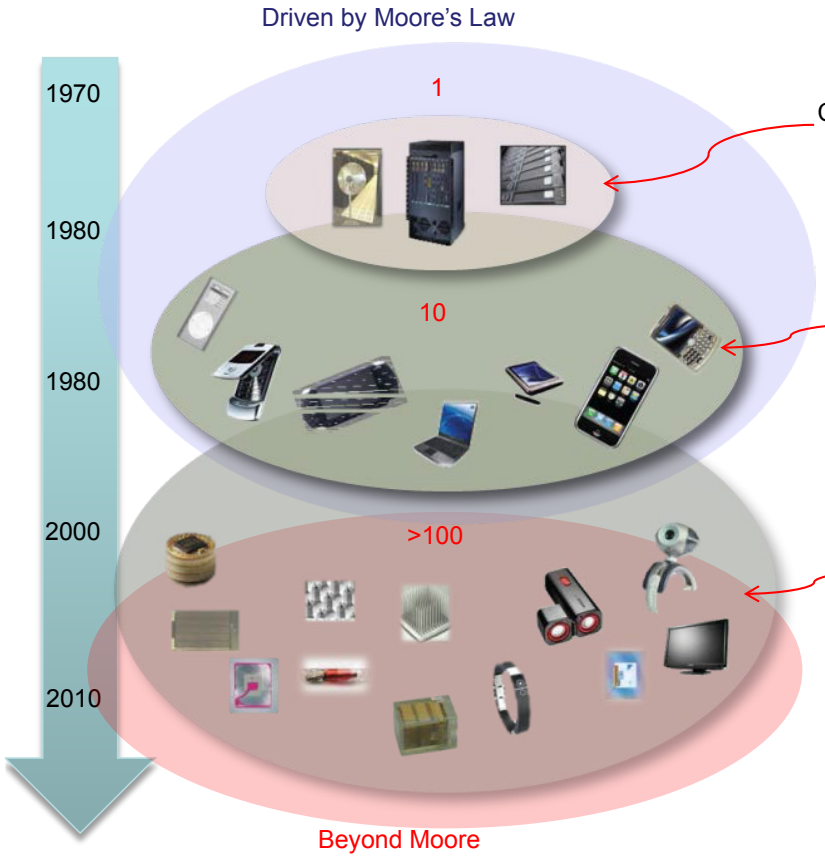
$\Leftrightarrow$

$\Leftrightarrow$ user $\Leftrightarrow$



Ubiquitous Sensors Interfaces

Trend to 'Cyberphysical Systems'



Computational Infrastructure
- Stationary/backend
- Wired
- High end computing

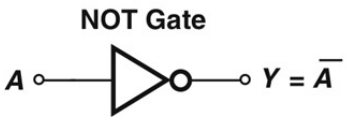
Mobile access devices
- Human interaction
- Portable
- Mostly wireless
- Battery

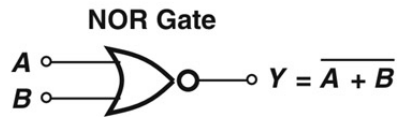
Sensory swarm
- Miniature
- Wireless
- Autonomous/self-contained
- Controlling and sensing natural processes

Even Computers are Analog ;-)

Where the digital abstraction breaks down

- Gates

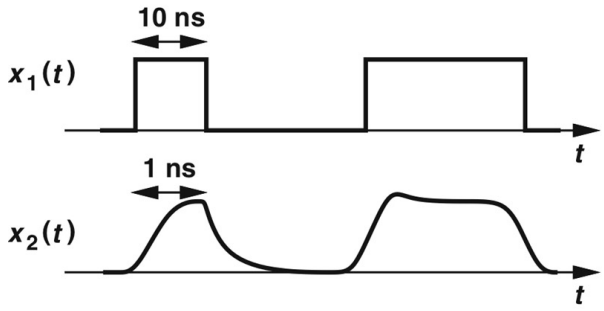




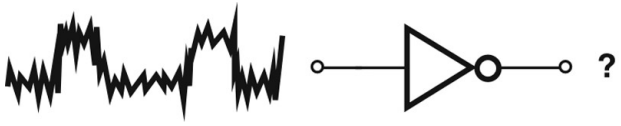
- Increasing speed
  - Why this degradation?
  - How do we improve performance?
  - Digital → analog
    - Going for speed…

100MHz

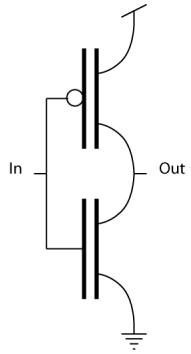
1GHz



- Noise/interference



  - Where does this noise originate?
  - How do we reduce this noise/interference?
  - Digital → analog
    - When scaling down size and scaling up complexity



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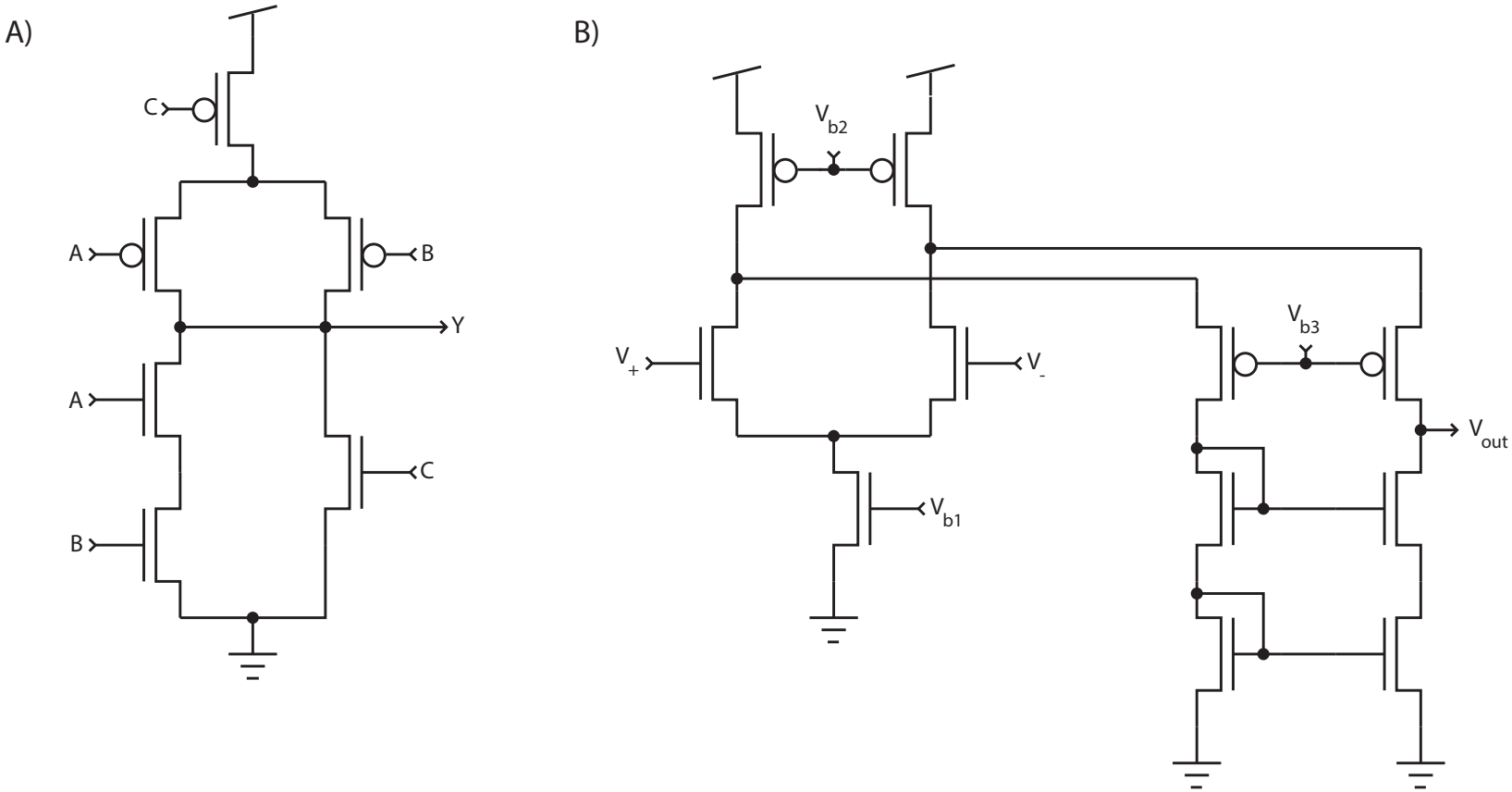
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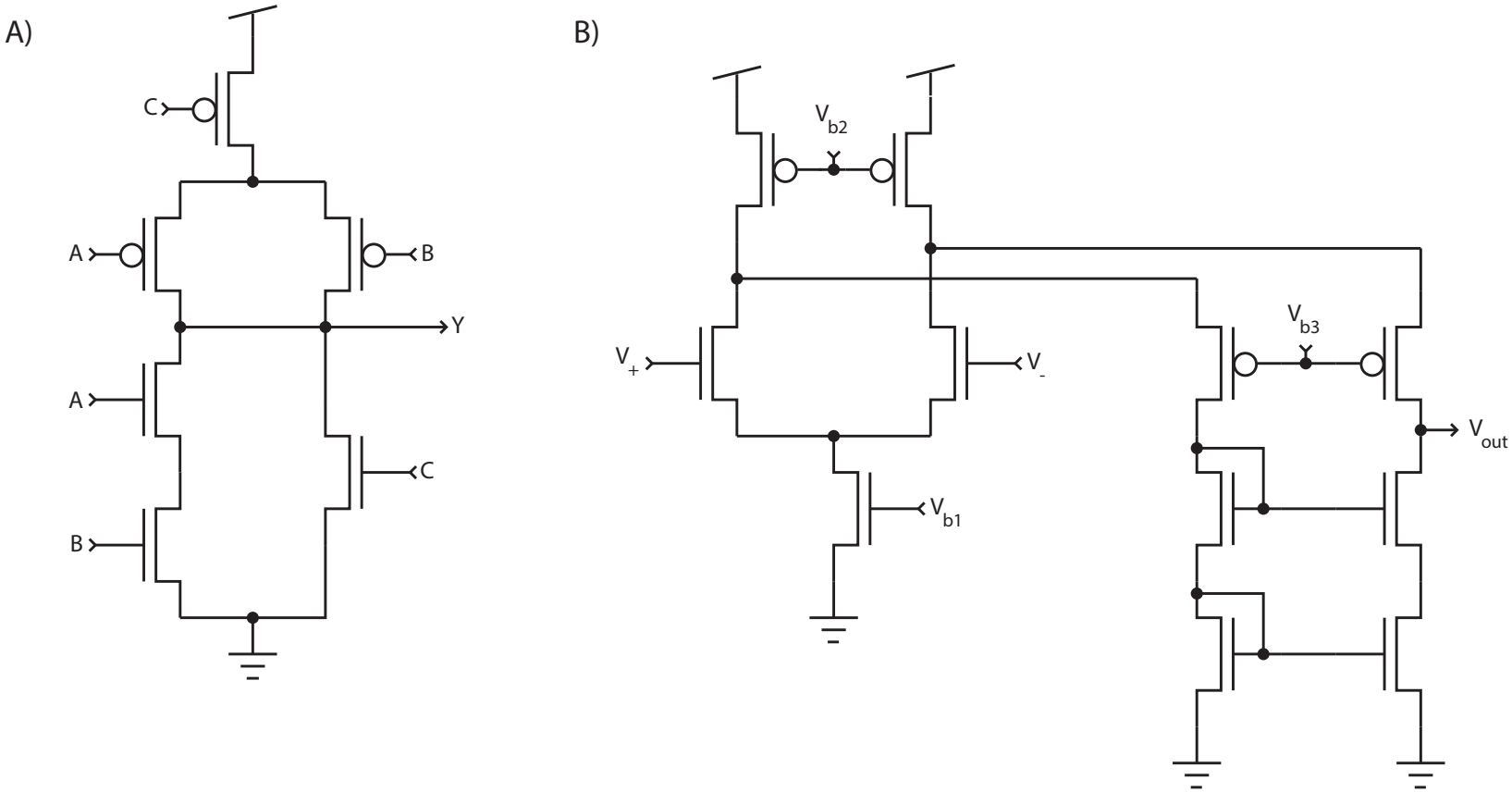
Course Organization

Course Goal (1/3)



Understand these two circuits thoroughly!

Course Goal (1/3)



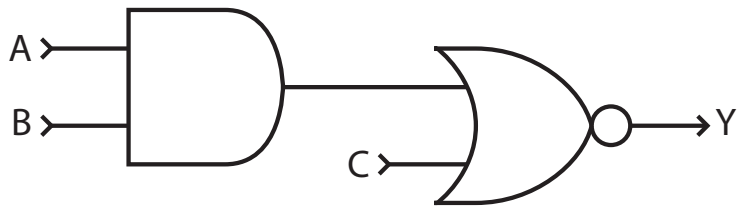
Understand these two circuits thoroughly!

Understand: analysis, properties, applications, limitations, tweaking, high level descriptions ...

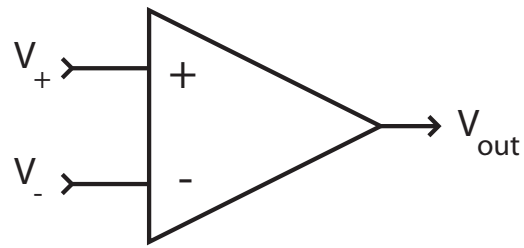
Course Goal (2/3)

And thereby understand the basic building blocks of analog and digital circuits:

A)



B)



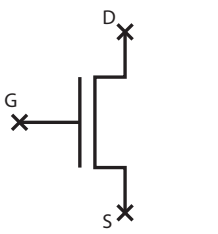
$$Y = \neg((A \wedge B) \vee C)$$

$$V_{out} = A(V_+ - V_-) \tag{1}$$

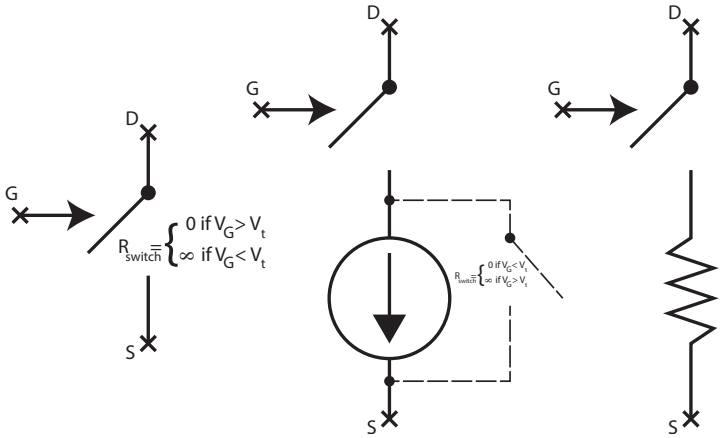
Course Goal (3/3)

... starting from modelling the basic active element of CMOS electronics, the field effect transistor (FET)

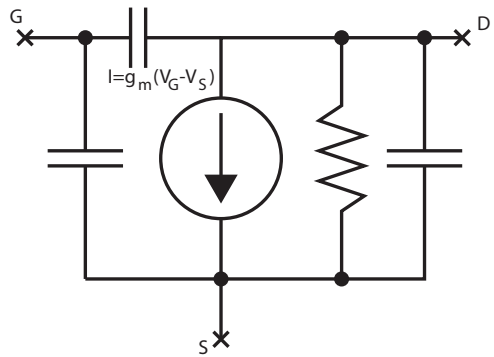
nFET symbol



Digital Abstractions



Analog Linear Abstraction



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Course Organization (1/2)

Teaching 17 lectures (Wednesdays 14-16 seminar room Java, sometimes Tuesdays 10-12 in seminar room C) , lecture foils, podcast (no guarantee! Backup: last year's recordings), book: 'Microelectronic Circuits' by Sedra & Smith, International (!) 7th Edition, selected papers

Labs 3 tasks (counting 40% towards final mark. Task 1 is only pass/not pass but a pass is required!), lab assistant: Tonny Nguyen Duc Do, workgroups with up to 3 students (register in Devilry), TA group sessions Tuesdays 14-16 and Fridays 14-16

Course Organization (2/2)

Paper exercises exercises in preparation for exam (!), mostly 'problems' from the book, Tuesdays 10-12 in seminar room C, teaching assistant: Mansur Dudajev

Exam written exam, counting 60% towards final mark, 7-June, 9:00-13:00

Tools Cadence, matlab, solder iron/bread board, lab equipment

Skills electronics, maths, physics, programming