IN3170, spring 2024, mandatory laboratory exercise 3: Interpret CG stage in a cascode as current conveyor (deadline 6-May-2024, 10:15!)

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change log	
2-Apr-2024	First release
11-Apr-2024	Added a word of caution that the output resistance r_{ds} or R_O of a current source is not to be confused with R_{ON} of a digital switch model, as has been the topic of lab 2!!! Also a more vehement hint for task 2 that it is NOT necessary to include the pFET switch or the capacitor to derive a $\frac{V}{I}$ relationship of a current source (that is needed to derive r_{ds})
30-Apr-2024	Task 1 updated: Since we did not get the 1μF capacitors in the lab, the students used 390pF. Thus they were allowed to change the specs for C, and also on the resistor and target current for task 1 to get a good measurement with the speed limitation of the oscilloscope. IMPORTANT: choose the target current I and resistor R such that the target current $I = \frac{V}{R}$ is the same that flows through the resistor at a voltage of 1V!
2-May-2024	explanation of equivalent output resistance R_O extended with link to compendium

Abstract

In this lab we shall investigate the function of a common gate stage as a current conveyor and devise some variants of good and bad current sources.

This is the third in a series of three lab tasks that will be graded and will count 40% towards the final grade. The first lab is only be 'pass' or 'fail'and the students are required to pass this lab assignment to be admitted to the exam. The second and third labs will get a score of between 0% and 100% and will each count 20% towards the course score. The deadline in the title is a hard deadline! Do not miss it! Plan to submit well ahead of the deadline! We will use devilry.ifi.uio.no for submission of you lab report.

1 Report and Group Assignments

1.1 Requirements for the Lab Report (read carefully!)

You are required to execute the tasks and answer all the questions posed below and to submit a report on your work. The report needs to be explaining clearly what you have done, how you have done it, what the results were and what you conclude from them. A good basic rule for any scientific writing is that a document should provide sufficient detail for someone reading it to be able to replicate the results that are presented. Make sure to answer all questions! Supply the report with drawings of the circuits (including the values of the components and parameters you used where appropriate, e.g. bias voltages/currents, component sizes etc.) and measurement setups! Show your measurements in graphs! Use labels in the schematics that you draw, such as M_1, M_2 (M is often used fro labelling CMOS transistors), $opamp_1$, I_1, V_1 etc. You should then use those labels in your text, since it is much easier to write: 'transistor M_1 in figure 1' than 'the transistor third from the top and second from the left in the righthand side circuit in figure 1'. **MANDATORY when assembling a circuit in the lab**: Include a photograph of your circuit into the report!

1.2 Graded Mandatory Group Assignments

Note that this is part of the course's exam and strict rules apply as described in the document https://www.uio.no/english/studies/examinations/compulsory-activities/mn-ifi-mandatory.html . The page explains the significance of mandatory assignments in a course and in particular group assignments. It also specifies your responsibility to not plagiarize anybody else's work and that you are required to conduct and understand your own experiments and obtain your own results, while you are still allowed and encouraged to exchange advice and experiences also between groups.

Each group must deliver a written lab report using the Devilry online submission system **before** the **hard** deadline indicated in the title. Note that you can submit multiple times and the last submission before the deadline will be graded, so it might be a good idea to plan to submit preliminary versions well before the deadline. The points given for this lab assignment will determine if the lab assignment is accepted or rejected. You will need to pass this lab

assignment in order to be admitted to the exam. The next two lab assignments will be weighted as 20% of the total score of the course, i.e. your final grade.

Each task is labelled with how many points it will contribute towards the score.

2 Lab Rules

2.1 Safety

Voltages over 40 Volt can in some cases be harmful, even though it usually requires more than that. The lab equipment is thus not able to provide voltages higher than 36V. Do not use equipment other than that provided in the lab! If a part of the skin is covered with a conductive fluid or is pierced and exposed to such voltages, a current could bypass the "insulator" of the skin and run through the body. If this current passes through the heart it can cause fibrillations or even cardiac arrest. Even higher more extreme currents could also give rise to internal burns. If this happens to anybody or something else happens in the lab, seek medical help immediately: heart fibrillations can last and cause trouble long after the incident. Also notify the person in charge of the lab.

Some electronic components can explode if they are exposed to high currents. This is important to remember when working with electrolytic capacitors. However, none of the capacitors provided in the lab are electrolytic capacitors. Never bring your own electronic components into the lab!

2.2 Conduct

Good routines are necessary to make the work in the lab effective and safe:

- Food and drinks are prohibited from every lab.
- In general everybody is responsible for keeping the lab tidy.
- Always turn off the power supply before you start adding and/or removing components.
- Use an ESD protection wrist strap when handling ICs and other sensitive components.(ESD: electrostatic discharge)
- Always clean up after using equipment and tools:
  - Turn off all equipment, except for lab computer.
  - Throw away cutoffs and vacuum clean the desk, chair, and floor if necessary.
  - Place all components you have used back to their respective places. (Do this while you work, if you have a component you don't use anymore, put it back.)
- When you leave; the desk should be clean and ready for the next group.

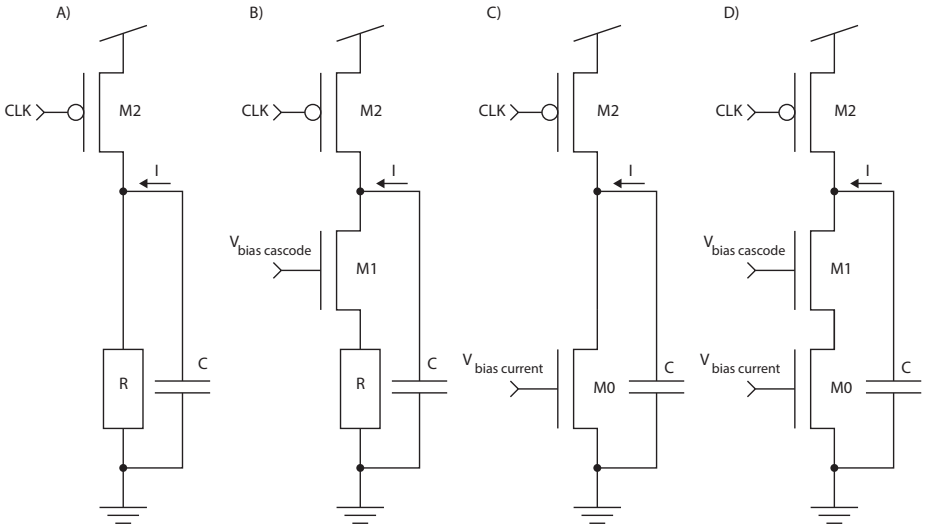

Figure 1:

- Read the information posters in the lab describing what to do in case of fire or medical emergency.

3 Task

3.1 Tools

Also see labs 1 and 2 for descriptions of the tools, software and equipment in the lab!

For the GPIB instruments there is a short guide to get started, including a *constantly updated list of known issues* here: https://www.uio.no/studier/emner/matnat/ifi/IN3170/v24/materiale/lab-gpib-instrument-guide.html

Additional items to be used in lab 3:

- **IC CD4007UBE with 6 transistors** There will be generic PCBs in the lab where you shall solder on an IC labelled 'CD4007UBE' and some resistors and where necessary some cables. The IC contains 6 transistors and some interconnections. Check the data sheet 'cd4007ub.pdf' under 'resources' on the course 2024 webpage.

- a 100kΩ resistor and a 1μF capacitor. You may use slightly deviating values. Please report the actual values used!

3.2 Lab Tasks

Task 1 (8p): (Idea: have a nFET as current source to discharge a capacitor, a pFET switch to reset. Check how constant the current is without and with a cascode nFET ....)

In short: we shall build a very bad current source and improve it with a CG current conveyor (aka cascode transistor).

Once again you shall use the IC CD4007UBE to build two circuits, specifically the ones in figure 1 a) and b). Use a 100kΩ resistor and a 1μF capacitor (or similar (report!)). Apply a 5V Vdd: be carefull to also connect pins 7 and 14 appropriately that connect to the bulks of respectively the nFETs and pFETs on the IC.

Applying a square wave CLK signal to M2 (Choose an appropriate cycle time for CLK to be able to observe the behaviour we are interested in!) will toggle between resetting the voltage V_C on the capacitor to Vdd and discharging that voltage through either only R (a) or R and M1 in series (b) to Gnd.

What we would like to achieve is a discharge of C with a constant current of 10μA. **If you use a different resistor than 100kΩ, choose the current to be the current that flows through the resistor at 1V!** This will be important for 1b) to achieve that current through a wide range of voltages on the capacitor. How would the voltage on C theoretically look like if we did manage to achieve a perfectly constant current, aka an ideal current source? Obviously, with just the resistor, that's not what will be happening. It will conduct 10μA only when the voltage across the 100kΩ is exactly 1V. Can you write a theoretical expression for that discharge curve? Can you measure it and plot it together with the ideal constant 10μA discharge curve?

Circuit (b) can make the discharge curve much more similar to that of a constant current discharge, at least for part of the voltage range on V_C. Can you choose an appropriate $V_{\text{bias\_cascode}}$ such that the current remains reasonably close to 10μA for as much of the entire discharge of V_C between Vdd and Gnd as possible? Why does that particular bias voltage work? Please describe where the current is close to 10μA and where it deviates more clearly and explain what's happening as best you can! Can you compute the total output resistance R_O of R and M0 in series for the part of the curve where it behaves most like a good current source? (**Hint:** See compendium section 5.2, and consider the Norton equivalent circuit as a model of a close to ideal current source to compute R_O (R_S or Z_S in the compendium). You will need the voltage and current at at least two relatively close points of your discharge curve, and for the current in those two points you need in turn two points around each of those points in the discharge curve)

NOTE: R_O here has nothing to do with the digital switch model equivalent

resistance R_{ON} that you had to find in lab 2! Instead, find out how to measure and compute the output resistance of a signal source in a particular point of operation (or here for a specific region of operation where the circuits behaves closest to an ideal current source and where R_O should be approximately constant). This is not at all simple here in the physical measurement setup. Maybe solve this in the simulation task 2 first (where it should be simpler), and then come back here and maybe figure out a way to do this here too.

3.3 Simulation Tasks

Task 2 (8p):

In short: we shall improve a reasonably good current source to be even better with a CG current conveyor (aka cascode transistor).

As you may already know, a FET operating in its saturation region is already a quite good approximation of an ideal current source. Can you briefly explain what the hallmark of an ideal current source is and how you can see from the I_D vs V_{DS} curve of a FET that it comes close?

Simulate in Cadence and the 65nm TSMC PDK only (!) the part of the circuit in figure 1 c) that you need in order to get the I_D vs V_{DS} curve of transistor M0 and plot that curve (i.e. you can actually do that without the capacitor and pFET reset switch). You may either use a DC analysis where V_C is a sweep parameter, or a transient analysis where V_C is a (slow) ramp produced by a 'vpulse' cell. You can measure currents by using 'choose on schematic' and then click on a pin of a component (ask your TA if in doubt!). Start with the standard size nFET dimensions. The 65nm TSMC process uses 1.2V as Vdd, so we only need V_{DS} from 0V to 1.2V. Choose $V_{\text{bias\_current}}$ appropriately such that the current I_D in saturation is close to 100nA (i.e. not 10μA as used in the previous task and the discreet IC, which would be a bit much current for a minimum size transistor in 65nm). Show the I_D vs V_{DS} (aka V_C) plot and compute r_{ds} in the saturation region from the measurement!

Can you change $\frac{W}{L}$ of M0 to make it a better current source? No need to try to make it the absolutely best current source it could be, just make it visibly better and explain what parameter you need to change for this. In other words try not to loose too much range of V_C for which it works (which likely would be a trade off). Document!

Now add M1 in series like in (d) and choose an appropriate $V_{\text{bias\_cascode}}$ for it to still provide close to 100nA for an as large as possible range of voltages V_C. Use the same dimensions $\frac{W}{L}$ that you use for M0. Show the new resulting I_D vs V_C curve. The goal is to make this a better current source at the cost of reducing the range of V_C for which it works like one. Try to get a good trade off here and report (do not forget to report the resulting R_O)!