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CMOS Field Effect Transistors (FETs)

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Field Effect Transistor (FET) Cross Sections

Large Signal Models

Small Signal Models

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First MOSFET circuits

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Field Effect Transistor (FET) Cross Sections

Large Signal Models

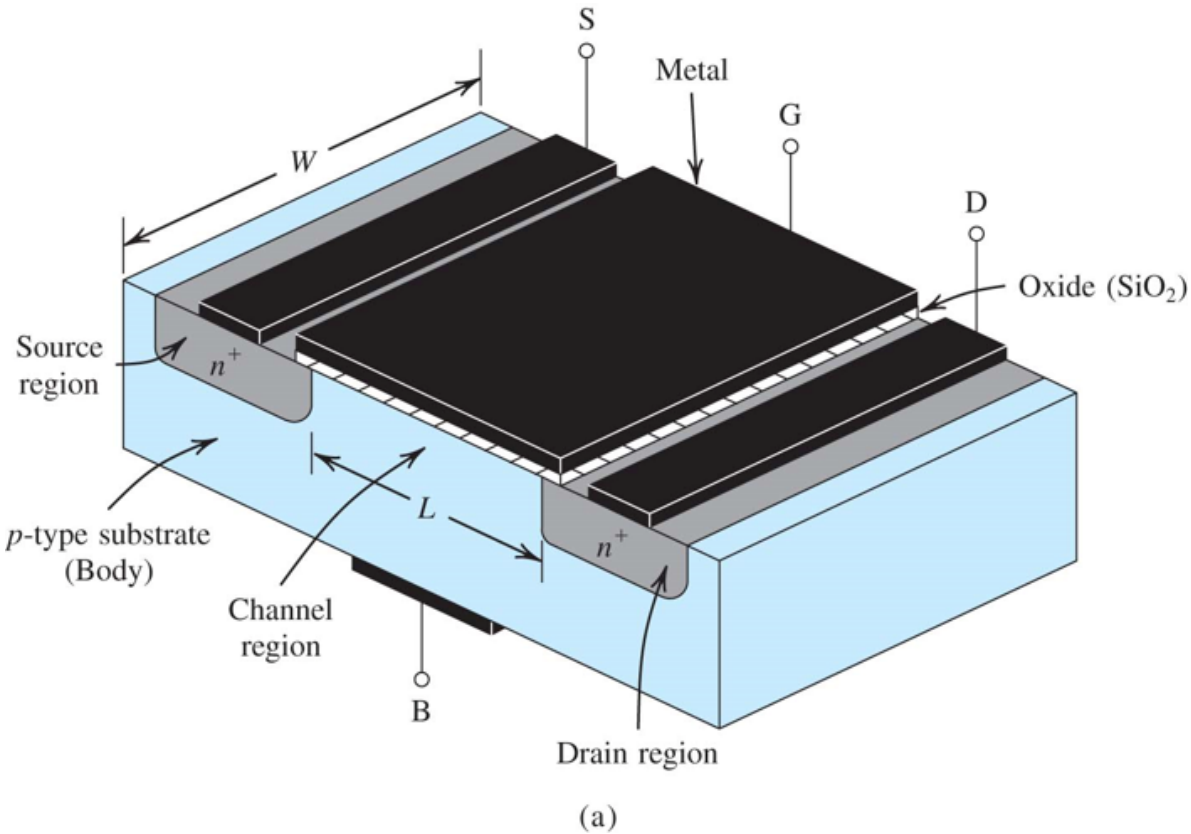
Small Signal Models

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Device Concept

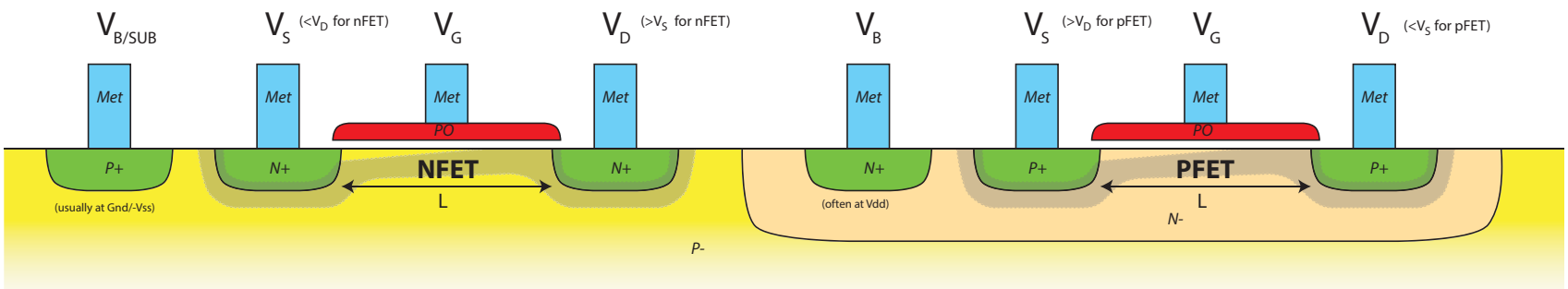
(illustration from book: Sedra, Smith)



(a)

nMOSFET and pMOSFET cross section

in 'Bulk' technology
Spelled out: n/p-channel Metal-Oxide-Semiconductor (MOS) Field-Effect Transistor (FET). Often just referred to as nFET/pFET or nMOS/pMOS. In the also often used term CMOS the 'C' stands for 'Complementary'. The 'Metal' term stems from a time when the gate was made from metal. Today it's polycrystalline silicon.
The terminals are bulk (B), gate (G), source (S), and drain (D).



Short Sidetrack: PN-junction

(illustration from book: Carusone, Johns, Martin)

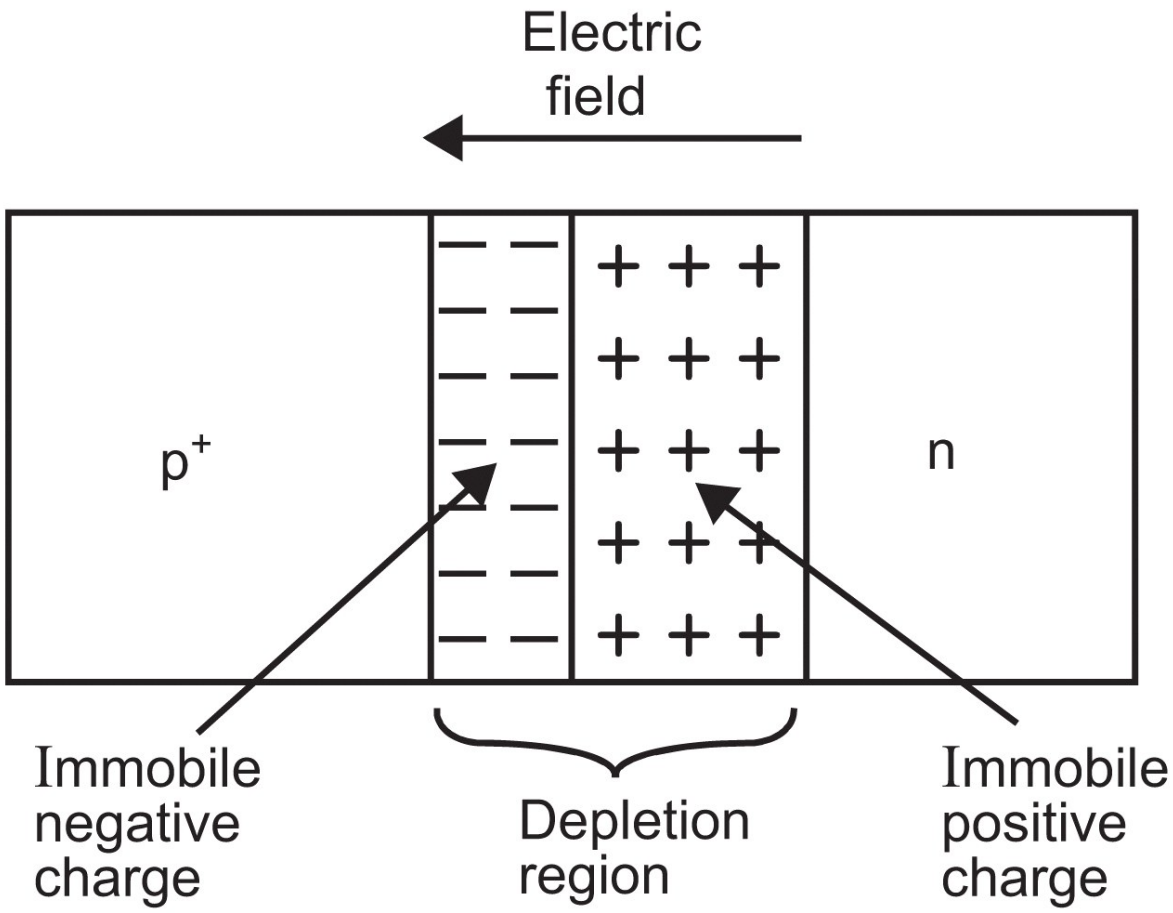
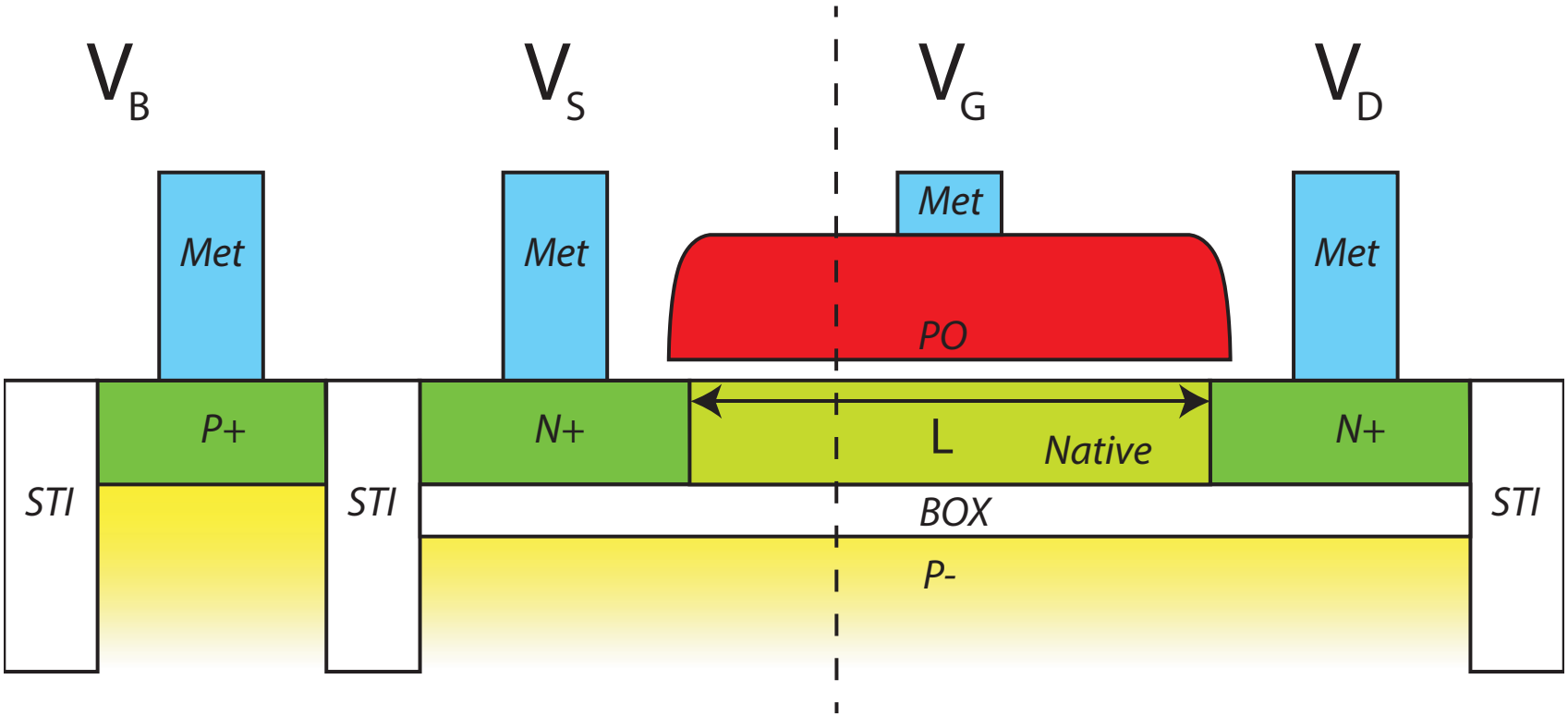


Figure 1.2
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Note: Reverse biased PN-junctions act like capacitors.

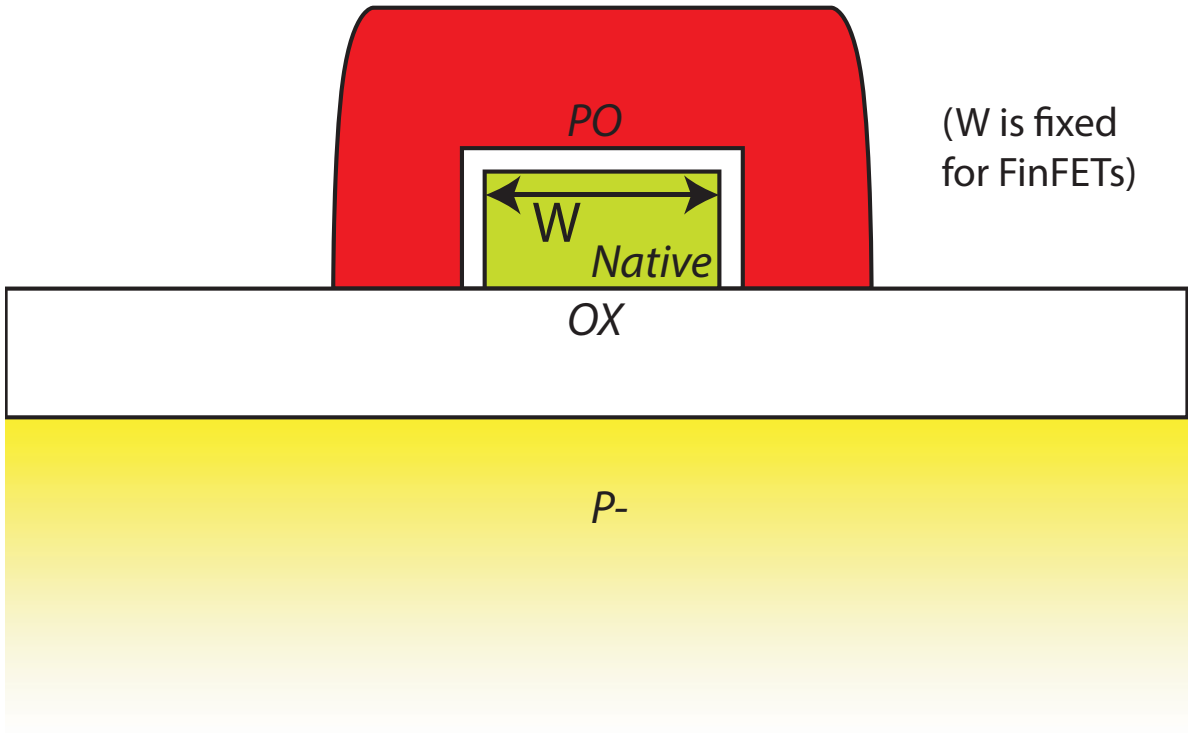
nMOSFET cross section

in 'Silicon-on-Insulator' (SOI) technology
Terms: Burried Oxide (BOX), shallow trench insulation (STI).
'Native' means no doping.



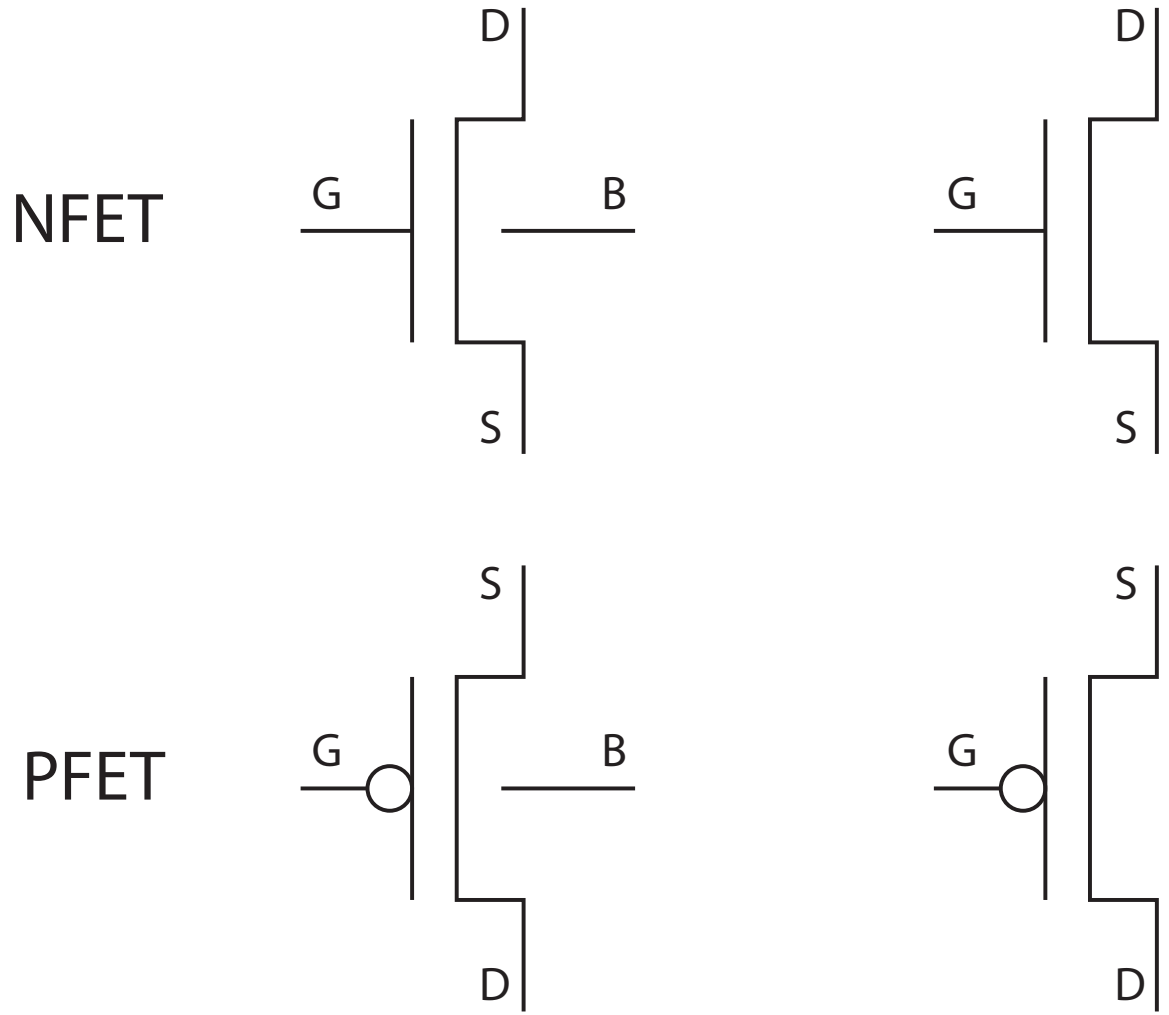
nMOSFET cross section

(in 'FinFET' technology)
Here the cross section is across the channel, i.e. not along the channel, so source and drain terminals are not visible, just the gate (PO). Can be both SOI (shown here) or Bulk (not shown) technology.



FET Device Symbols

(as used in the compendium. Other variations exist)



Transistor Modelling

Mathematical transistor models in the following describe the relation between the terminal voltages and the drain current specifically.

$$I_D = f(V_G, V_S, V_D, V_B)$$

Usually we will define $V_B := 0\text{V}$, and the equation can then be expressed as

$$I_D = f(V_G, V_D, V_S)$$

And as both V_G and V_D only appear as differences with V_S in the actual model we will introduce (see EKV model), i.e. $V_{GS} := V_G - V_S$ and $V_{DS} := V_D - V_S$, an often preferred form is:

$$I_D = f(V_{GS}, V_{DS}, V_S)$$

and oftentimes it is the case that V_S is kept at $V_S = V_B := 0$. So V_S and V_B can then be considered parameters, rather than variables and the only input variables left are $V_G = V_{GS}$ and $V_D = V_{DS}$:

$$I_D = f(V_G, V_D) = f(V_{GS}, V_{DS})$$

Transistor Model Parameters

We will encounter other internal parameters in those model functions, either 'process parameters' that are for example different in 28nm- or 7nm technology (the ones included in the follwing EKV model are: $\mu, C_{ox}, V_t, \lambda L, n$) or 'design parameters' that we can influence when drawing layout (namely the transistor size: W, L) or physical constants (U_T)

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Large Signal Models
- The EKV Model
- Simplified Equation for specific ROs

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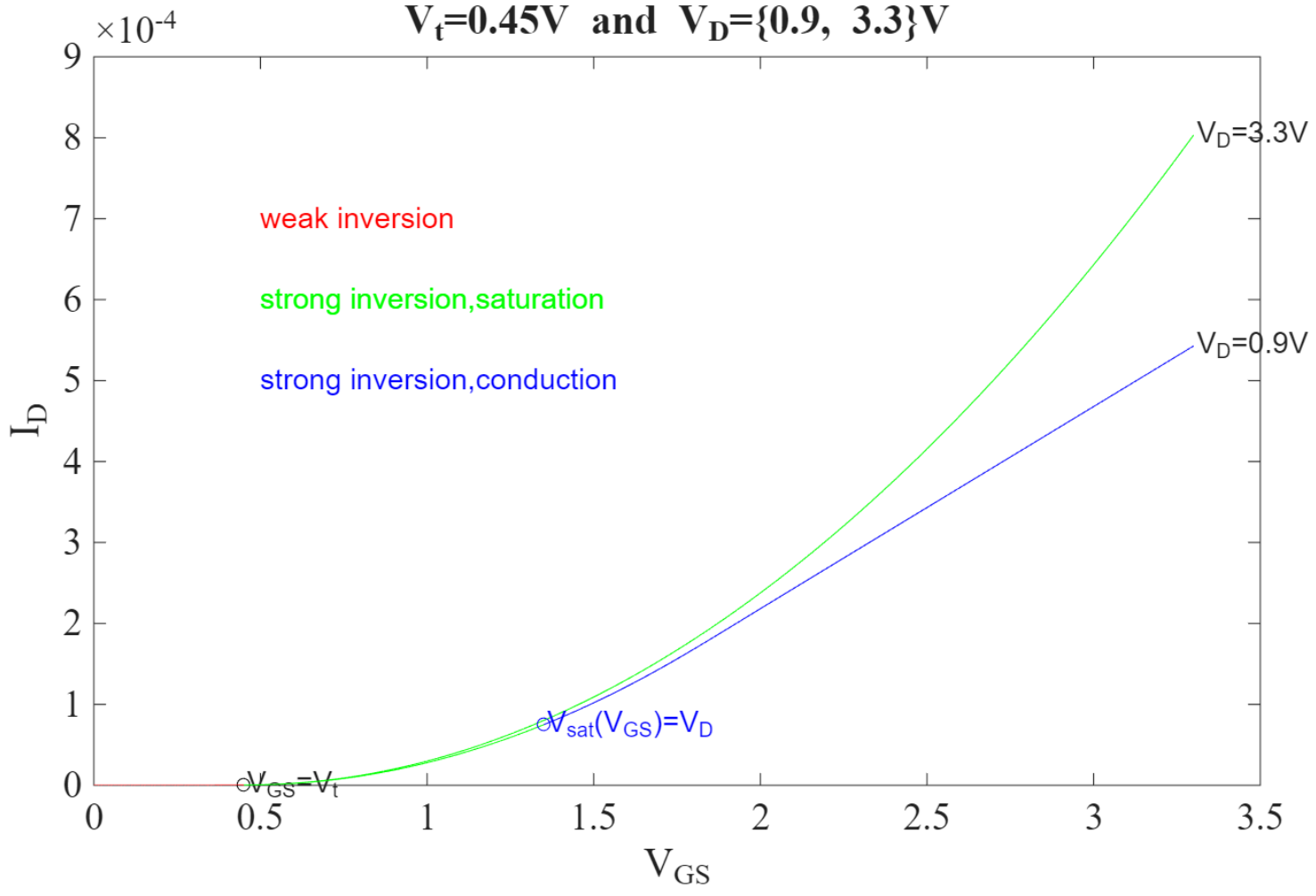
First MOSFET circuits

Large signal models of the MOSFET

Large signal models shall be the most complex introduced in this course, and are applicable for voltages on all terminals anywhere between the supply rails Vdd and $-Vss$. (Note: For digital circuits the reference voltage $Gnd := 0\text{V}$ is often identical to $Gnd := -Vss$. For analog circuits oftentimes we choose the reference between the supply rails $Vdd < Gnd < -Vss$.)
Assuming constant V_B and V_S we can graphically show the transistor behaviour as the previously mentioned 2D function $I_D = f(V_{GS}, V_{DS})$ and for example show cross sections of that function by keeping one of the two variables constant and sweeping the other (see next slides).

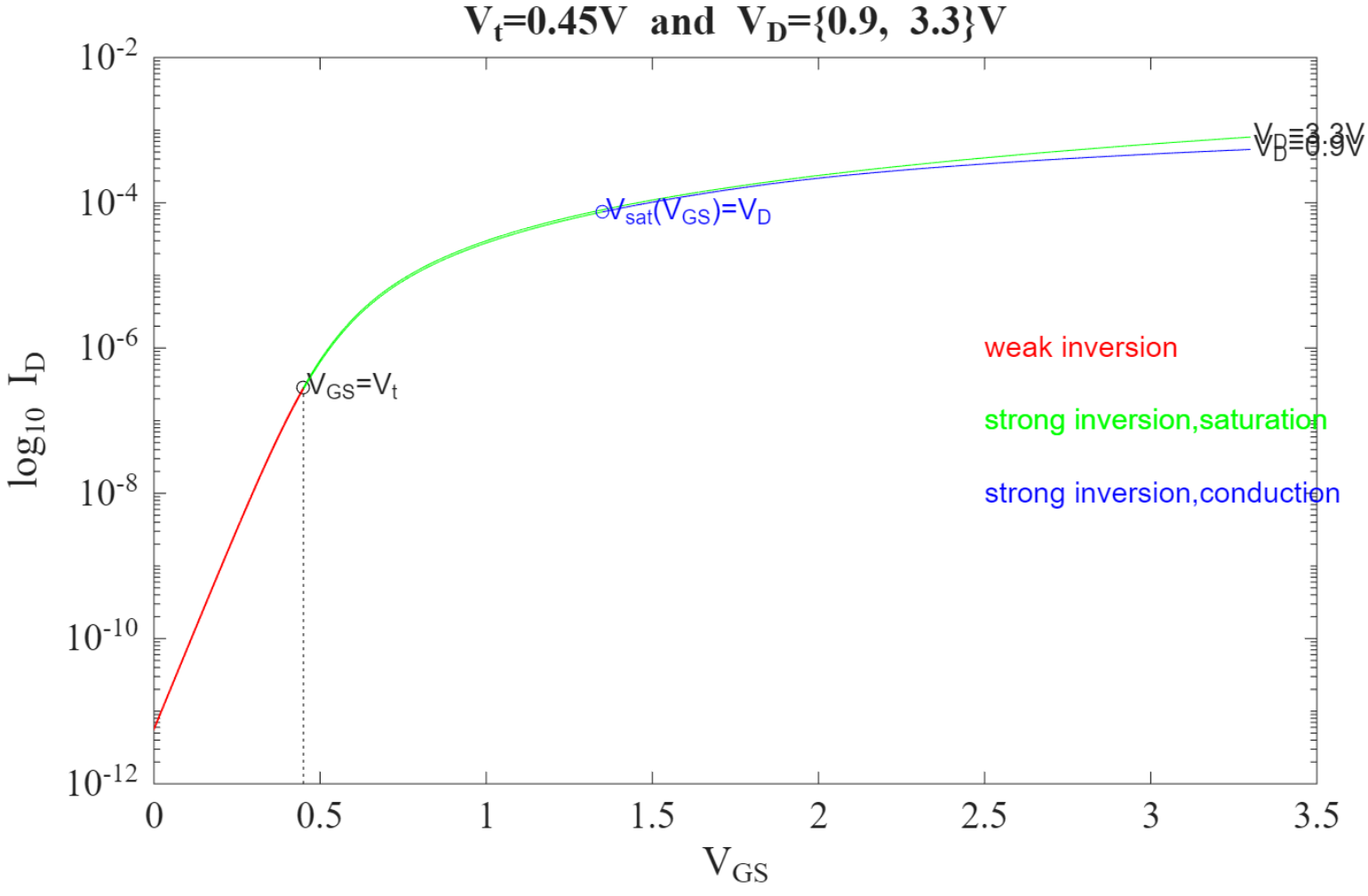
MOSFET large signal model snapshots (1/3)

When keeping V_D constant and sweeping V_G ($V_{GS} := V_G - V_S$):



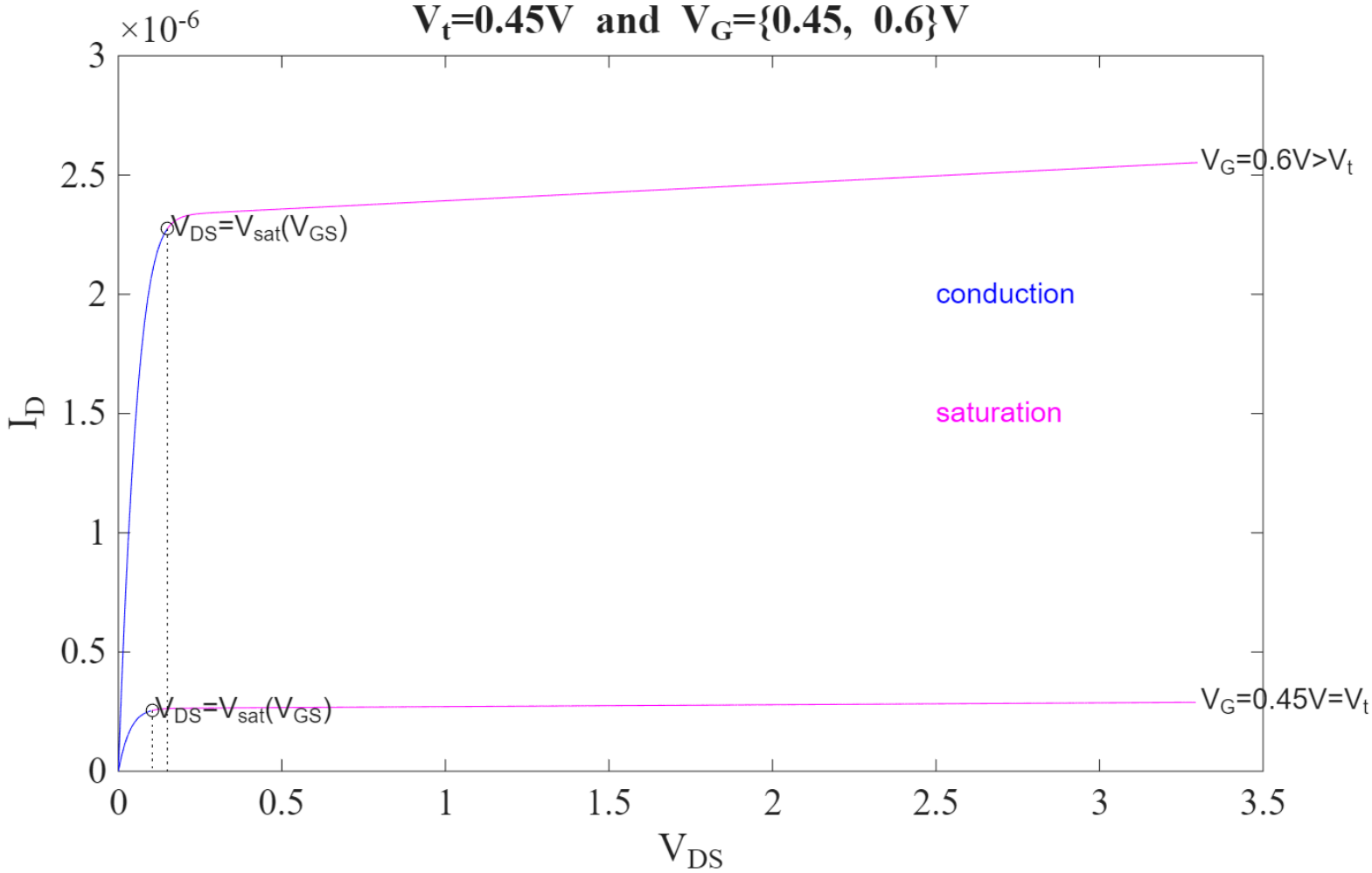
MOSFET large signal model snapshots (2/3)

When keeping V_D constant and sweeping V_G with log scale Y-axis:



MOSFET large signal model snapshots (3/3)

When keeping V_G constant and sweeping V_D ($V_{DS} := V_D - V_S$):



EKV Model nFET

$$I_D = I_F - I_R$$

I_D is defined as the current *into* the drain terminal. The forward current I_F in the direction of I_D and the reverse current I_R in the opposite direction. For nFETs:

$$I_{F(R)} = I_S \ln^2 \left[1 + e^{\frac{\left[V_G - V_{S(D)}\right] + (n-1)\left[V_B - V_{S(D)}\right] - V_t}{2nU_T}} \right] (1 + \lambda |V_D - V_S|)$$

Only 4 independent parameters: $\boldsymbol{I_S}$, $\boldsymbol{V_t}$, $\boldsymbol{n}$, and $\boldsymbol{\lambda}$. Some of them are composed of several interdependent parameters:

$$I_S = 2nkU_T^2$$

and

$$k = \mu C_{ox} \frac{W}{L}$$

(P.S: do not be intimidated! This full EKV we will never use for hand calculations.)

EKV Model Parameters

Process parameters (given by specific CMOS production process):
the threshold voltage $\boldsymbol{V_t}$,
the carrier mobility $\boldsymbol{\mu}$,
the gate oxide capacitance per area $\boldsymbol{C_{ox}}$,
the slope factor $\boldsymbol{n}$ (indicates effectiveness of V_G vs V_B, $1 \leq n < 2$ and usually $n \approx 1$),
λ' to derive the channel length modulation parameter $\boldsymbol{\lambda}$ that is $\lambda' = \boldsymbol{\lambda L} = \frac{1}{V'_A}$

Design parameters (can be chosen at design time):
channel width $\boldsymbol{W}$ and channel length $\boldsymbol{L}$

Physical constants:
The thermal voltage (simplifyingly assumed to be constant here) $\boldsymbol{U_T} = \frac{kT}{q_e} \approx 26\text{mV@}300^o K$ (k: Boltzmann constant, q_e: electron charge, T: temperature)

Variable Names (1/2)

Vdd: upper supply voltage

-Vss: lower supply voltage, voltage of ASIC P- substrate

Gnd: ambiguous! Either lower supply voltage, mostly in digital (Gnd:=-Vss), or signal zero reference in analogue as well as generally in small signal representation.

Variable Names (2/2)

V_G: Example of a terminal voltage relative to an arbitrary global reference, e.g. -Vss, where it appears in an explicit difference of voltages, e.g. $V_G - V_S$, **OR** terminal voltage relative to V_B where it does *not* appear in an explicit difference of voltages.

V_{GS}: example of an abreviation for a difference of two voltages, here $V_{GS} := V_G - V_S$

V_{OV}: defined as $V_{OV} := V_G - V_S - V_t$, i.e. the voltage by which V_{GS} exceeds the treshold voltage V_t.

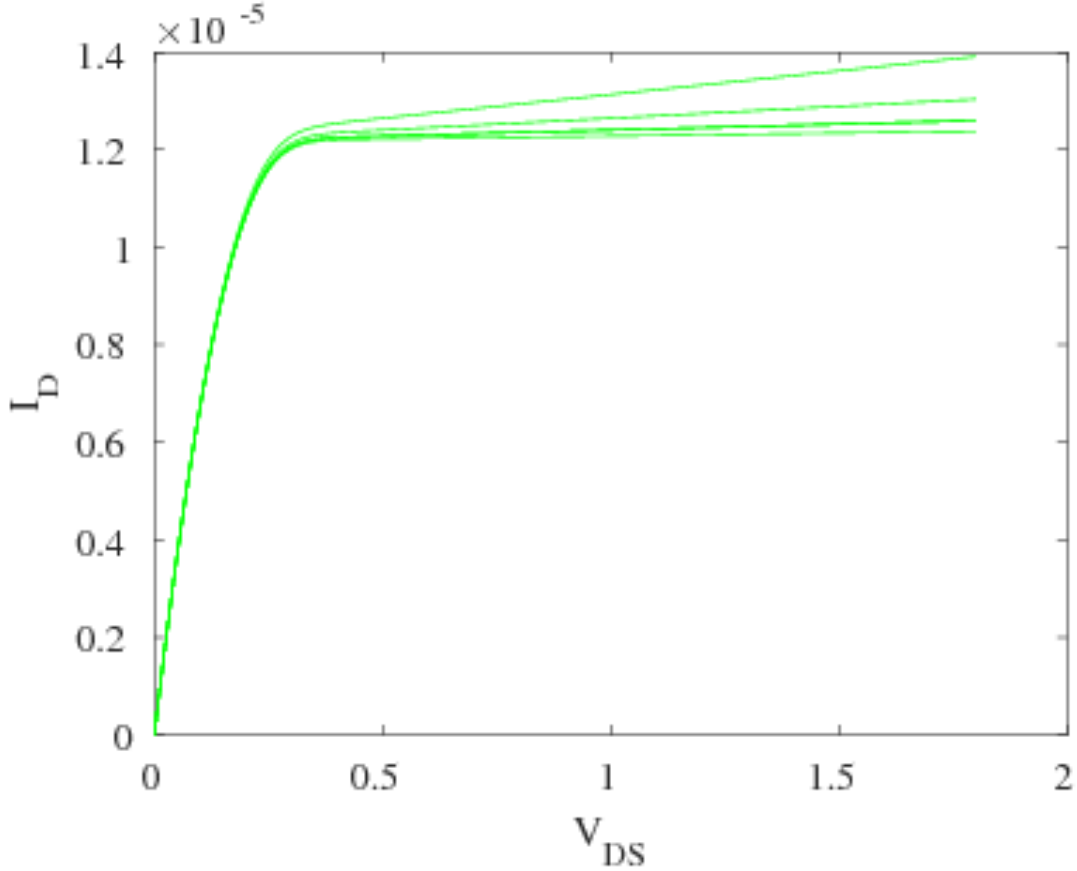
EKV Model pFET

For pFETs:

$$I_{F(R)} = -I_S \ln^2 \left[1 + e^{\frac{\left[V_{S(D)} - V_G\right] + (n-1)\left[V_{S(D)} - V_B\right] - V_t}{2nU_T}} \right] (1 + \lambda |V_D - V_S|)$$

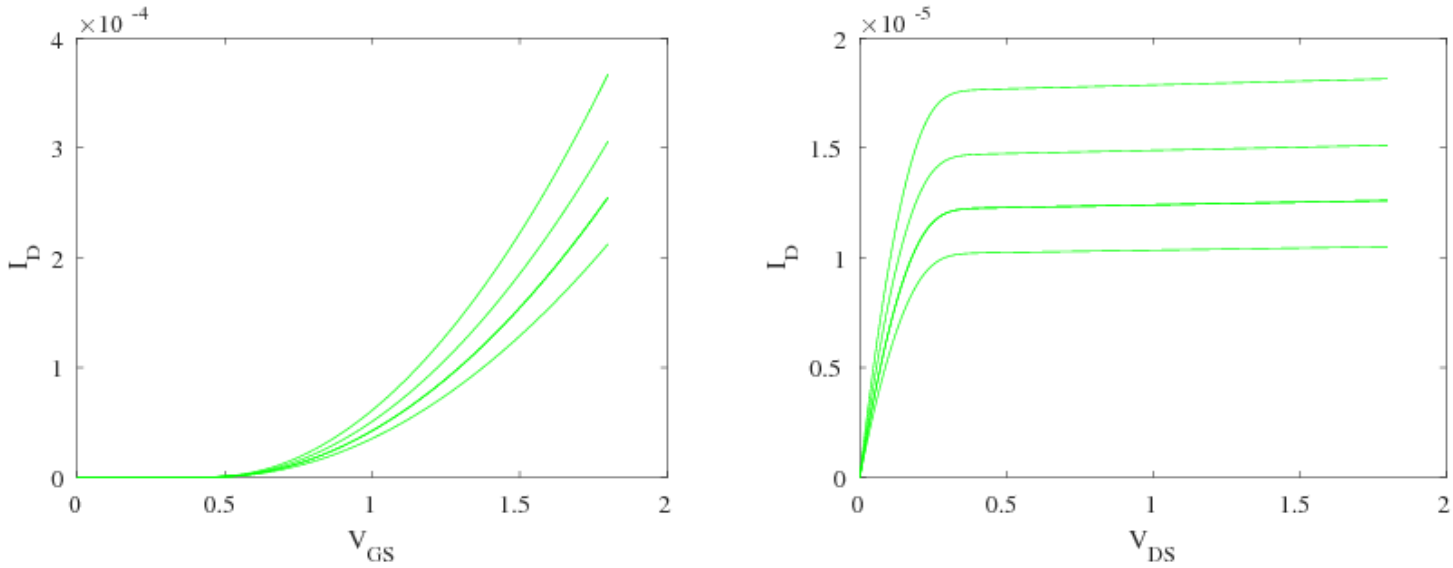
In the following we will assume that $|I_F| > |I_R|$ which is equivalent to saying that we define the drain and source terminals such that for nFETs $V_{DS} > 0$ and for pFETs $V_{SD} > 0$.

Effects of Parameter Tweaking: λ



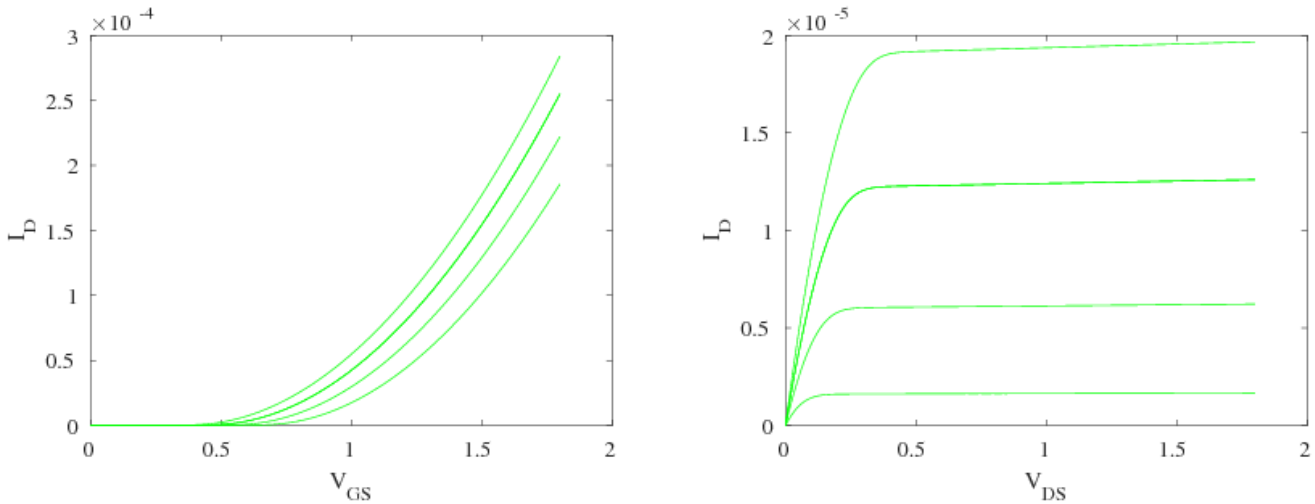
λ can be tweaked at design time by changing L, i.e. the actual process parameter is $L\lambda$ and $\lambda = \frac{L\lambda}{L}$ is 'tweakable' by L and derived from that parameter. λ is generally small and if $\lambda = 0$ the above curve becomes completely flat in saturation, i.e. an ideal current source.

Effects of Parameter Tweaking: I_S



I_S can be tweaked at design time by changing W/L but also depends on process parameters and U_T.

Effects of Parameter Tweaking: V_t



V_{tn}, V_{tp} cannot be tweaked at design time. They are process parameters.

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- Simplified Equation for specific ROs

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First MOSFET circuits

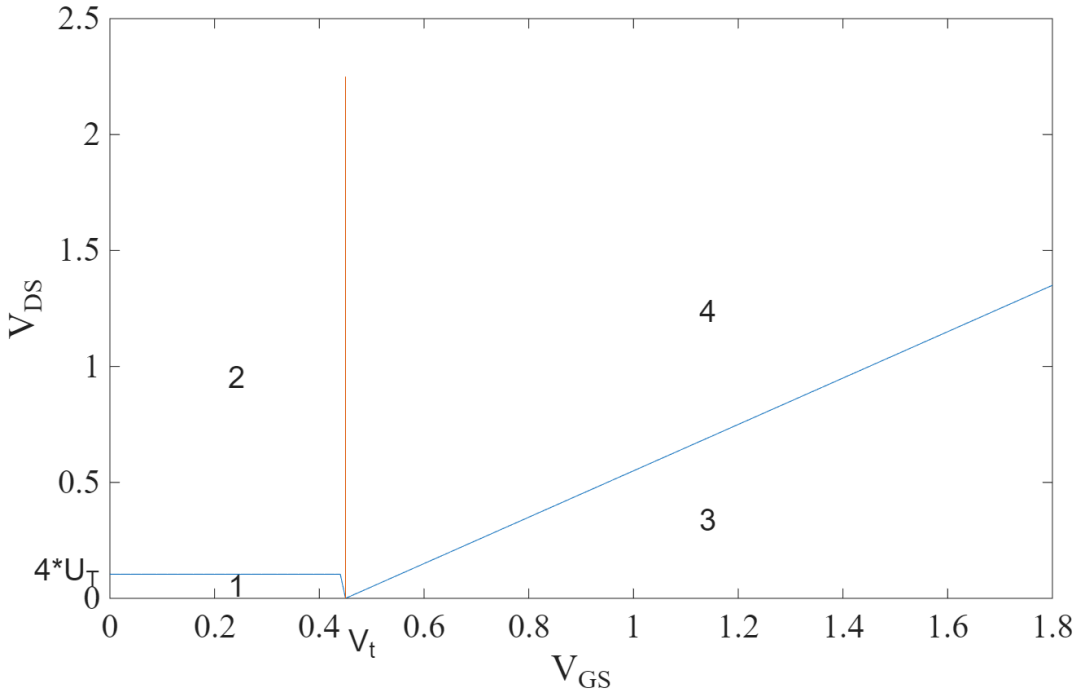
Simplified Equations for specific ROs

Note: in the following we'll define V_B as the zero reference for all voltages:

$$V_B := 0\text{V}$$

So some equations will become simpler.

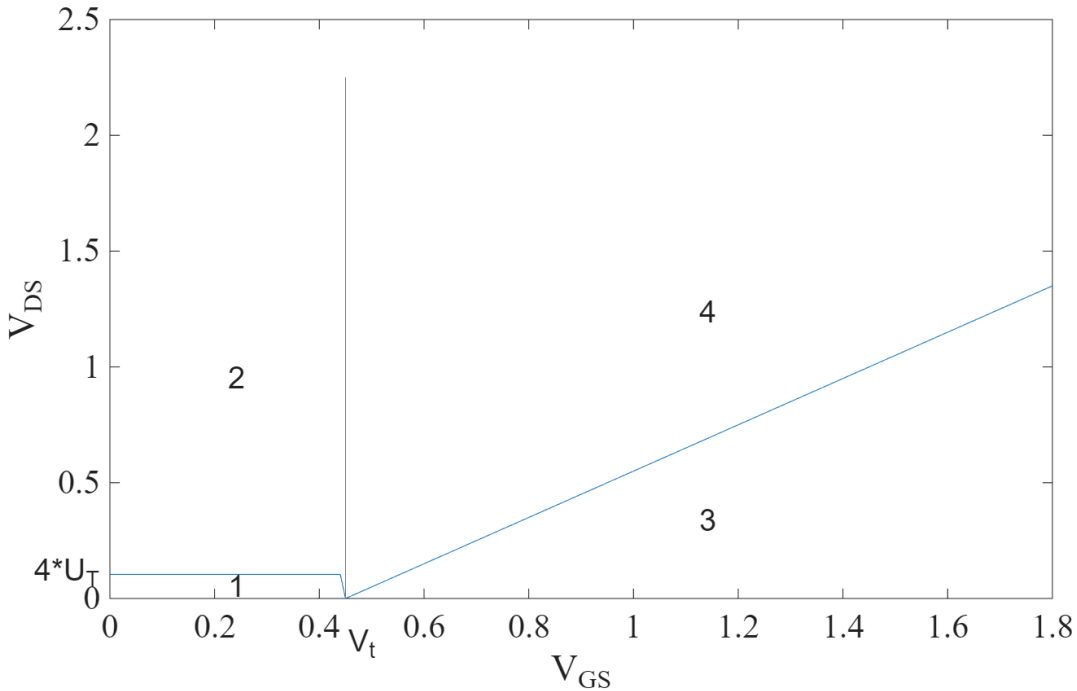
Regions of operation (1/2)



1. weak inversion, conduction
2. weak inversion, saturation
3. strong inversion, conduction
4. strong inversion, saturation

There are simplified equations for **4** different regions. The blue line separates the conduction (bottom) from the saturation region (top), the red the weak inversion (left) from the strong inversion region (right). IMPORTANT: the simplified equations are NO GOOD close to the separation lines!!!

Regions of operation (2/2)



1. weak inversion, conduction
2. weak inversion, saturation
3. strong inversion, conduction
4. strong inversion, saturation

Note that different names for these regions are also used in literature, for example:
'linear-/triode-' for 'conduction'
'active' for 'saturation'
'above threshold' for 'strong inversion'
'sub-threshold' for weak 'inversion'

Distinction Weak- vs Strong Inversion

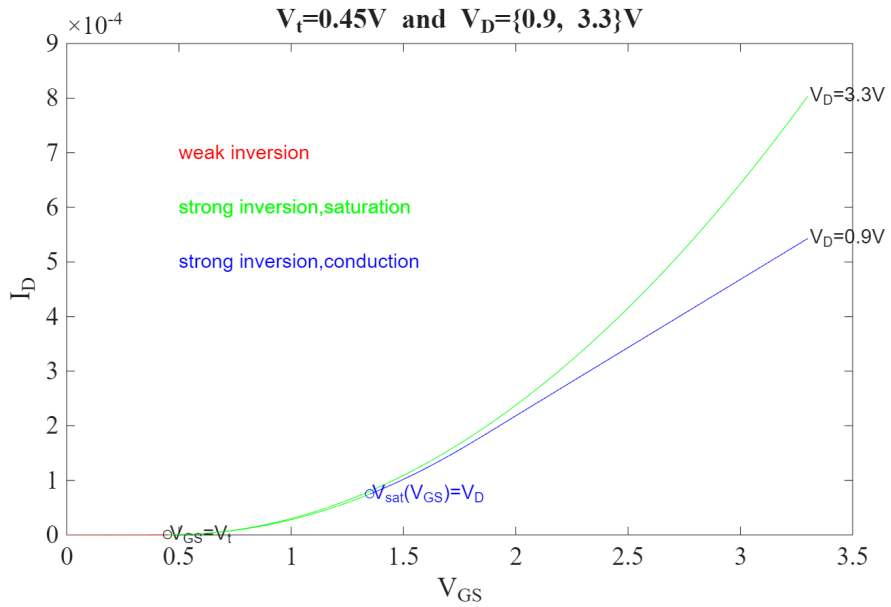
Weak inversion:

$$I_F << I_S \Leftrightarrow V_{GS} << V_t$$

Strong inversion:

$$I_F >> I_S \Leftrightarrow V_{GS} >> V_t$$

(that's for nFETs)



Destinction Conduction vs Saturation

Conduction:

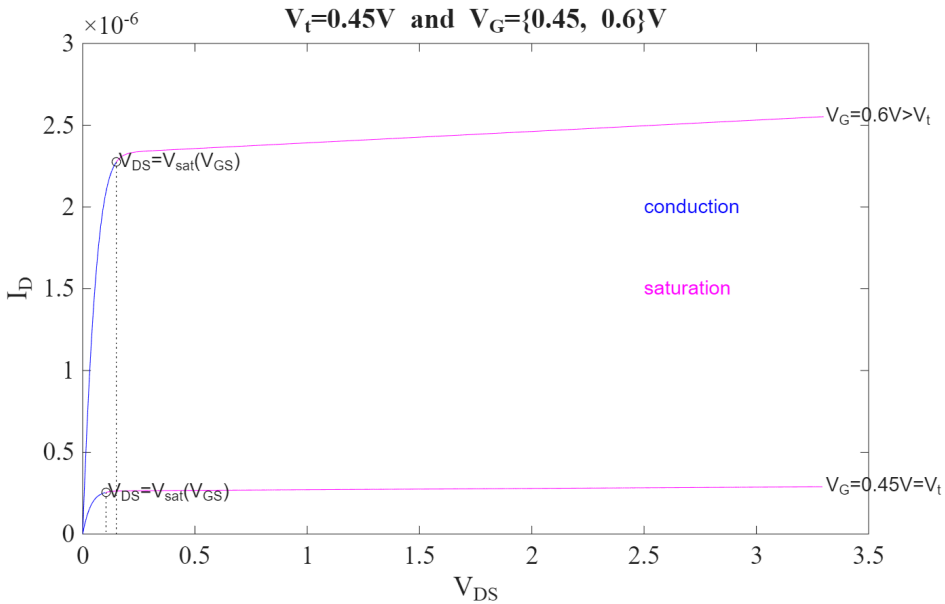
$$I_F \approx I_R \Leftrightarrow V_{DS} << V_{sat}$$

Saturation:

$$I_F >> I_R \Leftrightarrow V_{DS} >> V_{sat}$$

1. in weak inversion: $V_{sat} := 4U_T$ (i.e. constant)
2. in strong inversion: $V_{sat} := V_{OV}$ (i.e. scaling with V_{GS}!)

(that's for nFETs)



strong inversion, saturation

$$\begin{aligned} I_D &= \frac{1}{2n} k_n \left(V_G - V_{tn} - nV_S\right)^2 \left(1 + \lambda V_{DS}\right) \\ &= \frac{1}{2n} k_n \left(V_{ov} - (n-1)V_S\right)^2 \left(1 + \lambda V_{DS}\right) \end{aligned}$$

I_D vs V_{GS} is a square function where:

$$I_D \propto \left(V_G - nV_S - V_t\right)^2$$

I_D vs V_{DS} is a linear function where:

$$I_D \propto \left(1 + \lambda V_{DS}\right)$$

weak inversion, saturation

$$I_D = I_S e^{\frac{V_G - V_{tn} - nV_S}{nU_T}} (1 + \lambda V_{DS})$$

So for I_D vs V_{GS} the behaviour is exponential ($I_D \propto e^{\frac{V_{GS} - V_t}{nU_T}}$).

And for I_D vs V_{DS} we get a linear and usually very 'flat' (i.e. near ideal current source) relationship ($I_D \propto (1 + \lambda V_{DS})$).

strong inversion, conduction

$$I_D = k_n V_{DS} \left[V_G - V_{tn} - \frac{n}{2}(V_D + V_S) \right]$$

I_D vs V_{GS} is a linear function.

I_D vs V_{DS} in deep conduction is a linear function where for $V_{BS} = 0$ and $V_{DS} << V_{OV}$ the first order Taylor expansion in V_{DS} results in the behaviour of a resistor:

$$I_D = k_n V_{OV} V_{DS} \Rightarrow g_{DS} = k_n V_{ov}$$

weak inversion, conduction

$$I_D = I_S e^{\frac{V_G - V_{tn}}{nU_T}} \left(e^{\frac{-V_S}{U_T}} - e^{\frac{-V_D}{U_T}} \right)$$

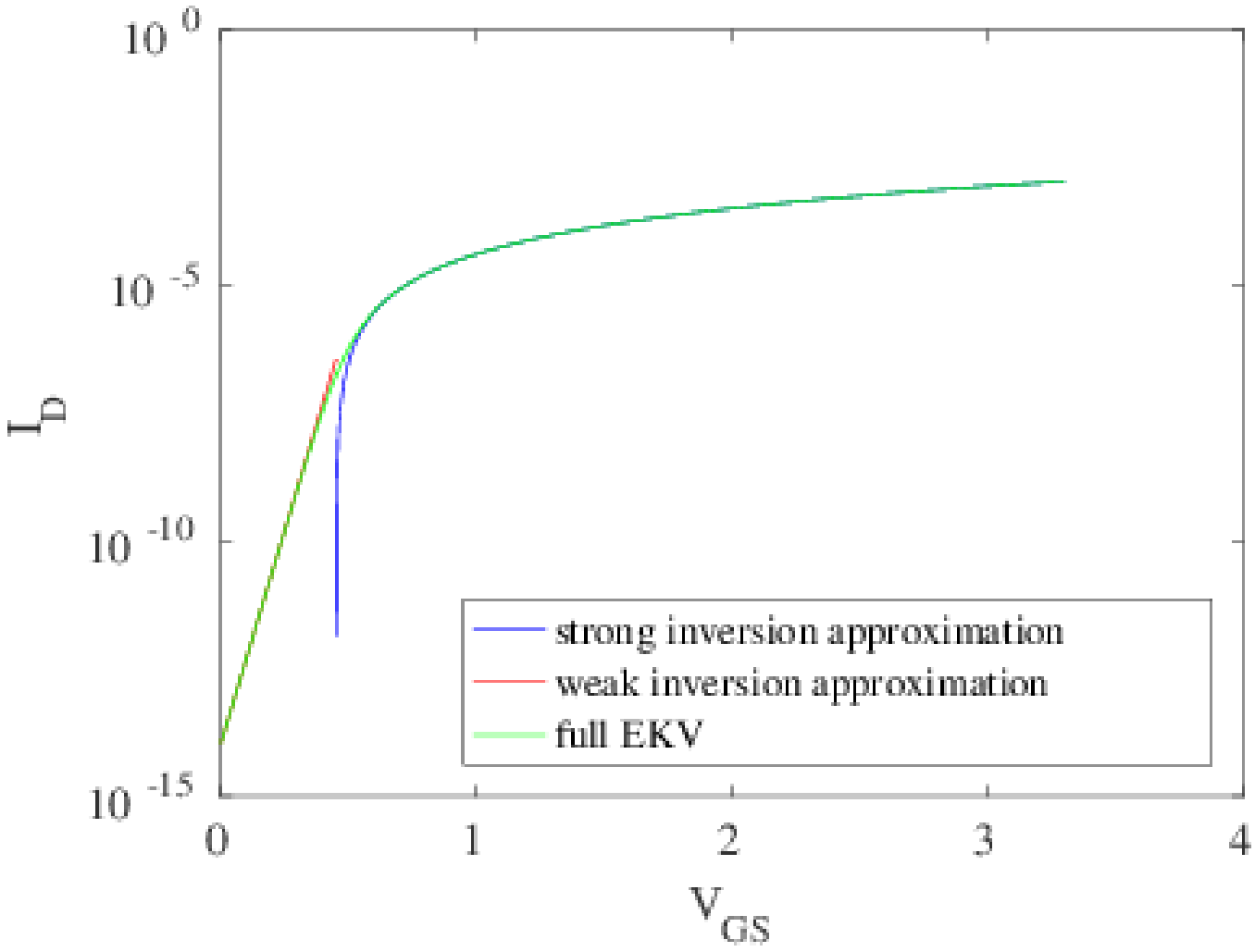
So for I_D vs V_{GS} an exponential law applies, same as in saturation but with a scaling factor 'reducing' I_S.

For I_D vs V_{DS} close to the origin $V_{DS} << V_{sat}$ (1st order Taylor expansion around $V_{DS} = 0$):

$$I_D = I_S e^{\frac{V_{ov}}{nU_T}} \frac{V_D}{U_T} \Rightarrow g_{DS} = I_S e^{\frac{V_{OV}}{nU_T}} \frac{1}{U_T}$$

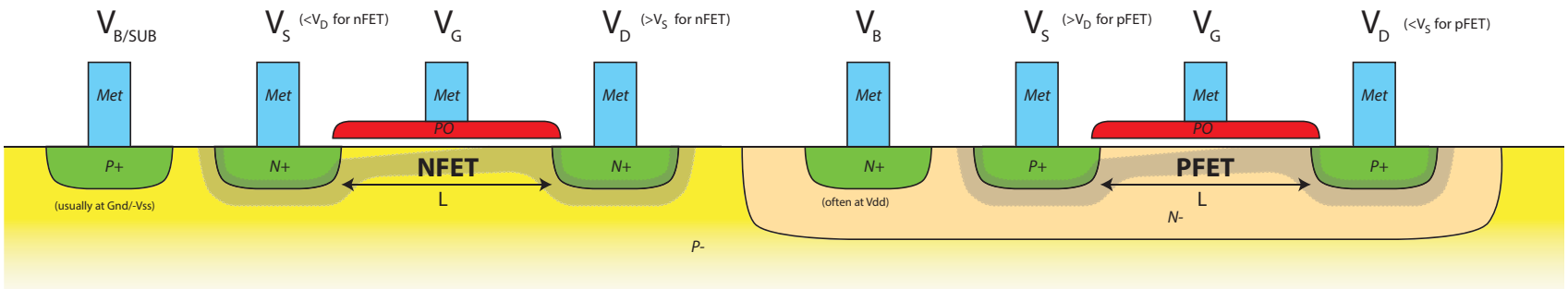
So you can model the behaviour with respect to V_{DS} as a simple resistor $r_{DS} = \frac{1}{g_{DS}}$

Illustration I_D vs V_{GS}



nFET/NMOS and pFET/PMOS cross section

(in 'Bulk' technology)



'Parasitic' Capacitors

$$C_{GD} = L_{OV} W C_{OX}$$

$$C_{GS} \approx \left(\frac{2}{3} WL + WL_{OV} \right) C_{OX}$$

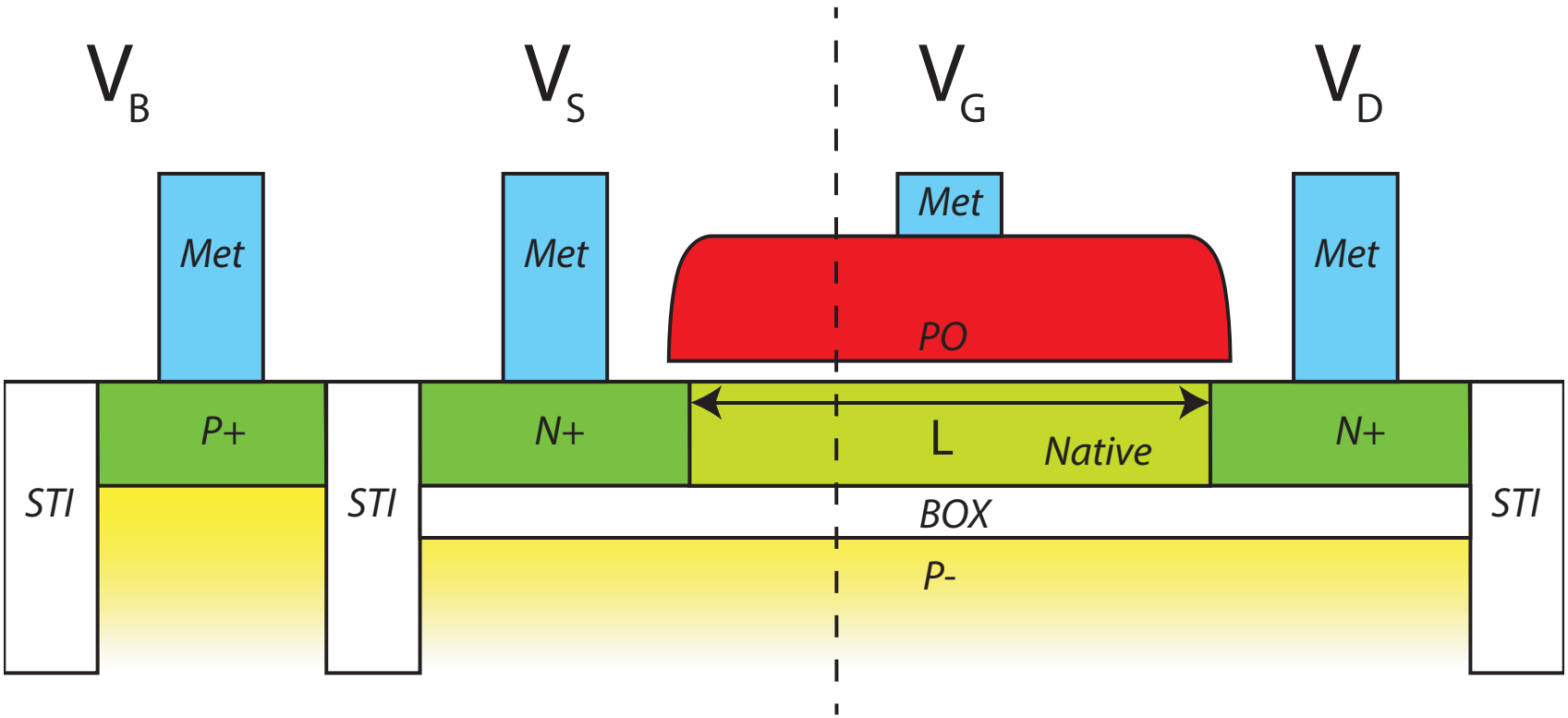
$$\begin{aligned} C_{DB} &= C_J A_D \\ C_{SB} &\approx C_J A_S + \frac{2}{3} WL C_{ChB} \end{aligned}$$

If the layout of the S/B terminals are rectangular with a width equal to the channel width W and constant length $L_{S/D}$:

$$A_{S/D} = W L_{S/D}$$

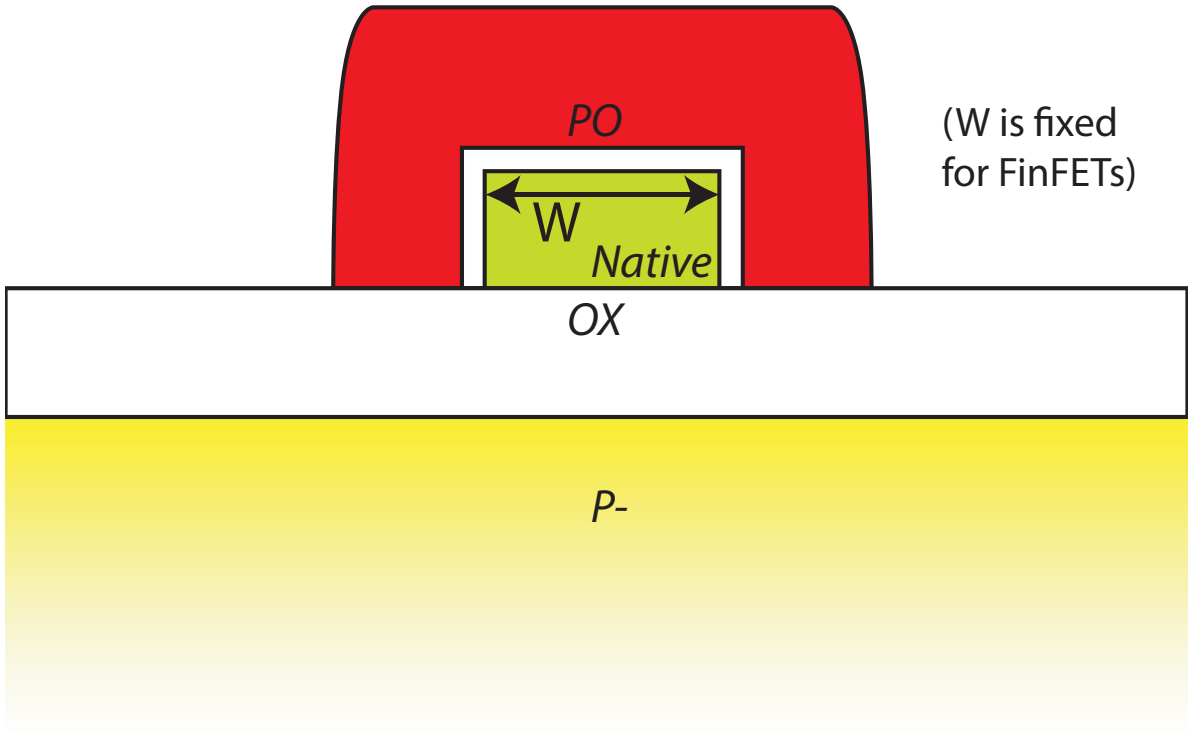
nFET cross section

(in Silicon on Insulator (SOI) technology)



nFET cross section

(in FinFET technology)



Content

Field Effect Transistor (FET) Cross Sections

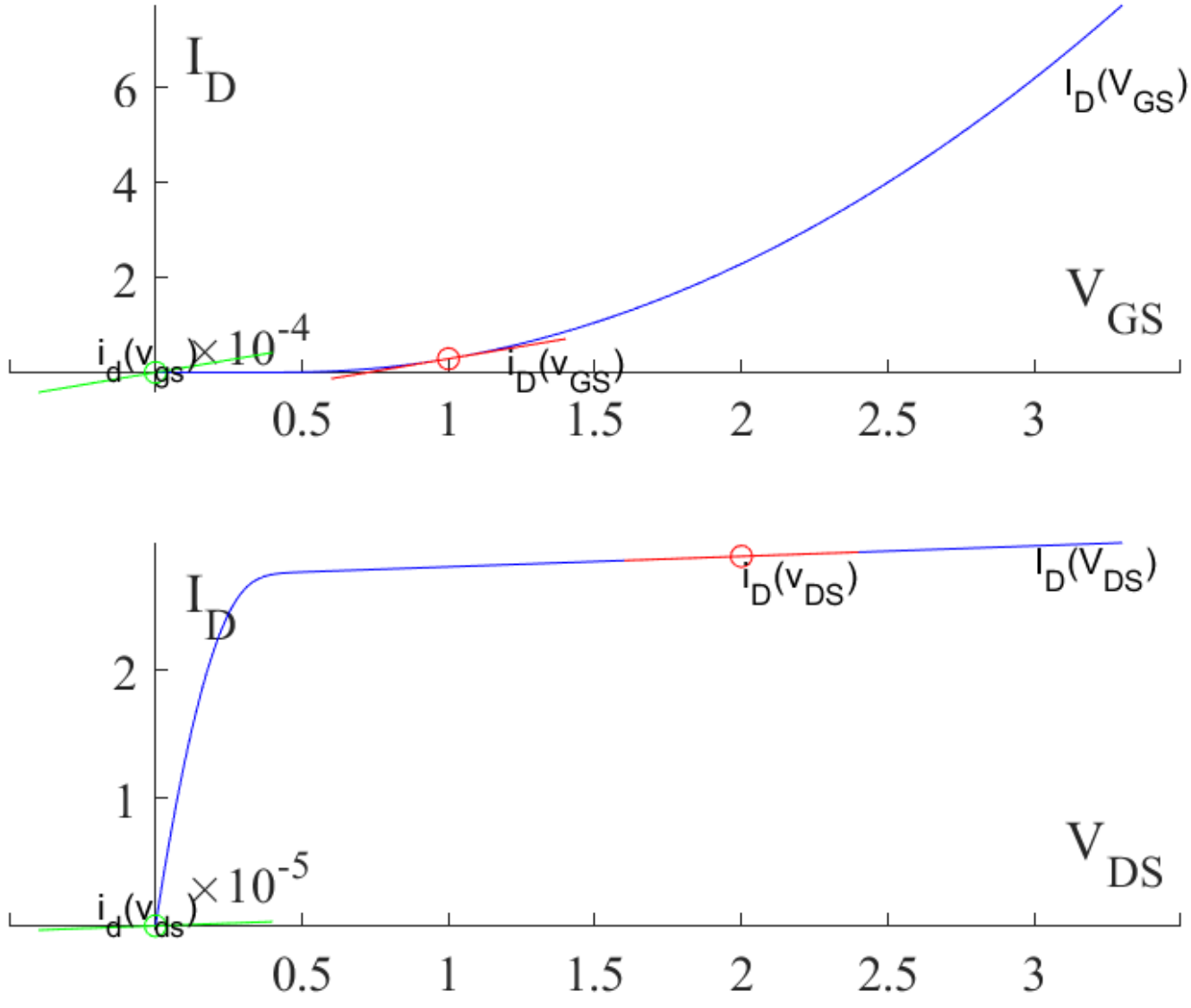
Large Signal Models

Small Signal Models

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First MOSFET circuits

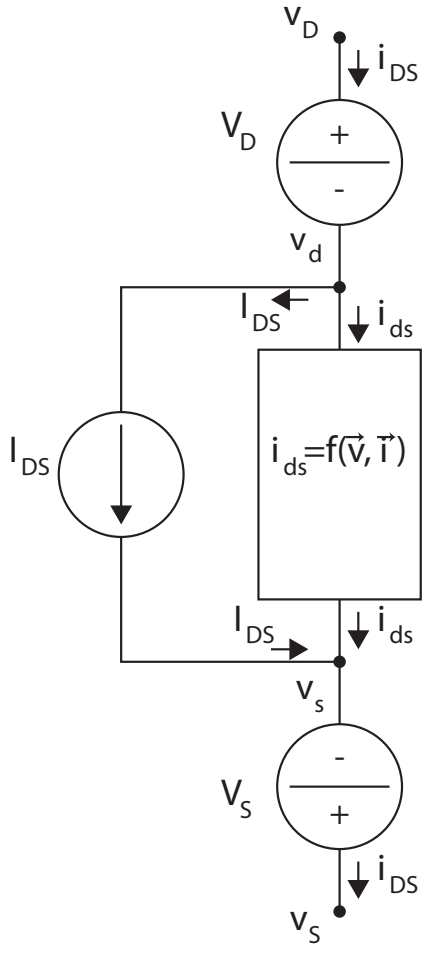
Approximate FET as linear element at point of operation

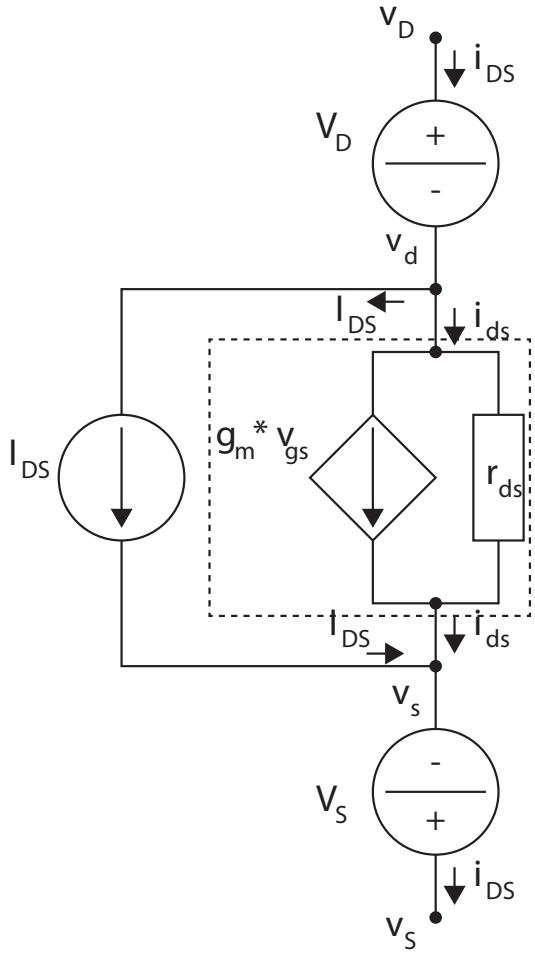


Taylor expansion at point of operation

$$i_{DS} = I_{DS}(V_{GS}, V_{DS}) + \delta v_{GS} * \frac{\delta I_{DS}}{\delta V_{GS}} + \delta v_{DS} * \frac{\delta I_{DS}}{\delta V_{DS}}$$

FET Taylor expansion equivalent circuit





$$g_m := \frac{\delta I_{DS}}{\delta V_{GS}}$$

$$g_{ds} := \frac{1}{r_{ds}} := \frac{\delta I_{DS}}{\delta V_{DS}}$$

Small Signal Parameters(1/2)

g_m for strong inversion, saturation:

$$g_m = \frac{dI_D}{dV_{GS}} = \sqrt{2k_n I_D}$$

g_m for strong inversion, conduction:

$$g_m = \frac{dI_D}{dV_{GS}} = k_n V_{DS}$$

g_m for weak inversion:

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{I_D}{U_T}$$

Small Signal Parameters(2/2)

r_{ds} in saturation:

$$r_{ds} = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$

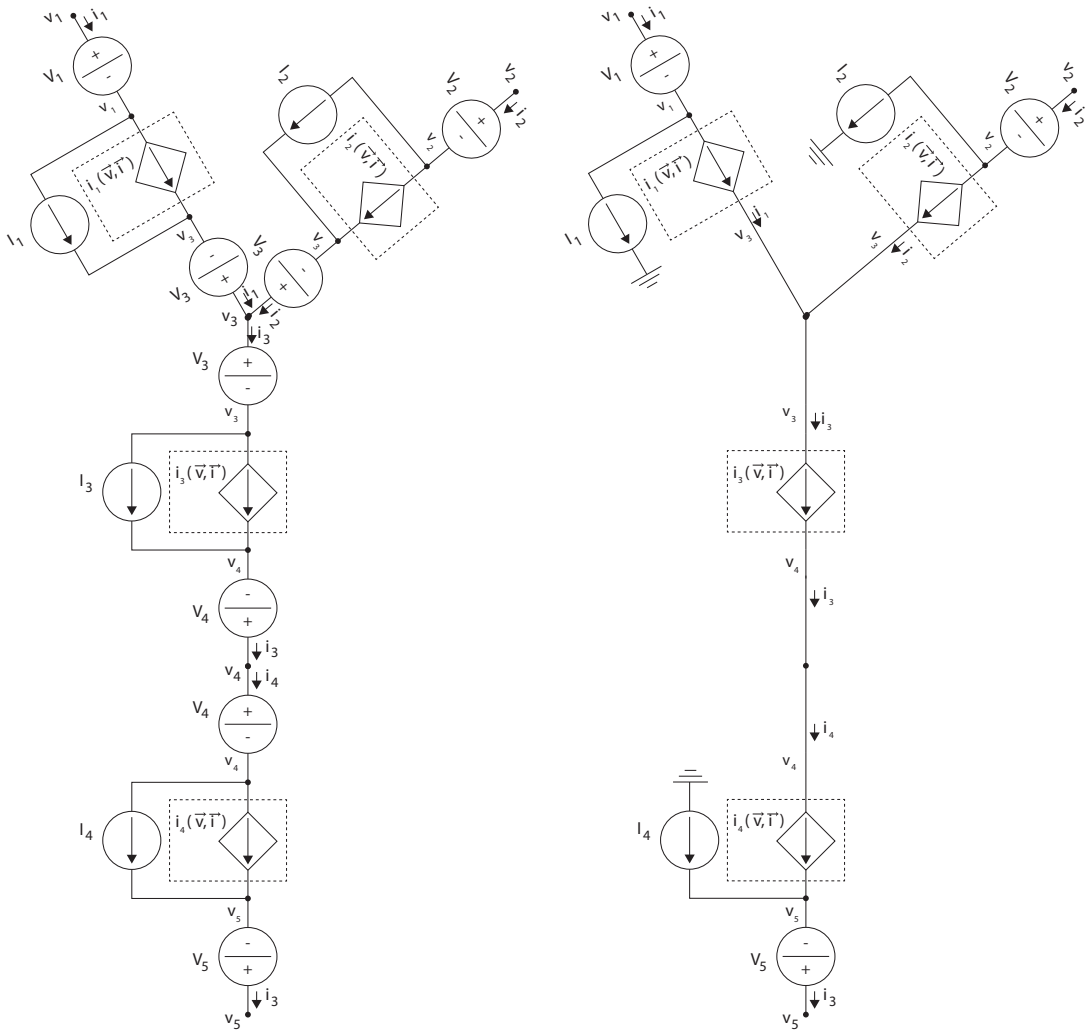
r_{ds} in deep conduction, strong inversion:

$$r_{ds} = \frac{1}{kV_{OV}}$$

r_{ds} in deep conduction, weak inversion:

$$r_{ds} = \frac{1}{I_S U_T} e^{-\frac{V_{OV}}{nU_T}}$$

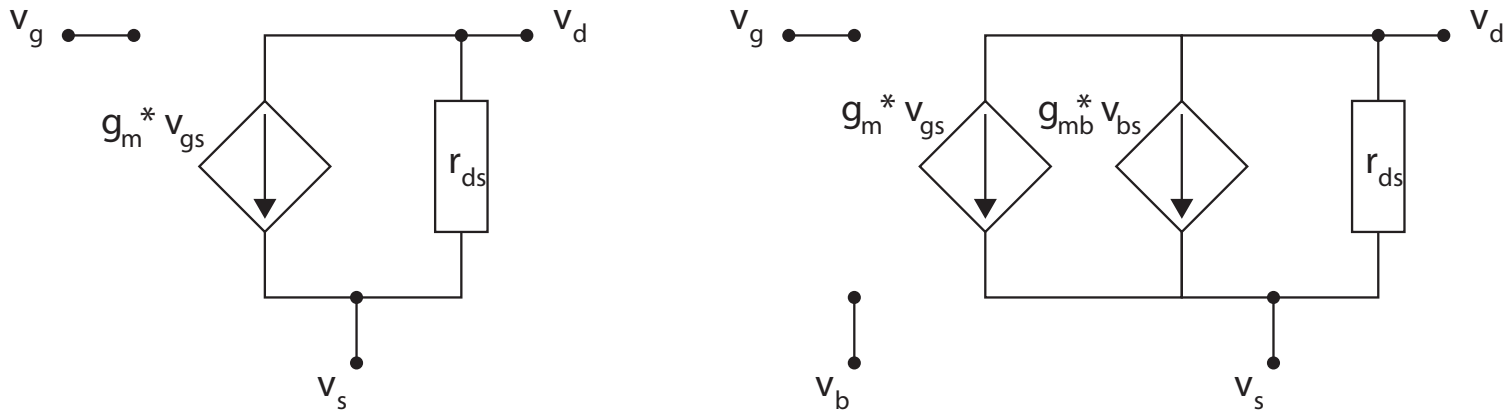
Small signal equivalent circuits



Eliminating the point of operation (also called 'biasing point') from analysis.

FET small signal equivalent circuit

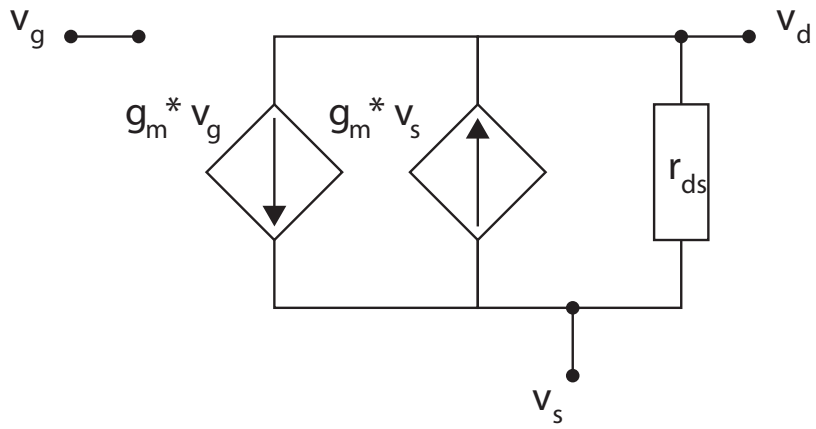
(Left: $V_{BS} = 0$, Right: $V_{BS} \neq 0 \wedge n \neq 1$)



$$g_{mb} = (n-1)g_m$$

FET small signal equivalent circuit variant

$(V_{BS} = 0)$

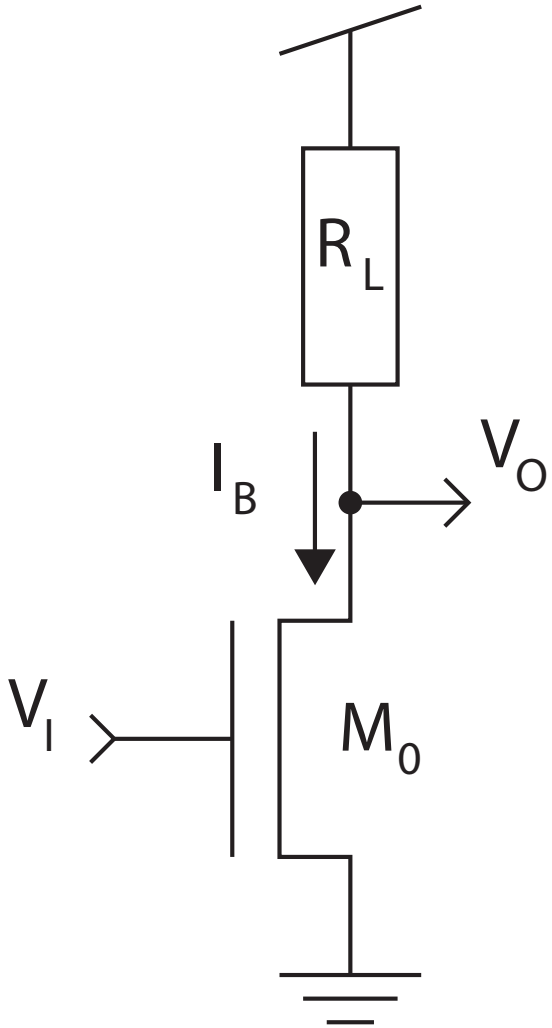


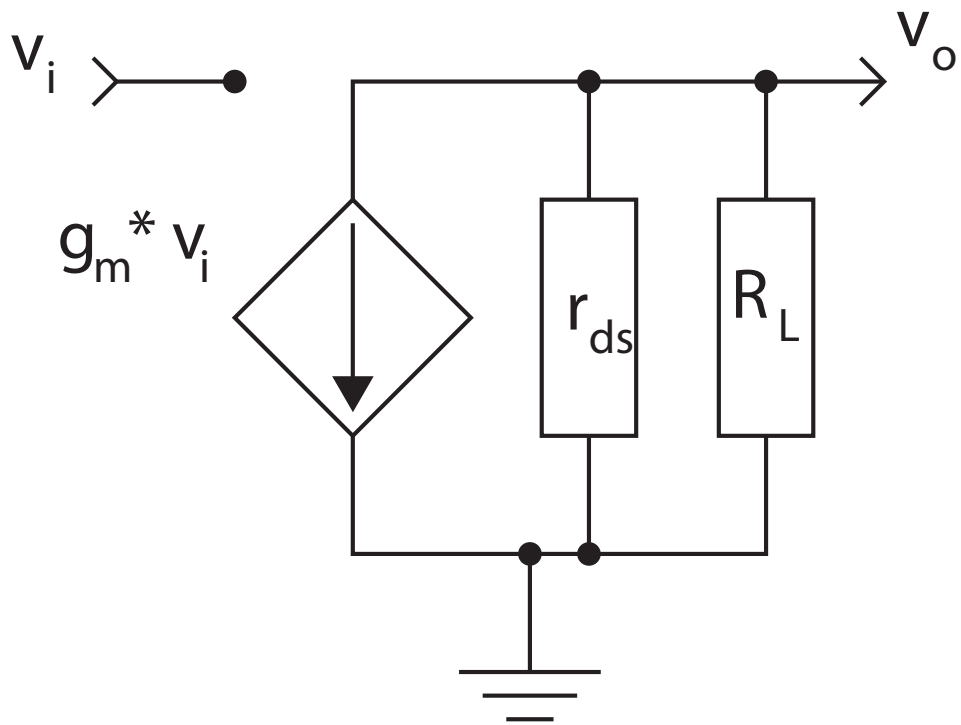
Applying small signal analysis

1. Fully determine the point of operation, i.e. all biasing parameters.
2. Derive small signal parameters (e.g. g_m and r_{ds}) based on that point of operation.
3. Replace all circuit elements with their small signal equivalent.
4. Remove all independent/constant current sources and replace all independent/constant voltage sources with Gnd (i.e. NOT the current sources that depend on a small signal input such as the $i_{ds} = g_m V_{gs}$).
5. perform a normal Kirchhoff's or Ohm's law analysis of the circuit.

Small Signal Analysis Example Step 3 & 4

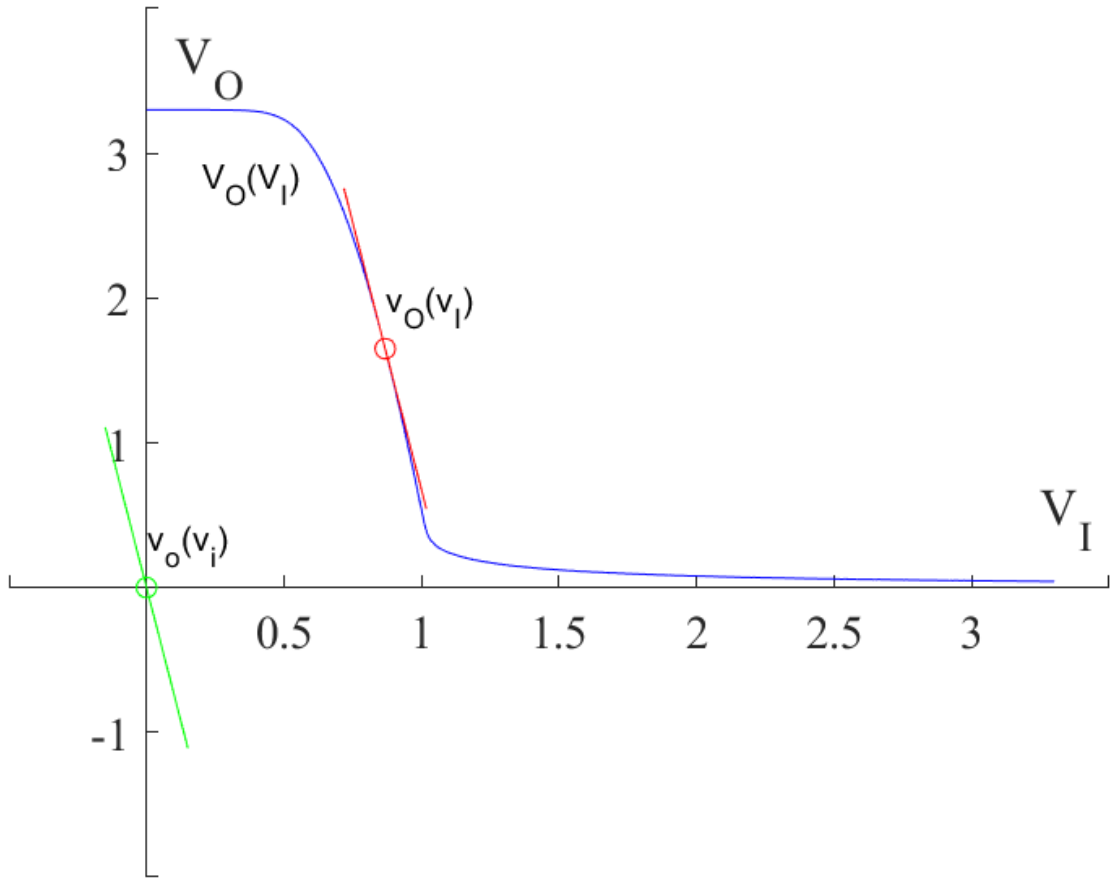
Let's start with steps 3 and 4:





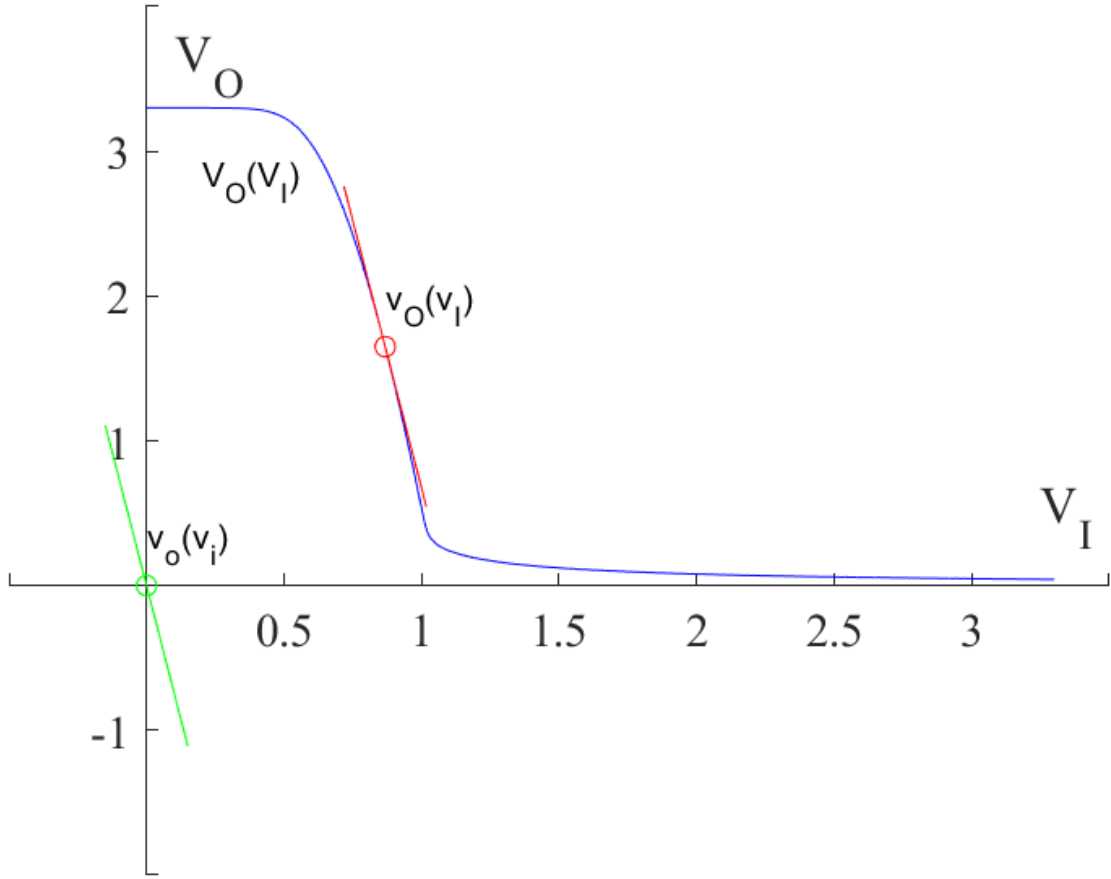
Small Signal Analysis Example Step 1 & 2

For steps 1 and 2 we need the **large signal model!** Where does this circuit operate as intended (amplifier)? Which are the regions of operation for the NFET for different parts of the curve?



Small Signal Analysis Example Step 1

Given:
Vdd $= 3.3$V
Vss $:= 0V$
$V_S = V_B = 0$V
$R_L =$1MΩ
$V_O := \frac{\text{Vdd}}{2}$
Parameters:
$I_S = 50$nA
$V_{tn} = 0.5$V
$\lambda = 0.05\frac{1}{\text{V}}$
$n = 1$
Asked:I_B, V_I, and A



Small Signal Analysis Example Step 1

$$V_O = \frac{\text{Vdd}}{2} = 1.65\text{V} \ \wedge \ R_L = 1\text{M}\Omega$$

$$\Rightarrow$$

$$I_B = \frac{V_O}{R_L} = 1.65\mu\text{A} \ (> I_S)$$

Small Signal Analysis Example Step 1

$$I_D = \frac{1}{2n} k_n \left(V_G - V_{tn} - nV_S\right)^2 \left(1 + \lambda V_{DS}\right)$$

$$\Rightarrow$$

$$\frac{I_D 2n}{k_n \left(1 + \lambda V_{DS}\right)} = \left(V_G - V_{tn} - nV_S\right)^2$$

$$\frac{I_D 2n}{\frac{I_S}{2nU_T^2} \left(1 + \lambda V_{DS}\right)} = \left(V_G - V_{tn} - nV_S\right)^2$$

$$\frac{I_D 4n^2 U_T^2}{I_S \left(1 + \lambda V_{DS}\right)} = \left(V_G - V_{tn} - nV_S\right)^2$$

$$V_G = 2nU_T \sqrt{\frac{I_D}{I_S \left(1 + \lambda V_{DS}\right)}} + V_{tn} + nV_S$$

Small Signal Analysis Example Step 1

$$V_I = 2 * 26\text{mV}\sqrt{\frac{1.65\mu\text{A}}{50\text{nA}\left(1 + 0.05\frac{1}{\text{V}} * 1.65\text{V}\right)}} + 0.5\text{V}$$

$$V_I = 2 * 26 * 10^{-3}\text{V}\sqrt{\frac{1.65 * 10^{-6}\text{A}}{50 * 10^{-9}\text{A}\left(1 + 0.05\frac{1}{\text{V}} * 1.65\text{V}\right)}} + 0.5\text{V}$$

$$V_I = 0.79\text{V}$$

Small Signal Analysis Example Step 2

$$g_m = \sqrt{2k_n I_D} = \sqrt{2\frac{I_S I_D}{2nU_T^2}} = \frac{\sqrt{50 * 10^{-9}\mathrm{A} * 1.65 * 10^{-6}\mathrm{A}}}{26 * 10^{-3}\mathrm{V}} = 11.05\frac{\mu\mathrm{A}}{\mathrm{V}}$$

$$r_{ds} = \frac{1}{\lambda I_D} = \frac{1}{0.05\frac{1}{\mathrm{V}}1.65 * 10^{-6}\mathrm{A}} = 12.12\mathrm{M}\Omega$$

Small Signal Analysis Example Step 5

$$g_m v_i + v_o\left(\frac{1}{r_{ds}} + \frac{1}{R_L}\right)$$

$$v_o = -g_m v_i \frac{1}{\frac{1}{r_{ds}} + \frac{1}{R_L}}$$

$$v_o = -g_m v_i \left(r_{ds} || R_L\right)$$

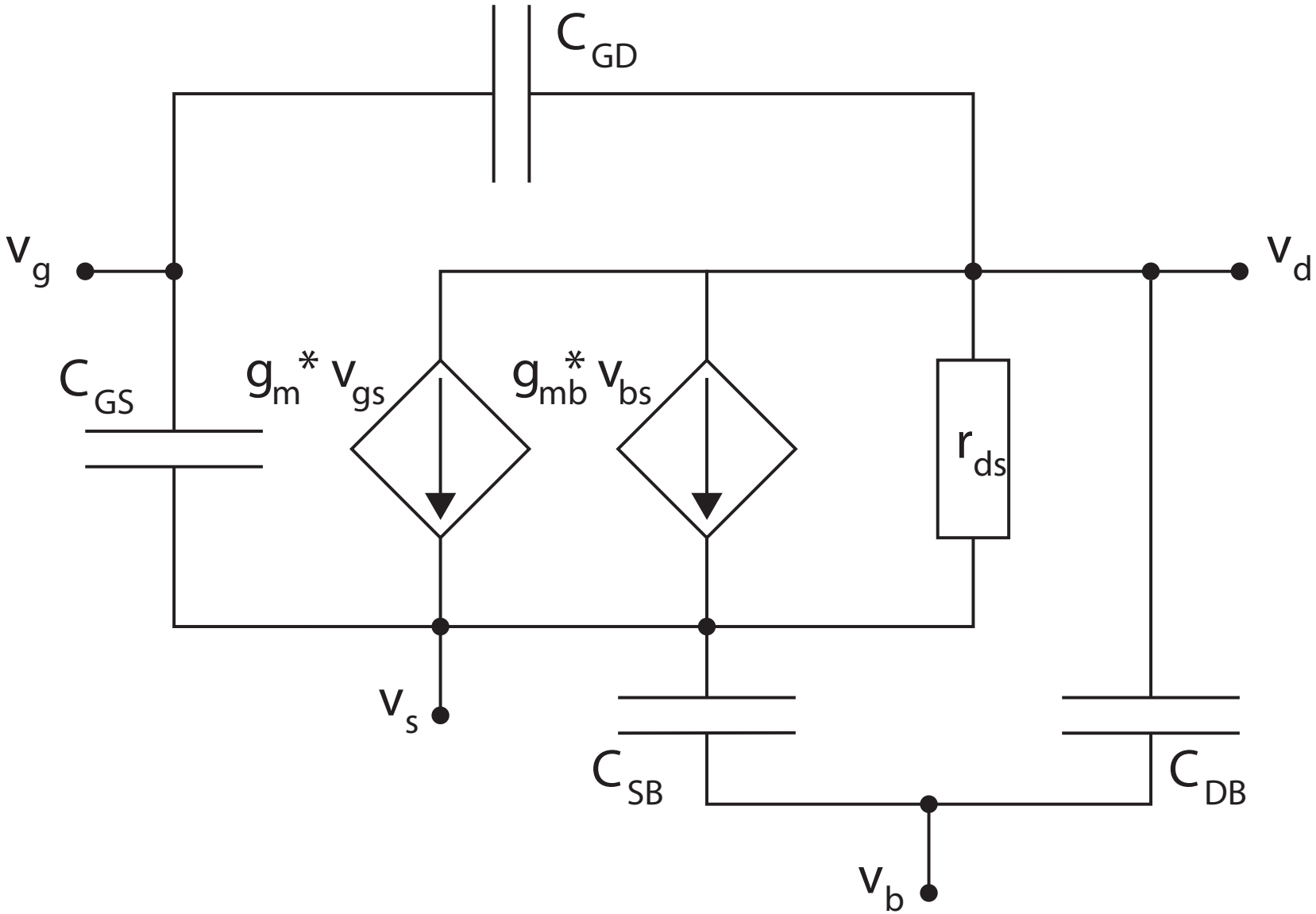
$$A := \frac{v_o}{v_i} = -g_m \left(r_{ds} || R_L\right) = -g_m \frac{r_{ds} R_L}{r_{ds} + R_L}$$

Since $r_{ds} >> R_L$ it follows that $(r_{ds} || R_L) \approx R_L$, but let's compute the exact value:

$$(r_{ds} || R_L) = 0.923\text{M}\Omega$$

$$A = 10.2$$

FET HF Small Circuit Equivalent



Content

Field Effect Transistor (FET) Cross Sections

Large Signal Models

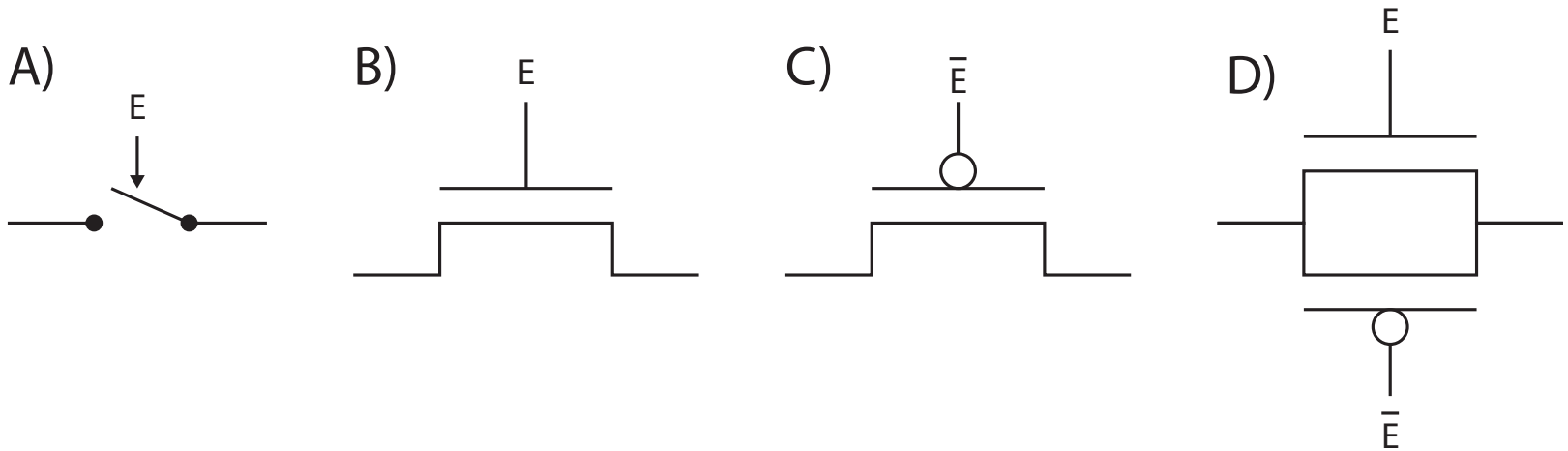
Small Signal Models

Switch Models

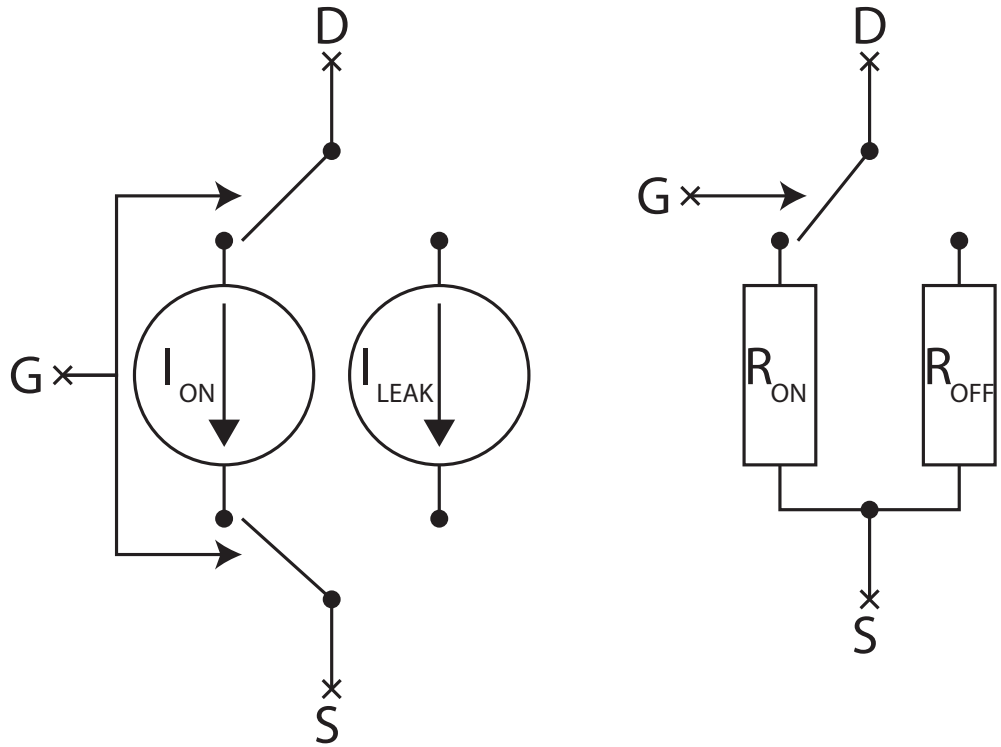
First MOSFET circuits

Practical implementation of switches

Regarding transistors as voltage controlled switches.
Question: why is version D) more universally applicable? What's a potential issue with B) and C)?

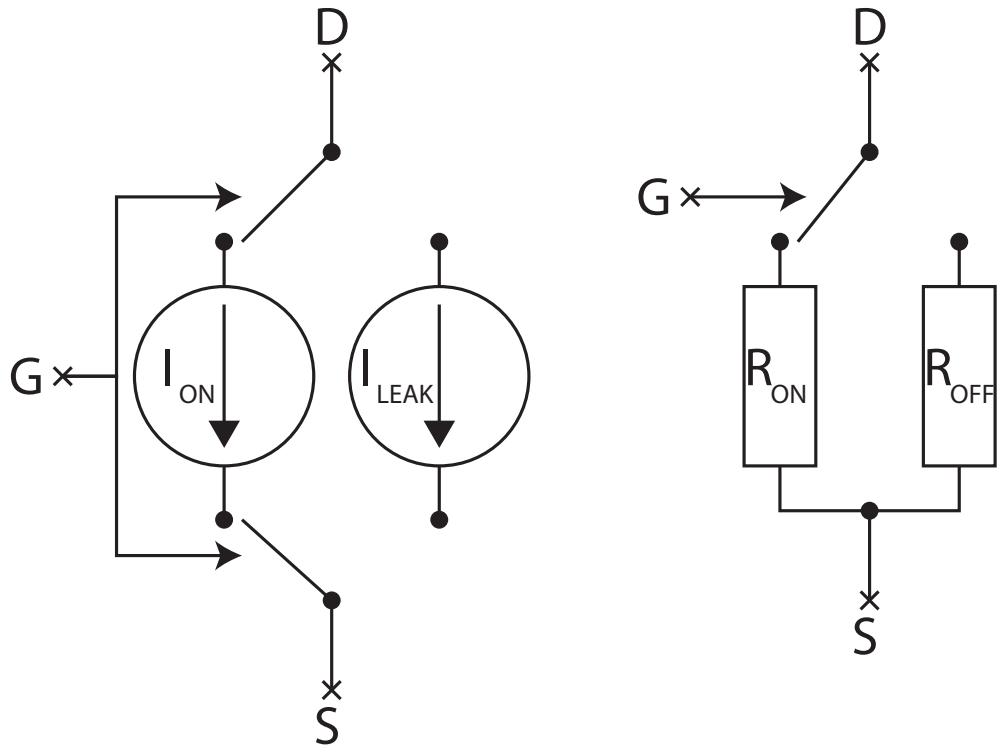


Models for nFET assuming V_S is constant (1/2)



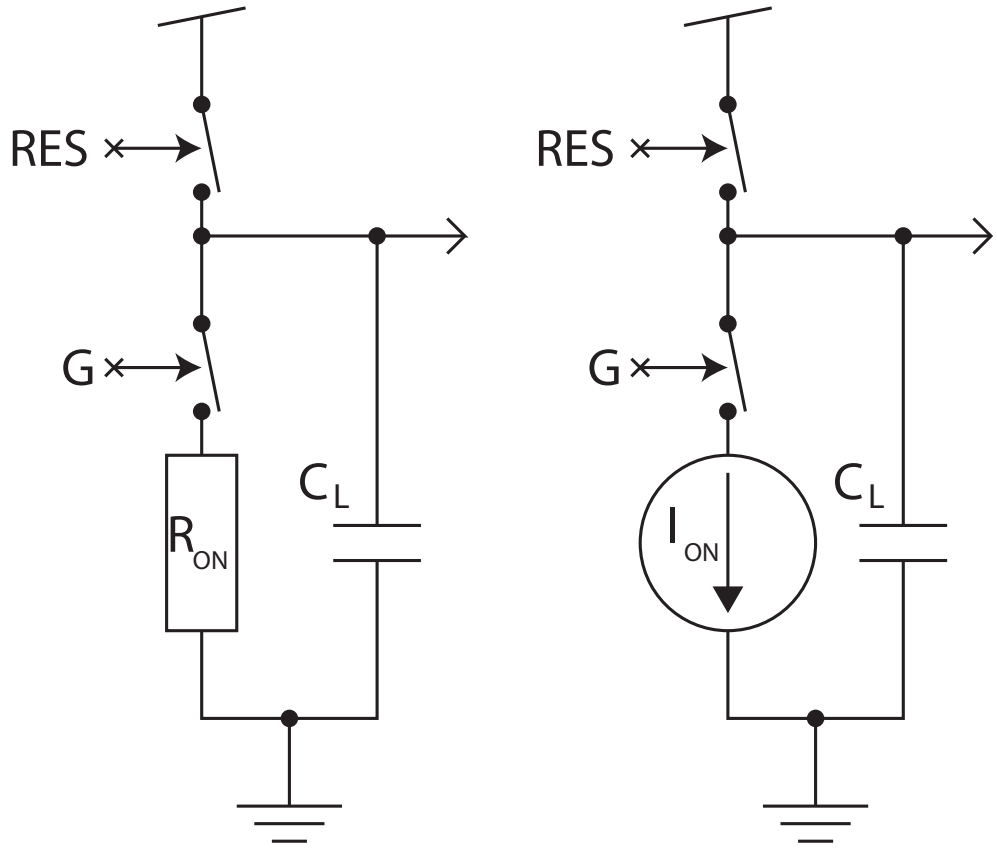
Most common use in digital circuits as switches pulling a signal 'low' ('false', '0', 'L', using nFET!!!) or 'high' ('true', '1', 'H', using pFETs!!!),

Models for nFET assuming V_S is constant (2/2)



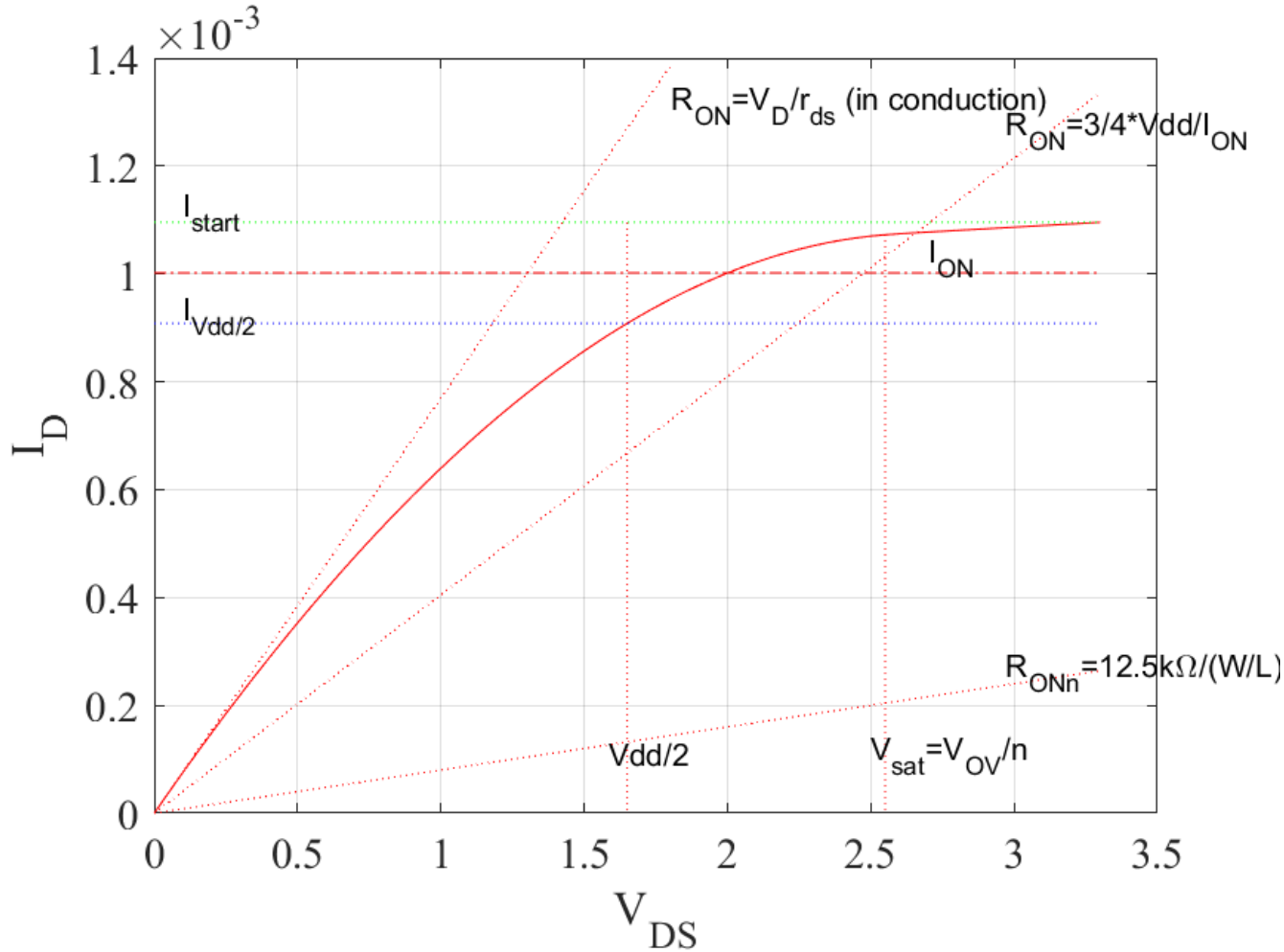
'high' and 'low' on spec-sheets of discreet components is being defined as voltages close to the supply rails with a certain tolerance, i.e. a minimum for 'high' and a maximum for 'low' and some area of uncertainty in-between. These models here, however, have only two states and no 'uncertainty', just a single **switching threshold** separating 'H' from 'L', usually $\frac{\text{Vdd}}{2}$.

Signal Propagation Delay



Progation delay is the time from the input reaching the switching threshold to the output reaching the switching threshold.

Approximations for I_{ON} and R_{ON}



With V_{GS} constant the current will follow the I_D vs V_{DS} curve (drawn out line). Approximations are for the current from Vdd to $\frac{\text{Vdd}}{2}$. Exception: $R_{ON} = V_D/r_{ds}$ can be used to model the output resistance *after* switching is complete.

Static output resistance after switch

This is so to speak the 'holding power' of the transistor:

$$R_{ON} = r_{ds}$$

using the deep conduction approximation for r_{ds}!

I_{ON} for transition from Vdd to $\frac{\text{Vdd}}{2}$

$$I_{ON} = \frac{I_{\text{start}} + I_{\frac{\text{Vdd}}{2}}}{2}$$

Closed form for strong inversion (assuming $n = 1$, $\lambda = 0$ and $V_S = V_B := 0\text{V}$):

$$I_{ON} = \frac{1}{4} k \text{Vdd}^2 \left[\left(\frac{3}{2} - \frac{V_t}{\text{Vdd}} \right)^2 - \frac{1}{2} \right]$$

Propagation delay

Defined as the time from the start of the switching (i.e. $V_G > V_{sw} := \frac{\text{Vdd}}{2}$) until the output reaches that same threshold.

$$t_p = \frac{\text{Vdd} C_L}{2 I_{ON}}$$

R_{ON} pragmatic crude approximation

$$R_{ON_n} = \frac{12.5}{\frac{W_n}{L_n}} \text{k}\Omega$$

$$R_{ON_p} = \frac{30}{\frac{W_p}{L_p}} \text{k}\Omega$$

R_{ON} better quantitative approximation

$$\frac{\frac{\mathrm{Vdd}}{R_{ON}} + \frac{\frac{\mathrm{Vdd}}{2}}{R_{ON}}}{2} = I_{ON}$$

$$\frac{3}{4}\frac{\mathrm{Vdd}}{R_{ON}} = I_{ON}$$

$$R_{ON} = \frac{3}{4}\frac{\mathrm{Vdd}}{I_{ON}}$$

Propagation delay

$$
\begin{aligned}
e^{\frac{-t_p}{R_{ON}C_L}} &= \frac{1}{2} \\
t_p &= -R_{ON}C_L \ln(\frac{1}{2}) \\
t_p &= 0.69 R_{ON} C_L
\end{aligned}
\tag{1}
$$

Content

Field Effect Transistor (FET) Cross Sections

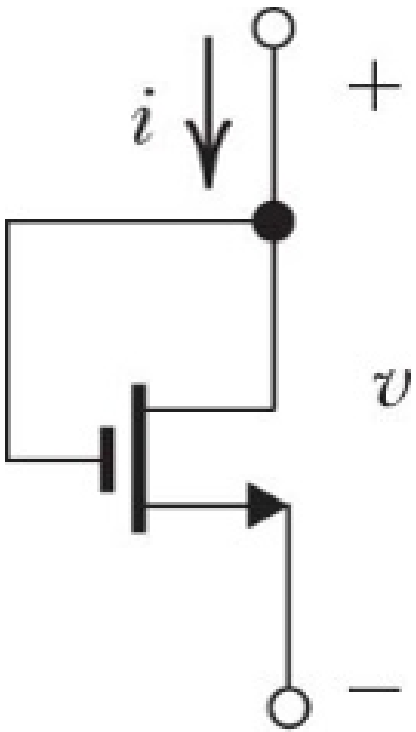
Large Signal Models

Small Signal Models

Switch Models

First MOSFET circuits

Diode Connected Transistor



In strong inversion:

$$I = \frac{1}{2} k_n (V - V_{tn})^2$$

Simple Current Mirror

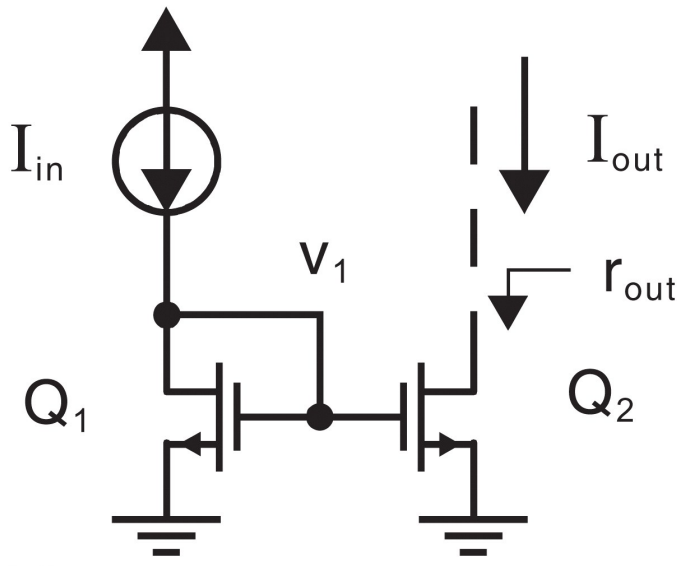


Figure 3.1
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When will $I_{out} = I_{in}$, $I_{out} \neq I_{in}$, $I_{out} \approx I_{in}$, $I_{out} \approx xI_{in}$?