LOW-DROPOUT REGULATOR DESIGN PROJECT

IN5180/IN9180 Assignment 2 Fall 2020

Milestone 1: 20. October 2020 (Preliminary delivery in devilry)

Final deadline: 10 November 2020 (delivery in devilry)

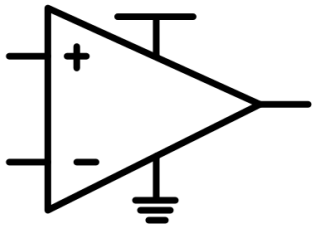
Project presentation: 18. November (for the class, room Java)

In wireless sensor systems circuits must be designed to accommodate and fully utilize the energy source which is available. In this case we will design a regulation circuit for a battery powered System-on-Chip circuit block. Due to voltage variations over the lifetime of the battery, local voltage regulation is required for stable power supply of the System-on-Chip integrated circuit and to use all the battery capacity. A typical voltage vs discharge curve for an alkaline 1.5 V battery is shown in the figure below where the voltage drops form 1.55 V to 1 V over the lifetime and the supply voltage for the circuit block must be stable within 10 mV. When the voltage is below 1 V the battery is empty. To maximize the battery life of the system several aspects with the LDO must be considered further explained in the text.

The design task is divided in to four parts. The first is designing the error amplifier (opamp) and include compensation to ensure stability. The second part is implementing a LDO architecture based on the error amplifier design and a pass-transistor. In this LDO implementation the error amplifier is used in a feedback configuration with one input connected to the reference voltage. With the other input connected to Vout and the output of the error amplifier driving the gate of the pass transistor the circuit regulates the Vout to Vref. Part 3 is layout and post-layout simulation of the LDO. If you have time task 4 is analysing how reducing Cload affect the LDO.

1 Opamp schematic and testbench

The first step is designing a two stage opamp error amplifier. Start with the opamp testbench (cell



opamp_tb) which is used to simulate the gain, frequency response and phase margin. Then design a two stage opamp (cell opamp) using the following suggested specifications:

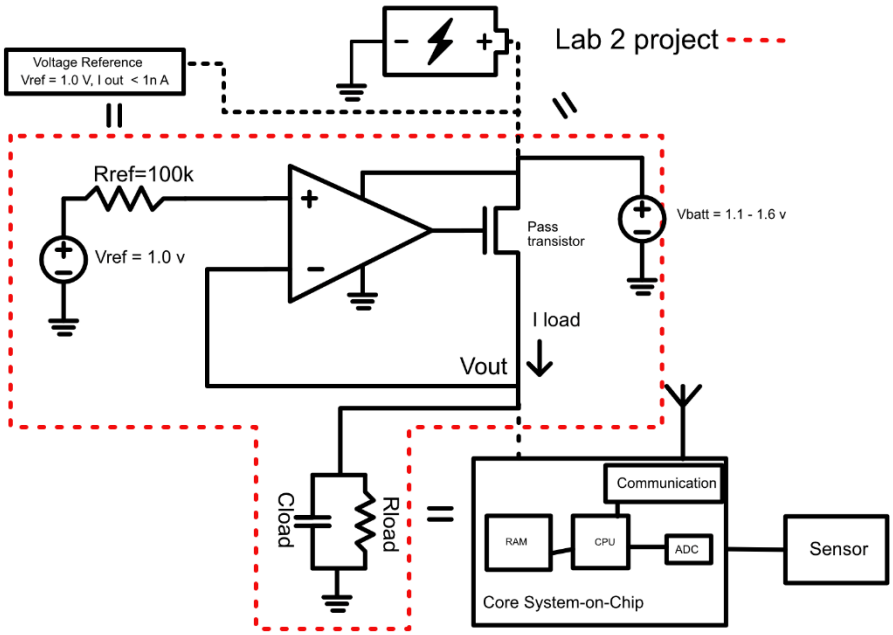
- VDD 1.2 V
- DC voltage gain > 1000
- Phase margin > 90 degrees

-Include the schematic and describe your design and compensation strategy.

-Report **gain**, **frequency response**, **phase margin**, **common-mode rejection ration (CMRR) / power supply rejection ratio (PSRR)**, **output swing**, **settling time** and **current consumption**.

-Discuss how these parameters are relevant for the given applications as an error amplifier in a Low Dropout Regulator.

2 LDO design



Design the LDO circuit with the operational amplifier as an error amplifier. Use ideal components for Cload, Rref and Rload as these model other circuits not available in this design phase. To have as high battery life as possible, minimize the dropout voltage (Vbatt-Vout), current consumption and settling time of the LDO. Stability and total circuit area are also important. In modern SoC for wireless IoT applications time gating of sub-circuits are widely used and transient loading of the LDO must be expected. This can be included in the testbench with ideal switches (analogLib-> switch) and a voltage source which has a transient signal response.

- Opamp based error amplifier
- One ideal current source Idc (< 30 uA)
- Minimum battery DC voltage 1.1 V
- Maximum battery voltage 1.6 V
- Regulated voltage 0.95 V < Vout < 1.05 V
- Rload = 5k and 500 Ohm
- Cload = 100 pF
- 1.0 V or 1.2 V reference voltage

-Report **minimum dropout voltage**, **power consumption, settling time** and **phase margin**. In the transient simulation plot Vout to ensure no oscillations will occur.

-How does the pass transistor in the feedback loop affect the circuit? What type/size of pass transistor should be used?

-Discuss your design process and report the results.

3 Layout and post layout extraction

Draw the layout of the LDO and complete Design Rule Check (DRC). When the design is DRC clean report setup a post-layout extraction and post-layout simulation and report the performance of the circuit including parasitic capacitance and resistances of the routing.

-Include the layout and post-layout simulation results in the report.

-How are the performance of the LDO affected by the parasitic components

-Discuss layout considerations and area usage.

(4) Extra: Component cost-down

The SoC customer want to reduce the number of external components and you are asked to design the LDO without external decoupling of VDDA. When the external decoupling capacitor is removed, Cload is only the internal decoupling capacitance of the core circuit and Cload is reduced to 500 fF

-Analyse the circuit as in part 2.

-Discuss what happens when Cload is reduced?

Project requirements

The main purpose of this project is to design and simulate a opamp based LOD, which meets the specifications outlined in section 1/2.

- Other than these specifications, the students have the freedom to choose the methods used to implement the system.
- The students can work in a group of two as the workload in this project is intended for two students. The group members must read this document completely and carefully assess the task. The work must be distributed almost equally among the members of the group and the same must be mentioned in the final report.
- A full schematic for the system and its sub-modules must be drawn. Separate symbol for all sub-modules must be made. The top-level representation should include these sub-modules in a well-organized hierarchical design.
- A full physical layout should be made
- Design Rule Checking (DRC) and Layout Versus Schematic (LVS) for the total system must be completed. These checks have to be free of errors. The reports should be enclosed in the final report.
- When the layout is ready for sub-modules and system, back annotation of all parasitic components (post layout extraction) into the schematic must be performed. The full schematic including back annotated parasitic elements (post layout simulations) must be simulated and the results compared with the simulation without parasitic elements.

Report requirements

- The report should be prepared using LATEX, MS Word or a similar word processor and must document all the different phases of the project. Plots of schematics, layout and simulated results for sub-modules and total system must be included in additions to LVS reports.
- The organization of the project and the distribution of responsibility within the group must also be included. In addition, the location of all design files should be listed. Please remember that the report must be considered a stand-alone document that should give the reader a complete view of what you have done. This is important to make sure that the entire picture is included in the final assessment and grading of the project.
- Please remember to include the references that you used to prepare the report.
- Note: DO NOT use “Print screen” to capture the waveforms. Cadence provides a way to capture nice waveforms. In the “Virtuoso Visualization & Analysis” window, select “Graph → Major and Minor Grids” and toggle to disable the grids. This captures a clear waveform. Next, select “File → Print”. In the Print window, select the name of the printer as “Print to File (PDF)”, select the output file path and then select “Options”. In the “Qt-subapplication” window, select “A4” as the Paper and “Landscape” as the orientation. Adjust the margins if you like. Click “OK” to exit window. Finally, select “Print” to print the waveform.