AMPLIFIER DESIGN USING GM/ID

IN5180/IN9180 Assignment 1 Fall 2021

Deadline: 22. September 2021 23:59 CEST (Delivery in devilry)

In this assignment you will design a single stage amplifier based on the gm/Id design methodology in TSMC 65nm technology.

- Resistively loaded common source (CS) amplifier
- Unity gain frequency ($\boldsymbol{UGF}$) > 4 GHz
- Capacitive Load ($\boldsymbol{C_L}$)= 120 fF at the output of the CS
- DC voltage gain = 3.5 V/V
- Overdrive voltage / Veff = 250 mV
- $L_{min} = 65\ nm$

1 Square law model vs simulation

Find the transistor width (W) in a single stage amplifier using the square law model and typical mosfet parameters given in the table. Use 45 nm as the closest approximation and Veff in moderate to strong inversion $\sim 200\ mV$

Table 1.5 MOSFET parameters representative of various CMOS technologies and used for rough hand calculations in this text.

	0.8 μm		0.35 μm		0.18 μm		45 nm	
Technology	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
μC_{ox} ($\mu A/V^2$)	92	30	190	55	270	70	280	70
V_{t0} (V)	0.80	–0.90	0.57	–0.71	0.45	–0.45	0.45	–0.45
$\lambda \cdot L$ (μm/V)	0.12	0.08	0.16	0.16	0.08	0.08	0.10	0.15
C_{ox} ($fF/\mu m^2$)	1.8	1.8	4.5	4.5	8.5	8.5	25	25
t_{ox} (nm)	18	18	8	8	5	5	1.2	1.2
n	1.5	1.5	1.8	1.7	1.6	1.7	1.85	1.85
θ (1/V)	0.06	0.135	1.5	1.0	1.7	1.0	2.3	2.0
m	1.0	1.0	1.8	1.8	1.6	2.4	3.0	3.0
$C_{ov}/W = L_{ov}C_{ox}$ (fF/μm)	0.20	0.20	0.20	0.20	0.35	0.35	0.50	0.50
$C_{db}/W \approx C_{sb}/W$ (fF/μm)	0.50	0.80	0.75	1.10	0.50	0.55	0.45	0.50

Hint:

1. Start with finding the required transconductance for the specified Unit Gain Frequency of the transistor with the given load capacitanceC_L (C_{gs}, C_{dg}<< C_L). $UGF = \frac{g_m}{2\pi C_L}$
2. Find R_L to give the correct DC voltage gain A_V $A_V = g_m R_L$
3. Find I_D
4. Using $L = 1.5 * L_{min}$ and using the square law model (without any non-idealities) find W $V_{EFF} = \frac{2I_D}{g_m}$

Task 1:

- Draw the schematic of your design and include the derived component values

Task 2:

- Create a testbench for the design as in Figure A

- Simulate AC using ADE L (Figure B) and plot the AC magnitude vs frequency in the report (Output -> To be plotted -> select in sch)
- Answer: What is the DC gain and bandwidth compared with the initial specifications? Discuss what is the benefit of hand calculations?

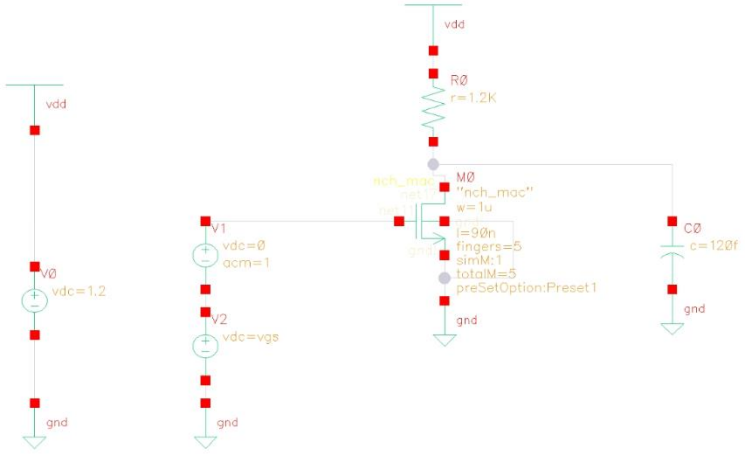


Figure A

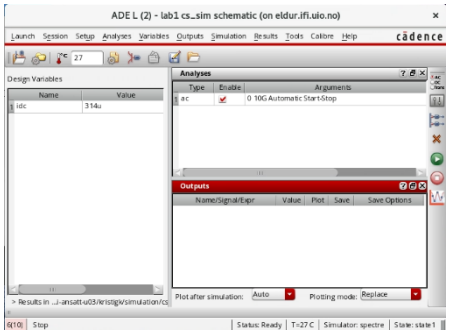


Figure B

2 gm/Id - Lookup table generation

To find an appropriate transistor operation point (V_{eff}) for the given specifications we simulate the DC characteristics of a transistor. (start with a new schematic cell view)

1. Start with an appropriate unit transistor (e.g. L = 90nm, W= 1 um)
2. In Cadence IC make a testbench like in Fig. 1
3. Setup a DC analysis in ADE L with "Save DC operating point" enabled
4. Add the following outputs (assuming M0 is the name of transistor see fig.2)

```
id pv("M0" "id" ?result "dcOpInfo")
gm pv("M0" "gm" ?result "dcOpInfo")
ft pv("M0" "ft" ?result "dcOpInfo")
2idovergm ((2 * id) / gm)
gmoverid (gm / id)
```

5. Sweep the voltage source from 50 mV to 700 mV in 10 mv steps using the parametric analysis tool (see fig. 3)
6. Plot **id , gmoverid** vs **2idovergm:** Right-click on the x-axis and choose "Y vs Y …", and then select **2idovergm** in the dialog.

The plot is the lookup table for choosing transistor width. Use Marker -> create marker -> vertical to find values

Task 3: Include the **id , gmoverid** vs **2idovergm** plot in the report and explain the plot.

Task 4: Plot **ft vs id** and explain why this is relevant for the amplifier design.

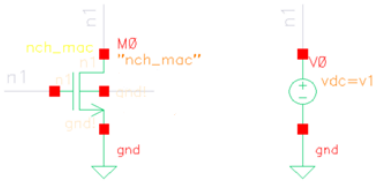


Figure 1: Lookup table testbench

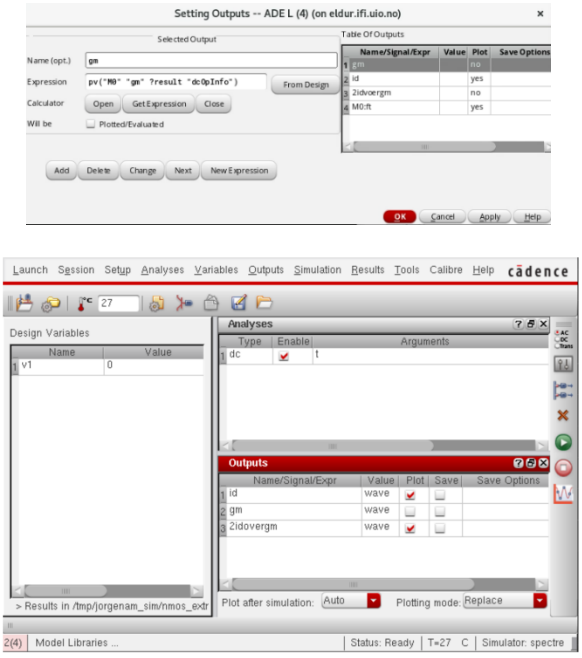


Figure 2: ADE L setup

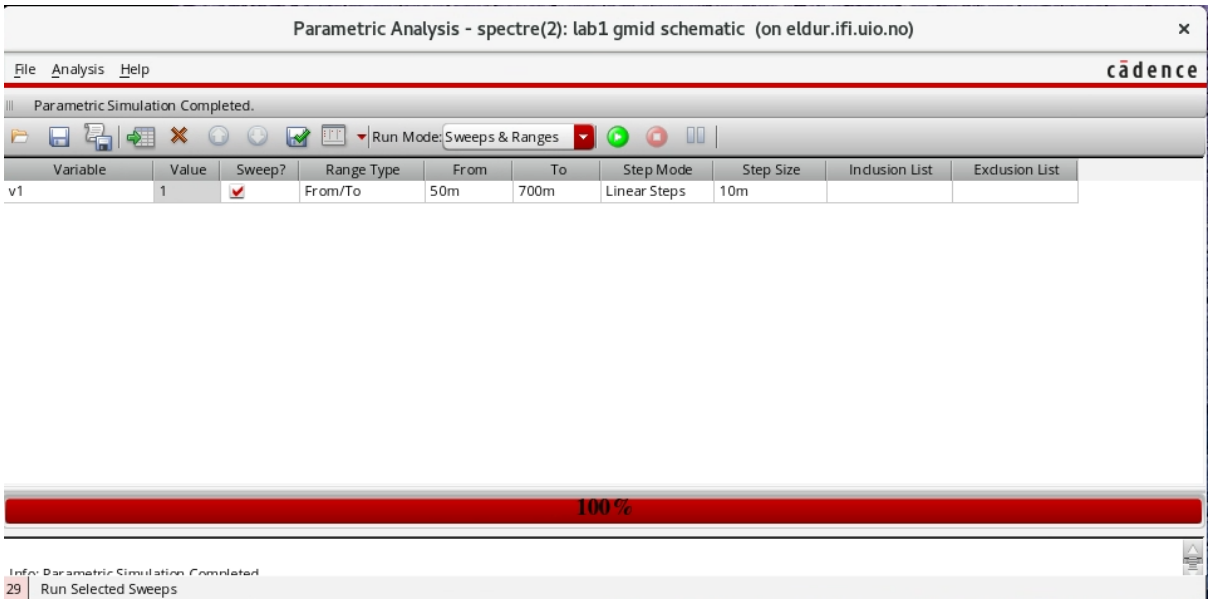


Figure 3: Parametric analysis setup (in ADE L → Tool → Parametric Analysis ...)

3 gm/Id - Amplifier design

In this par you will design the amplifier using the extracted gm/Id lookup table and simple hand calculations.

1. Choose an appropriate value for gm/Id using the information from the look up table
   Hint: for the transistor to not affect the BW of the amplifier choose **ft >> UGF**

Task 5: Discuss the trade-offs for choosing a higher or lower gm/Id.

2. Use the gm, Id and Rl from Task 1
3. Use the design chart generated in the previous section to lookup the unit transistor drain current for the gm/id that you chose (call this Iunit)
4. Calculate the width of the amplifier transistor as

$$W_{amp} = \frac{I_d}{I_{unit}} * W_{unit}$$

   where W_{unit} is the width you chose for the unit transistor.
5. Create a testbench like in fig 4. And run a DC simulation (with DC operation points) and an AC analysis.
   E0 is voltage controlled voltage source (VCVS) from analogLib to set the gate bias voltage
   V0 is a voltage source to generate the AC input
6. Extract the simulation results by using the results browser from the tools menu.

Task 6: Report the simulation results (Id, gm, DC gain and UFG). If the results differ from the hand calculations explain discrepancies. What can be done to improve the accuracy of the design.

4 gm/Id - Design variations (optional extra)

Task 7: Repeat the Amplifier design with 2 variations. Suggested variations below:

Different device lengths L = Lmin , 2*lmin

Different gm/id values initial +5 - 5

Different device types (LVT, HVT,2.5v I/O)

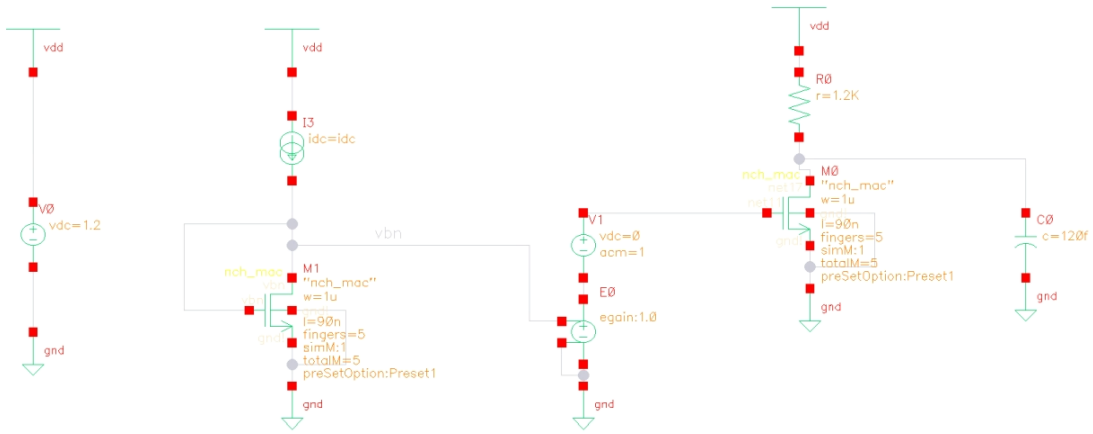


Figure 4