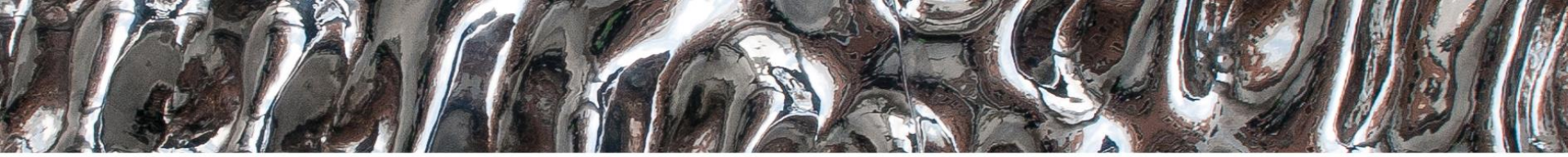


UiO : Department of Informatics
University of Oslo

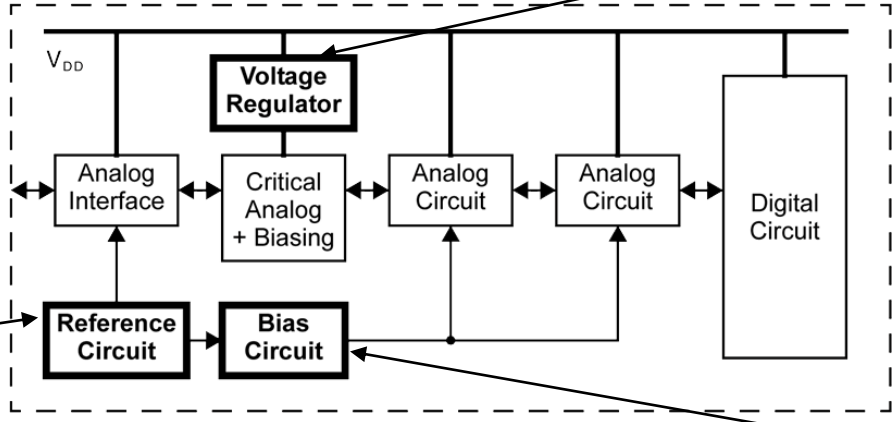
IN4180 - Analog Microelectronics Design

Biasing, References and Regulators - pt 1

Kristian G. Kjelgård

Biasing, references, regulators

- Providing suitable working conditions for analog circuit elements



Regulator

Improve DC voltage or keeping them stable

Reference

Generate constant and absolute voltage Independent of working conditions

Bias circuit

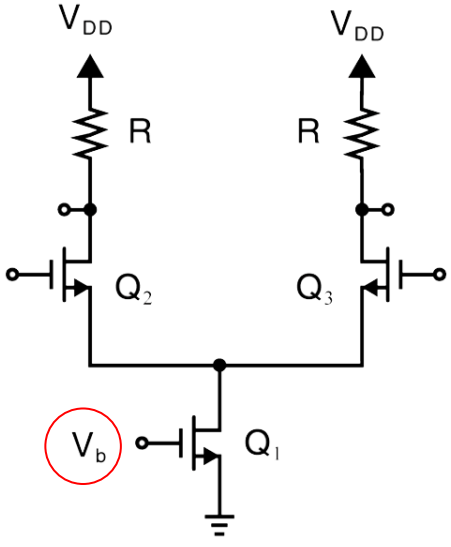
Setting DC voltages or currents

Biasing

Bias circuits

Assuming 10-20% device variations

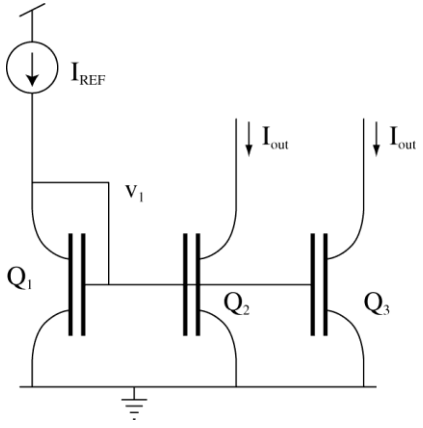
- What bias voltage Vb?
  - Constant drain current in match diff-pair?
  - Constant voltage drop over R?
  - Constant gain?



Bias circuits

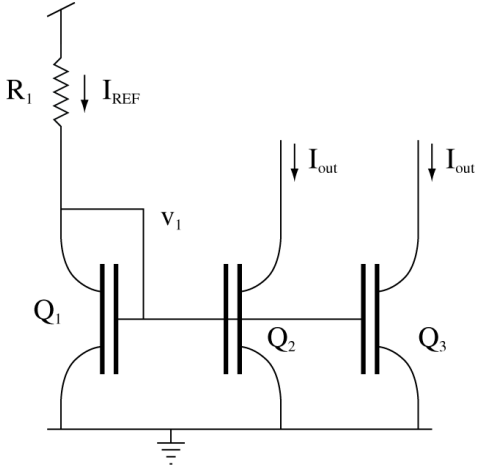
- Provide a bias voltage that tracks varying parameters and sets operation point accordingly
- Stable Gm – In may cases the most important
- Compensate supply voltage, temperature and process variations

Crude "Bias"



$$\Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_{m1}} \cdot \frac{(W/L)_2}{(W/L)_1}$$

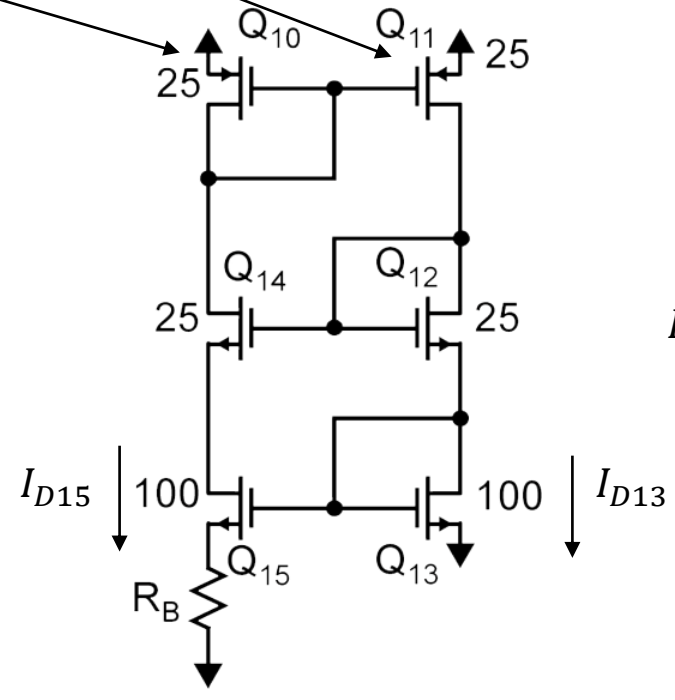
- Resistive current generator
  - Known load → good approximation
  - Sensitivite to Vdd and process parameters



Need some sort of self-biasing / feedback!

Constant transconductance bias circuit

$$\left(\frac{W}{L}\right)_{10} = \left(\frac{W}{L}\right)_{11}$$



$$I_{D15} = I_{D13}$$

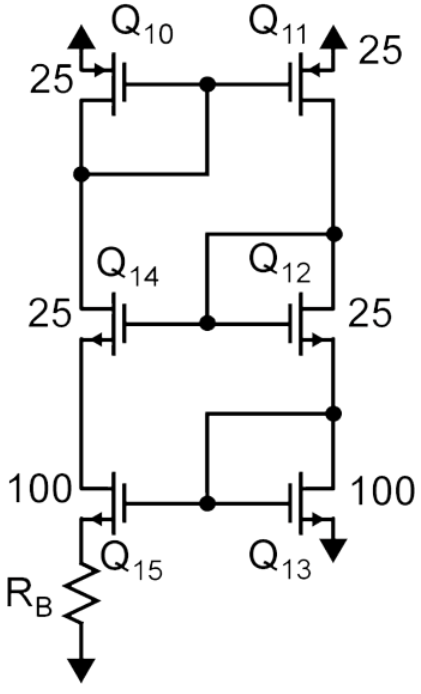
$$V_{EFF} = V_{GS} - V_{TN}$$

$$V_{GS13} = V_{GS15} + I_{D15}R_B$$

$$V_{TN13} = V_{TN15}$$

$$V_{eff13} = V_{eff15} + I_{D15}R_B$$

Constant transconductance bias circuit



$$V_{eff13} = V_{eff15} + I_{D15}R_B$$

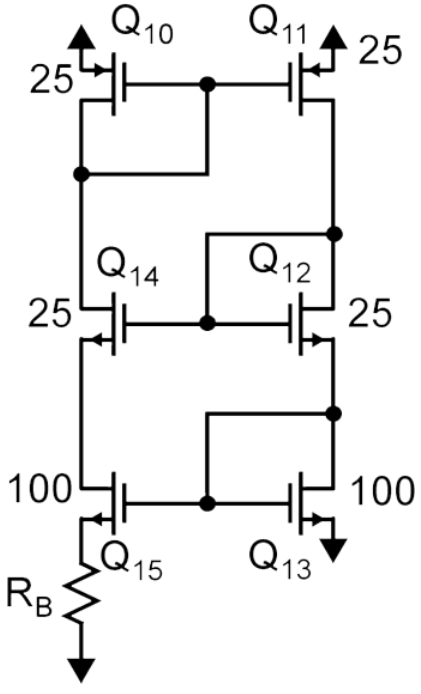
$$V_{eff} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(\frac{W}{L})}}$$

$$\sqrt{\frac{2I_{D13}}{\mu_n C_{ox}\,(\frac{W}{L})_{13}}} = \sqrt{\frac{2I_{D15}}{\mu_n C_{ox}\,(\frac{W}{L})_{15}}} + I_{D15}R_B$$

$$g_{m13} = \frac{2\left[1 - \sqrt{\frac{\left(\frac{W}{L}\right)_{13}}{\left(\frac{W}{L}\right)_{15}}}\right]}{R_B}$$

Gm independent of voltages and unCox

Constant transconductance bias circuit



For the special case:

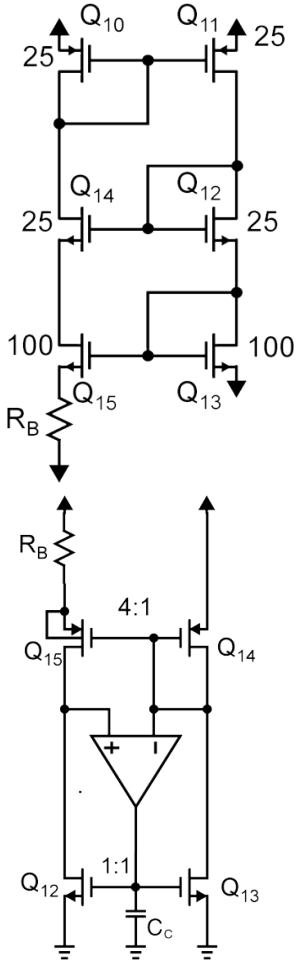
$$\left(\frac{W}{L}\right)_{15} = 4\left(\frac{W}{L}\right)_{13} \Rightarrow \qquad g_{m13} = \frac{1}{R_B}$$

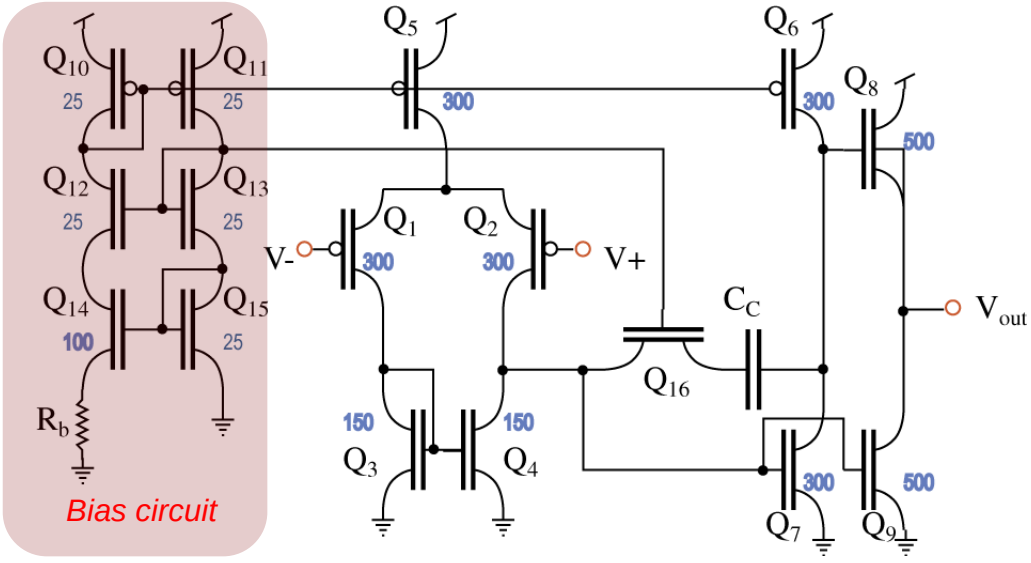
Constant transconductance

- PMOS devices

$$g_{mp} = \sqrt{\frac{\mu_p}{\mu_n}\frac{\left(\frac{W}{L}\right)I_D}{\left(\frac{W}{L}\right)I_{15}}} \approx g_{m13}$$

  - Unfortunately, mobility variations are significant
- Additional compensation for
  - Temp, body …
- Second stable state (I = 0)
  - Startup circuits required
- Runaway compensation at high temp. High power consumption

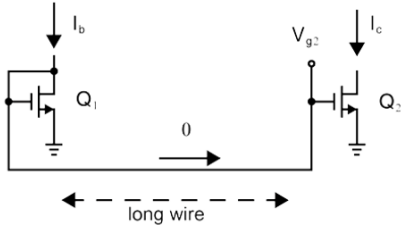



Q10
Q11
Q12
Q13
Q14
Q15
25
25
25
25
100
25
Rb
Bias circuit
Q5
300
Q6
300
Q8
500
Q1
Q2
V-
V+
300
300
CC
Vout
Q16
150
150
Q3
Q4
300
500
Q7
Q9

Bias distribution

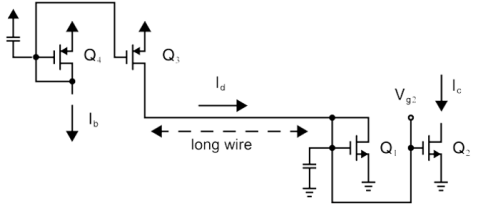
- Provide Vb -> transistors independent of temperature, process and supply parameters
- May be large and should be reused by several sub-circuits

Voltage mode distribution



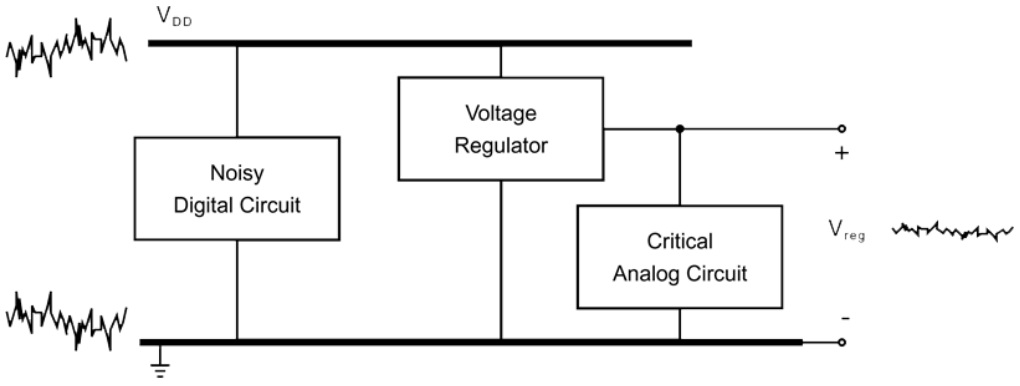
- Vtn variation sensitive
- GND potential sensitive
- Noise at high Z nodes
- Low current consumption

Current mode distribution



- Vtn independent
- GND indepentent
- More devices required
- Higher current consumption + Id

Voltage Regulator



- Handle VDD variations
- Provide power (in contrary to bias / references)
- Reduce supply voltage
  - Stabilize supply voltage for improved performance
- Filter noisy supply
  - Ground ref may still convey noise

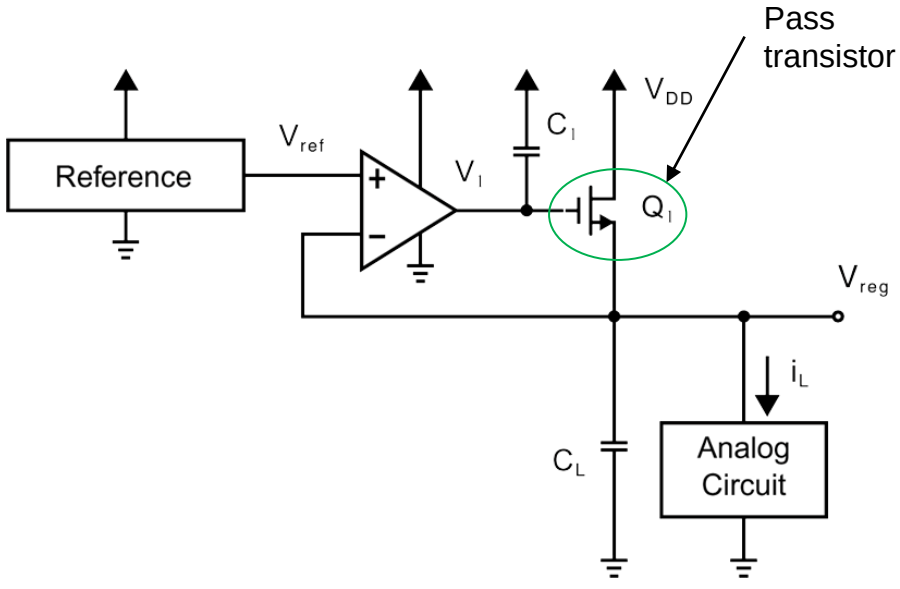
Classic linear regulator implementation

$$V_{ref} \approx V_{reg}$$

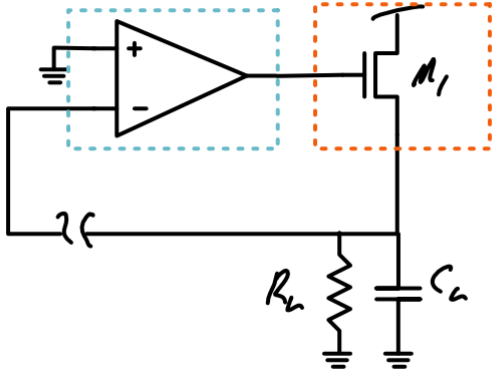
- Quiet and stable on-chip voltage
  - Input reference
  - Amp gain
- Specifications
  - Power-supply rejection ratio

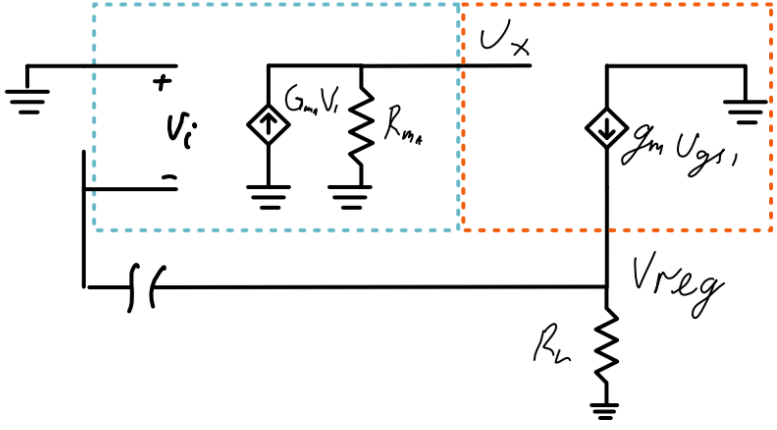
$$PSSR(\omega) = 10 \log_{10}\left(\frac{v_{DD}}{v_{reg}}\right)$$

  - Output impedance
  - Transient current load
  - Dropout voltage
    - Minimum voltage between supply and regulated voltage



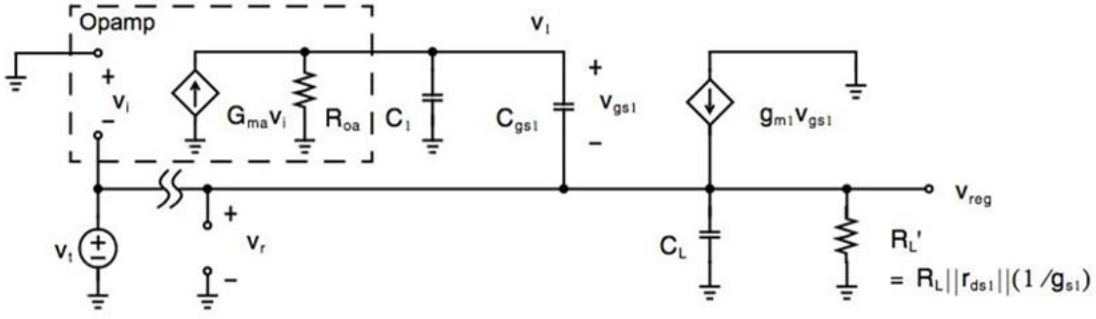
Regulator Feedback analysis – DC (ω=0)





$$L(\omega=0) = \frac{G_{mA} R_{mA} R_L}{\left(\frac{1}{g_{m1}} + R_L\right)}$$

Regulator Feedback analysis AC

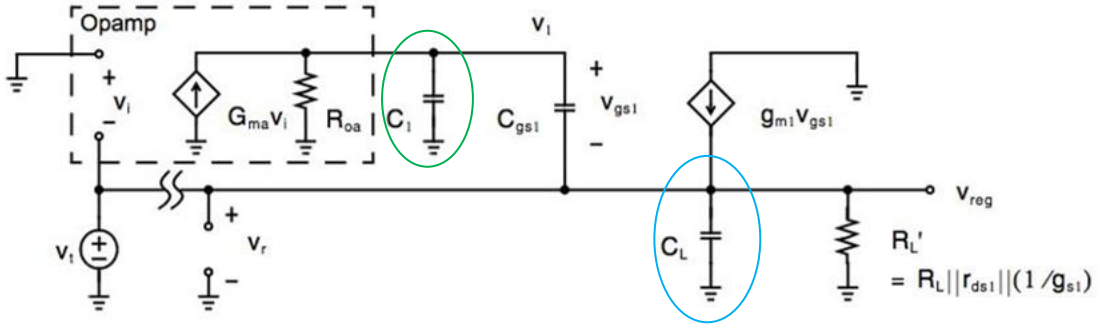


$$L(s) = \left(\frac{G_{mA} R_{OA} R_L}{R_L + 1/g_{m1}}\right) \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

Regulator Feedback analysis AC poles

$$-\omega_{p1} = -\omega_0 Q = -\frac{(1/R_{oa})(g_{m1} + 1/R_L')}{C_L/R_{oa} + C_1(g_{m1} + 1/R_{oa}) + C_{gs1}/R_L'}$$

$$-\omega_{p2} = -\frac{\omega_0}{Q} = -\frac{C_L/R_{oa} + C_1(g_{m1} + 1/R_{oa}) + C_{gs1}/R_L'}{C_{gs1}C_L + C_1(C_{gs1} + C_L)}$$



As a designer make C_1 large

Dominant pole

$$\omega_{p1} \approx \frac{1}{R_{oa} C_1}$$

$$\omega_{p2} \approx \frac{g_{m1}}{C_L}$$

Or C_L large ?

Low Drop-out regulator

- Dropout voltage
  - Maximum regulated voltage
- pMOS for minimal voltage drop
  - Notice reversed amp polarity
- Regulating loop

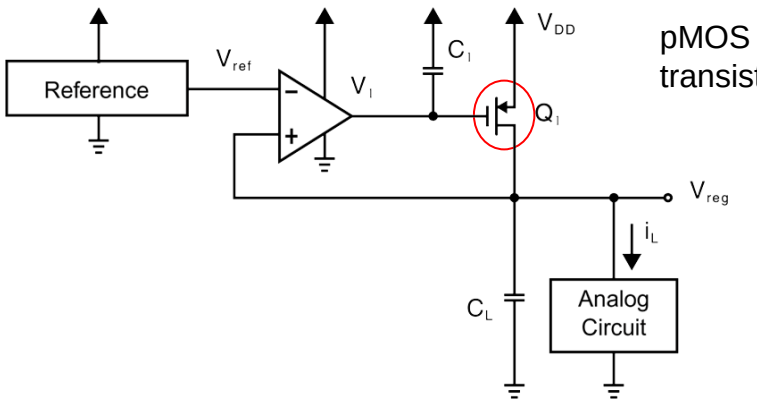
$$L(s) = \frac{G_{ma} R_{oa} g_{m1} R_L'}{\left(1 + \frac{s}{\omega_{pa}}\right)\left(1 + \frac{s}{\omega_{pL}}\right)}$$

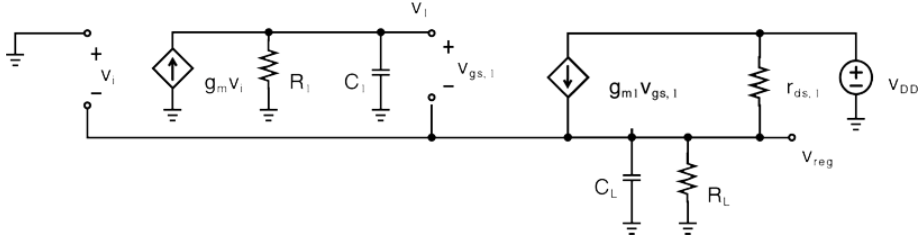
- Amp pole

$$\omega_{pa} = \frac{1}{R_{oa} C_1'}$$

  - Amp pole dominant → worse rejection
- Output pole

$$\omega_{pL} = \frac{1}{R_L' C_L}$$





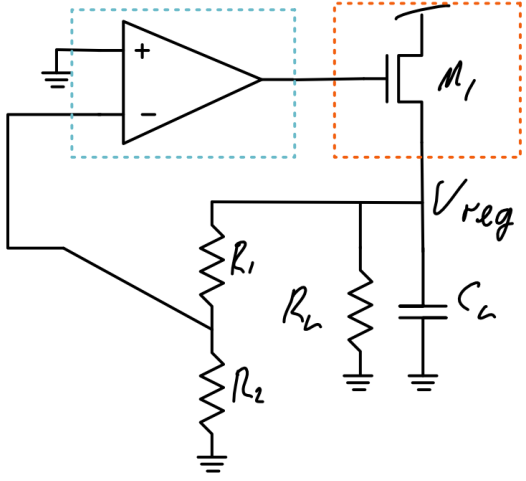
$$C_1' = C_1 + C_{gs1}$$

Regulator design considerations

- NMOS pass transistor -> better PSRR
- NMOS pass needs Vgs > Vth… Not suitable for Low Dropout

- PMOS pass transistor -> only limited by Veff (need some channel to get current trough
- High W needed with low VDD -Vreg)
- Higher gain in last stage (CS) and VDD is source voltage -> poorer PSRR

Regulator voltage control



$$V_{reg} = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$