

INTEGRATED PHOTODETECTOR DESIGN

IN5180 Assignment 2 Fall 2022

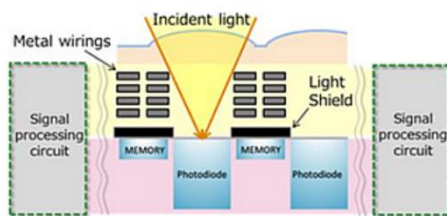
Milestone 1: 25. October (Preliminary delivery in devilry)

Final deadline: 18. November (delivery in devilry)

Project presentation: 25. November (for the class, room Shell OJD)

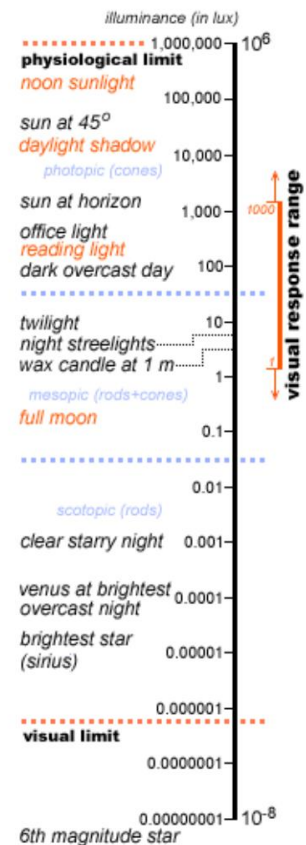
In this project you will design, simulate, and make layout of a photodetector circuit in 65 nm CMOS. (Read through the whole assignment before you start)

The design task is divided in to 4 main parts. The first is designing the amplifier (opamp) according to the given specifications and include compensation to ensure stability. The second part is to design the photo detector system on the block level. Part 3 is verification of the circuit given an ideal model of the photodiode.



The current provided from the current diode is dependent on the illuminance and the interesting threshold for this application is when it is perceived as dark (< 20 lux).

In the given process, the photocurrent out of the photo diode is a result of light intensity, wavelength, quantum efficiency, area of the photodiode, dark current etc . In this case the photo diode is designed to provide a I_{pd} of 40 μA at 20 lux of light illuminance. At 0 lux (only dark current) the photo diode can be modelled as a -0.5 μA current source.



1 Opamp schematic and testbench

The first step is designing a two stage opamp. Start making the opamp testbench (cell opamp_tb),

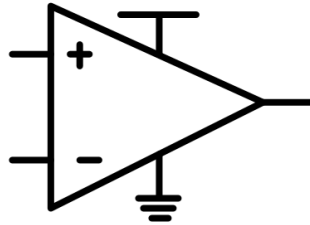


Figure 1

opamp cell (opamp) and symbol (hierarchal design). The testbench is used to simulate the gain, frequency response and phase margin. Then design a two stage opamp (inside cell opamp) using the following suggested specifications:

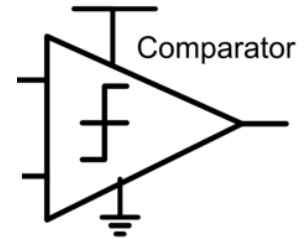
- VDD 1.2 V
- Phase margin > 65 degrees
- UGF > 10 MHz
- Have differential to single ended gain $A_{vd-c} = \frac{V_{out}}{V_+ - V_-} > 30 \text{ dB} \frac{\text{V}}{\text{V}}$ (higher is better)
- PSRR > 50 dB
- CMRR > 40 dB
- One ideal static current (idc) source between 0 and 30 uA can be used.
- VDD, and bias voltages can be set using ideal voltage sources (vdc)

TASK1:

- Include the schematic and describe your design, transistor sizing and compensation strategy.
- Report **open loop gain, frequency response, phase margin, common-mode rejection ration (CMRR) , power supply rejection ratio (PSRR)**
- Configure as voltage follower and report: **output swing, settling time, slew rate and current consumption.**
- Discuss how these parameters are relevant for the photo detector
- Draw layout DRC and LVS error free. Include image of layout and DRC/LVS reports as appendix

2 Comparator

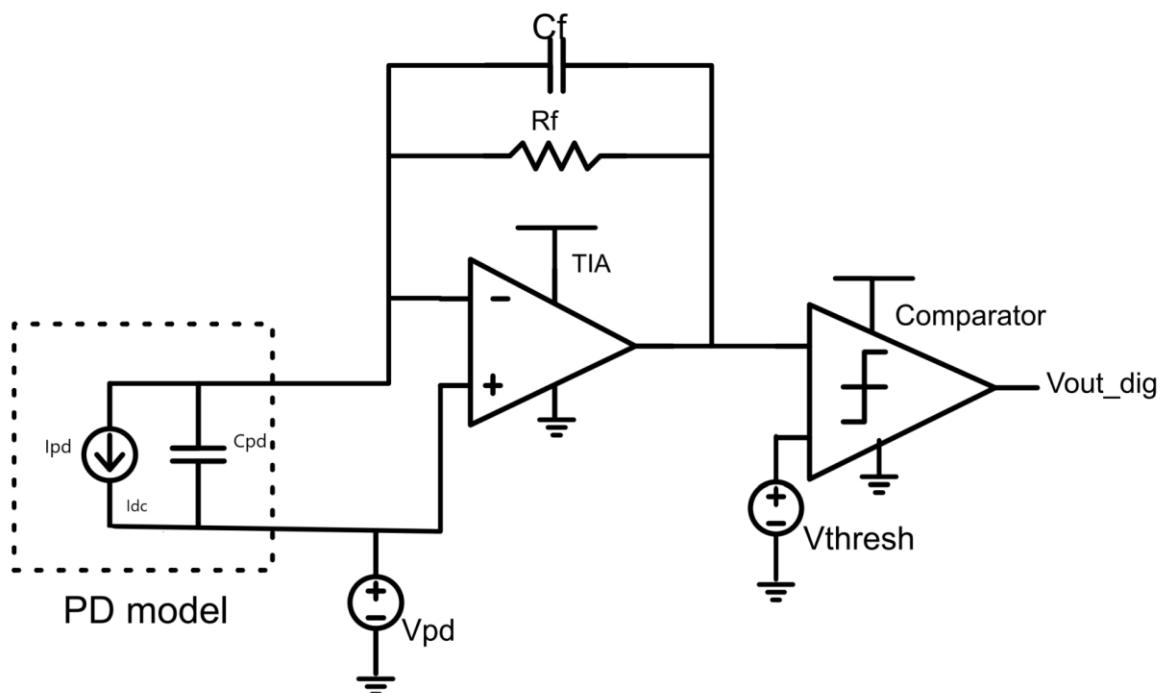
The photodetector output is a digital level signal which correspond to a given light intensity. Choose an appropriate comparator topology, either based on the opamp designed in the previous section, or some other and implement the design. (cell comparator and comparator_tb)



TASK 2:

- Include the schematic and describe your design
- Report **sensitivity, power consumption, response time.**
- Discuss your design process and report the results.
- Draw layout DRC and LVS error free. Include image of layout and DRC/LVS reports as appendix

3 Photo detector top level design and verification



TASK3:

- Build the top-level system testbench and verify that the photo detector gives a digital output which switches at 20 lux.
- R_f and C_f (if needed) must be implemented as tsmc65 library components
- Simulate the dc response by sweeping I_{pd} using an I_{dc} component from analogLib
- Simulate the transient response by using a I_{pulse} as I_{pdf} with 50 % duty cycle between 0 and 44 μA . Use a low frequency (ie 1 kHz)

Project requirements

The main purpose of this project is to design and simulate an opamp, comparator and photodetector circuits which meets the specifications outlined in section 1/2.

- Other than these specifications, the students have the freedom to choose the methods used to implement the system.
- The students should work in a group of two as the workload in this project is intended for two students. The group members must read this document completely and carefully assess the task. The work must be distributed almost equally among the members of the group and the same must be mentioned in the final report.
- A full schematic for the system and its sub-modules must be drawn. Separate symbol for all sub-modules must be made. The top-level representation should include these sub-modules in a well-organized hierarchical design.
- A full physical layout should be made
- Design Rule Checking (DRC) and Layout Versus Schematic (LVS) for the total system must be completed. These checks have to be free of essential errors. The reports should be enclosed in the final report.

Report requirements

- The report should be prepared using LATEX, MS Word or a similar word processor to create a PDF file and must document all the different phases of the project. Plots of schematics, layout and simulated results for sub-modules and total system must be included in additions to LVS reports.
- A critical discussion of the results and issues are expected and will count towards your grade.
- The organization of the project and the distribution of responsibility within the group must also be included. In addition, the location of all design files should be listed. Please remember that the report must be considered a stand-alone document that should give the reader a complete view of what you have done. This is important to make sure that the entire picture is included in the final assessment and grading of the project.
- Please remember to include the references that you used to prepare the report.
- Note: DO NOT use "Print screen" to capture the waveforms. Cadence provides a way to capture nice waveforms. In the "Virtuoso Visualization & Analysis" window, select "Graph → Major and Minor Grids" and toggle to disable the grids. This captures a clear waveform. Next, select "File → Print". In the Print window, select the name of the printer as "Print to File (PDF)", select the output file path and then select "Options". In the "Qt-subapplication" window, select "A4" as the Paper and "Landscape" as the orientation. Adjust the margins if you like. Click "OK" to exit window. Finally, select "Print" to print the waveform.

