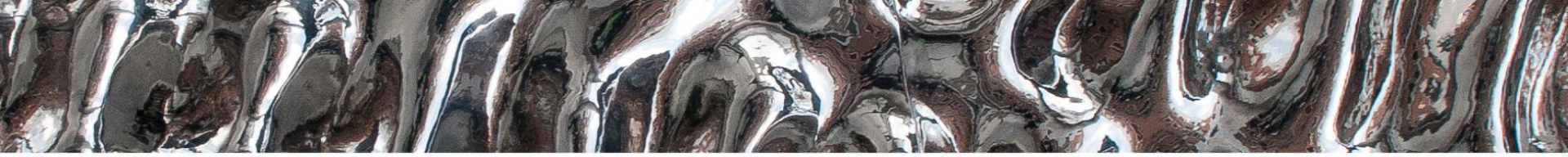


UiO : Department of Informatics
University of Oslo

## IN4180 - Analog Microelectronics Design

# Advanced MOSFET modelling, passives and EDA tools

Kristian G. Kjelgård

# Topics

Body effect

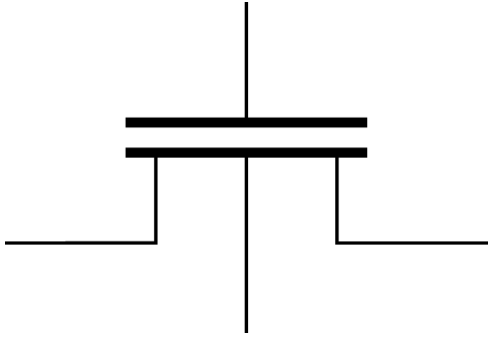
Short channel effects

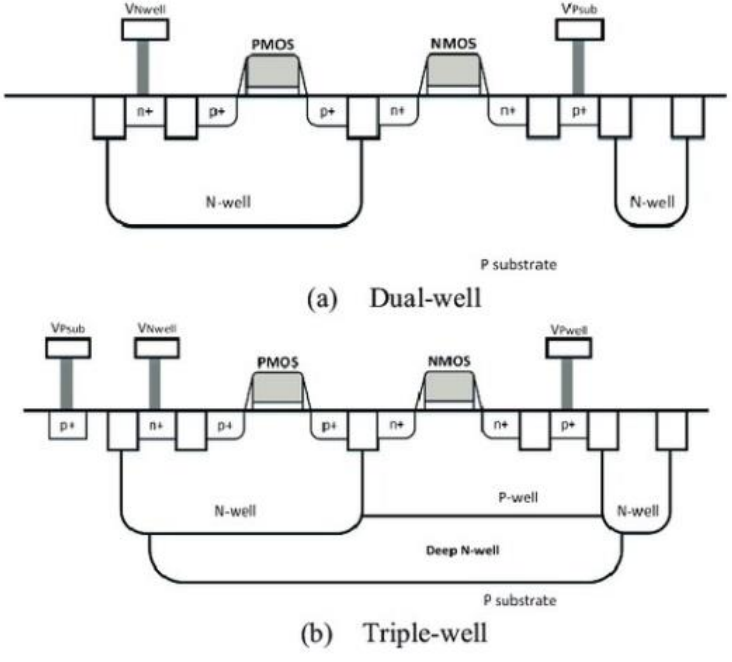
- Mobility Degradation
- Drain Induced Barrier Lowering
- Hot carriers

Passives

EDA tools

# The 4th terminal





# Body effect

- Back-gate effect, substrate effect

– Current change as $V_{SB}$ is different from zero

– Modeled as change in threshold voltage

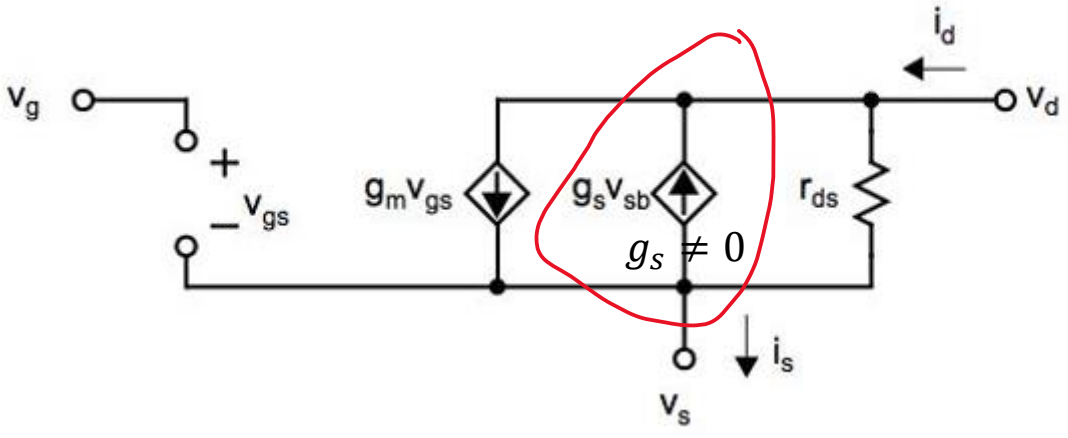
$$V_{tn} = V_{tn0} + \gamma\left(\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|}\right)$$

– $V_{tn0}$ – zero biased threshold voltage

$$\gamma = \sqrt{\frac{2qN_A K_S \varepsilon_0}{C_{ox}}}$$

$\phi_F$ - Fermi potential

# Body effect – small signal




$$g_s = \frac{\partial I_D}{\partial V_{SB}} = \frac{\partial I_D}{\partial V_{tn}} \frac{\partial V_{tn}}{\partial V_{SB}} = \frac{\gamma g_m}{2\sqrt{V_{SB} + |2\phi_F|}}$$

- If bulk connected to source

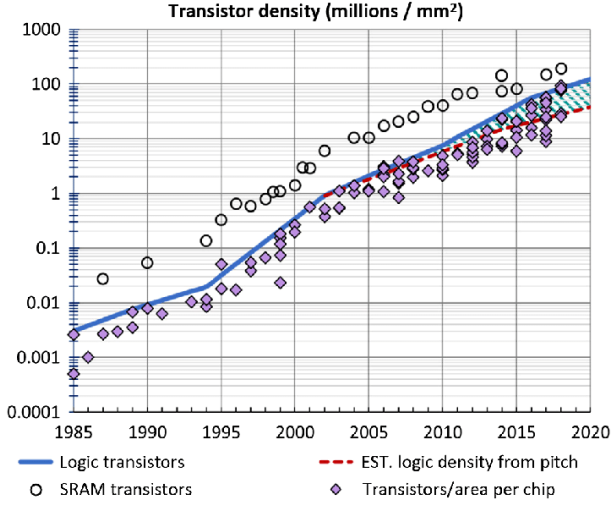
$$g_s = 0$$

- If Vsb ≠ 0

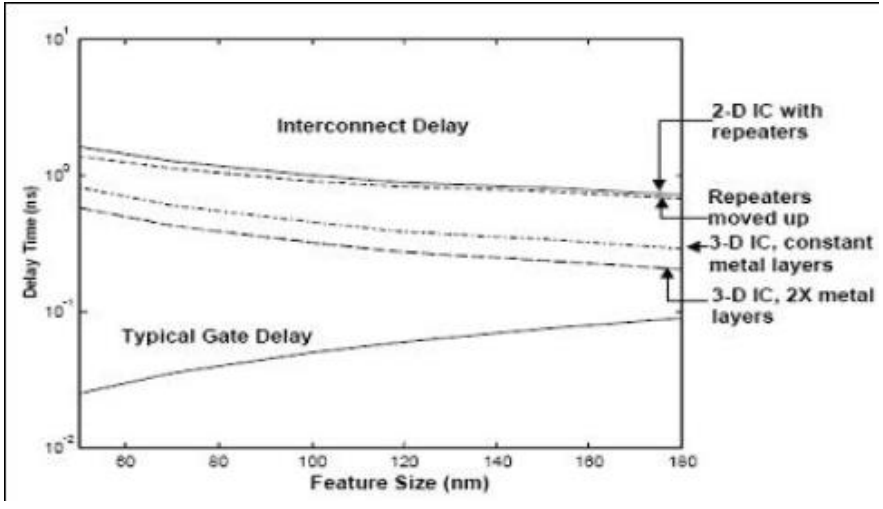
$$g_s \neq 0$$

# Why scaling?

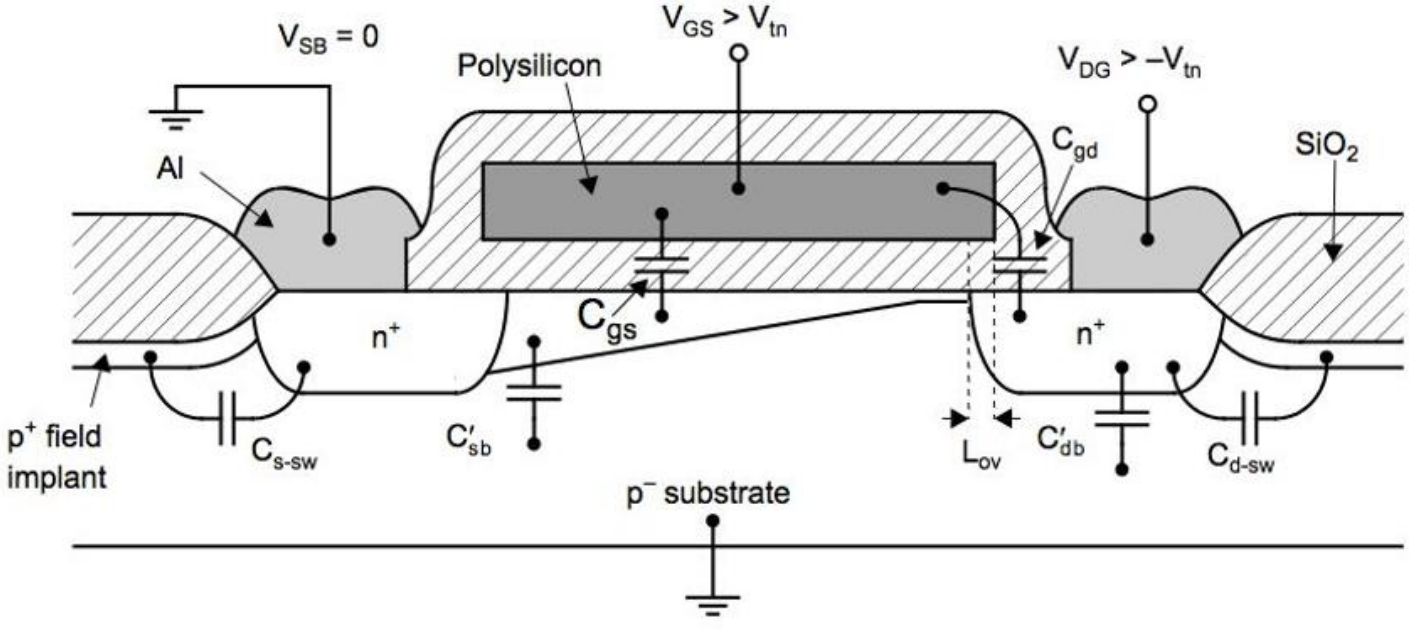
- Transistor density



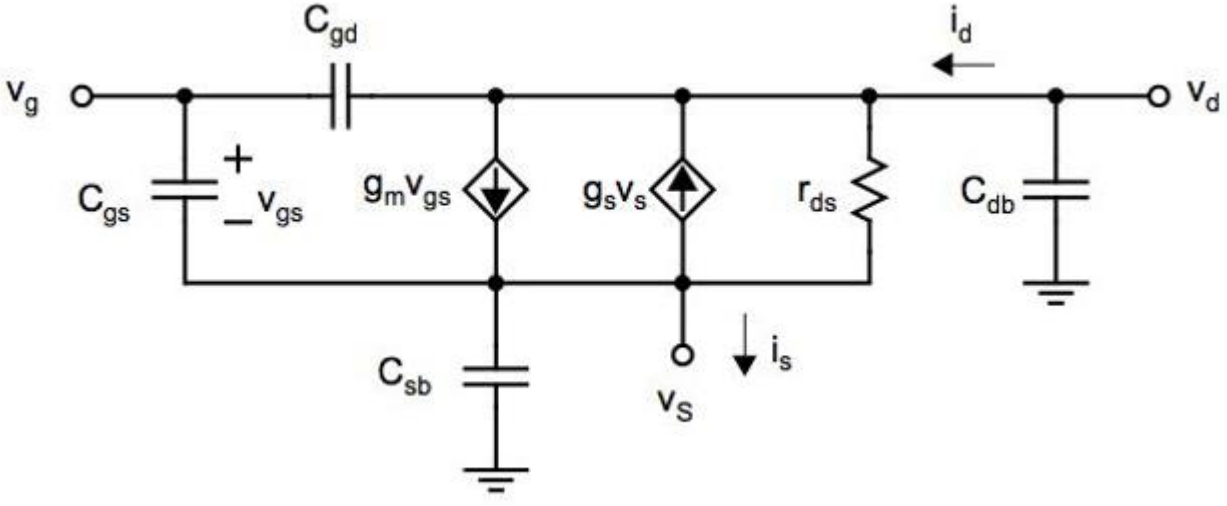

- Speed



# X-section with capacitance

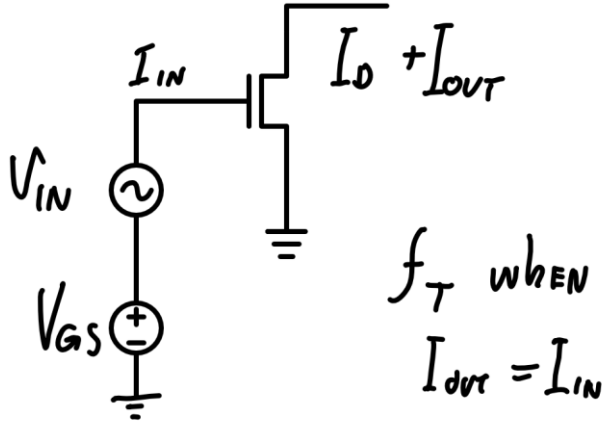


# Small signal model with capacitances

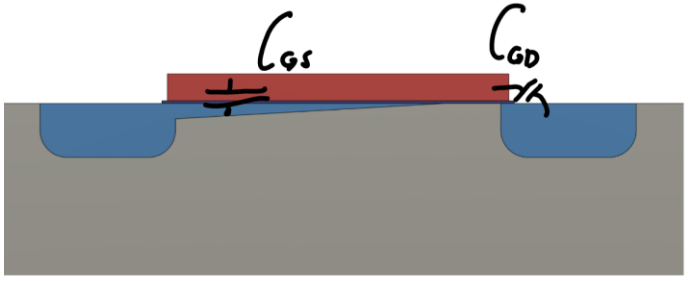


# $f_T$ transition frequency - transistor speed

- Higher $f_T$ -> faster digital systems and analog/RF (ie mmwave radio / radar systems)




Current gain unity gain frequency




$$f_T \approx \frac{g_m}{2\pi(C_{GS}+C_{GD})}$$

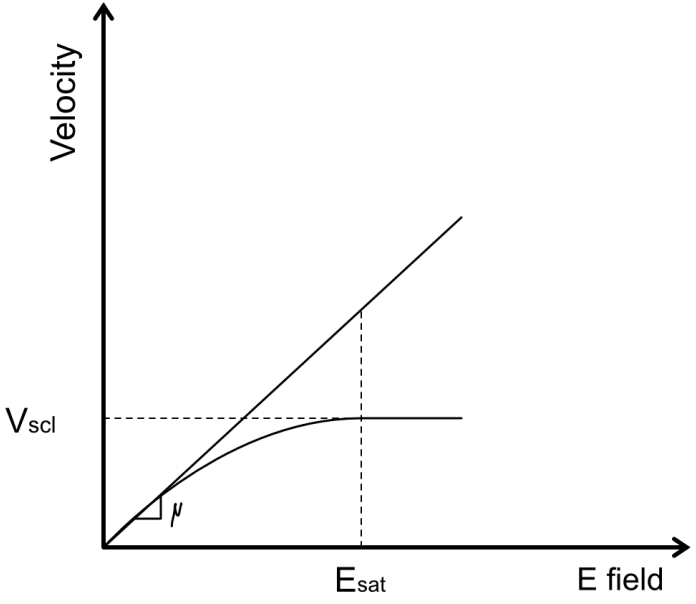
- Lower capacitance and higher Gm with shorter L
- ft proportional to $1/L^2$

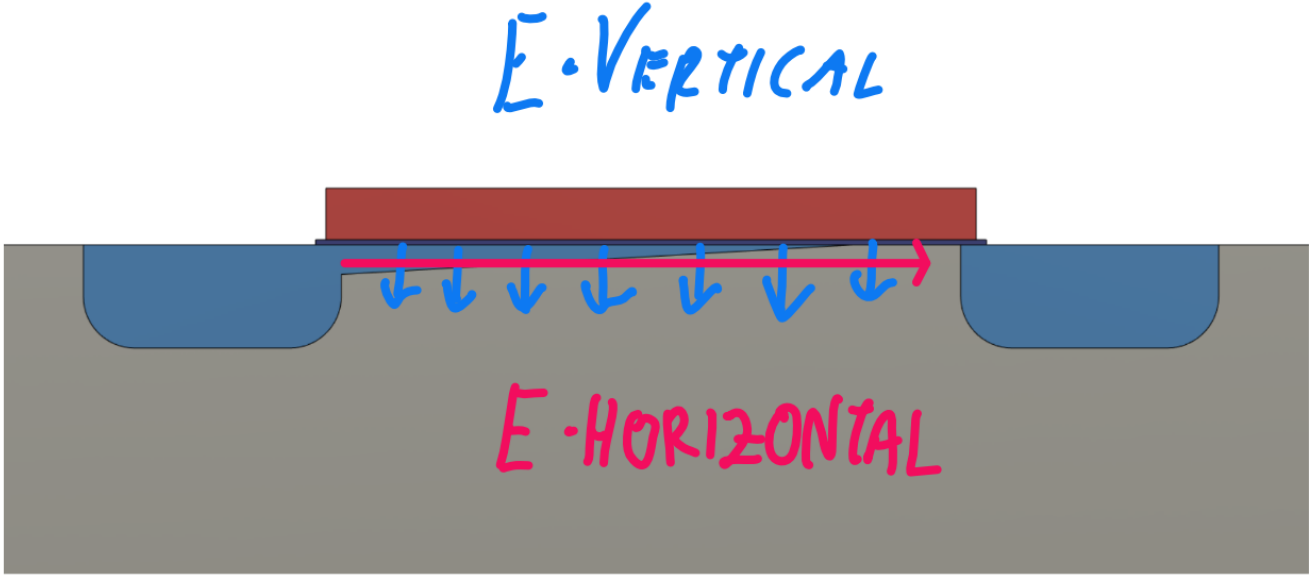
Assumes $\mu_n$ constant…

$$f_T \approx \frac{\mu_n C_{ox}\left(\frac{W}{L}\right)V_{EFF}}{2\pi C_{ox} W\left(\frac{2}{3}\right)L} = \frac{3\mu_n V_{EFF}}{4\pi L^2}$$

# Mobility degradation - $\mu_n$ with high E

- When transistors scale E gets high and mobility degraded
- Velocity of charge carrier limited to $10^7$ cm/s
- Affects speed and transconductance




E-VERTICAL
E-HORIZONTAL

$$\mu_{n,eff} = \frac{\mu_n}{\left(1 + (\theta V_{EFF})^m\right)^{1/m}}$$

$V_{EFF} \gg 1/\theta$

↓ MOBILITY DEGRADATION TERM

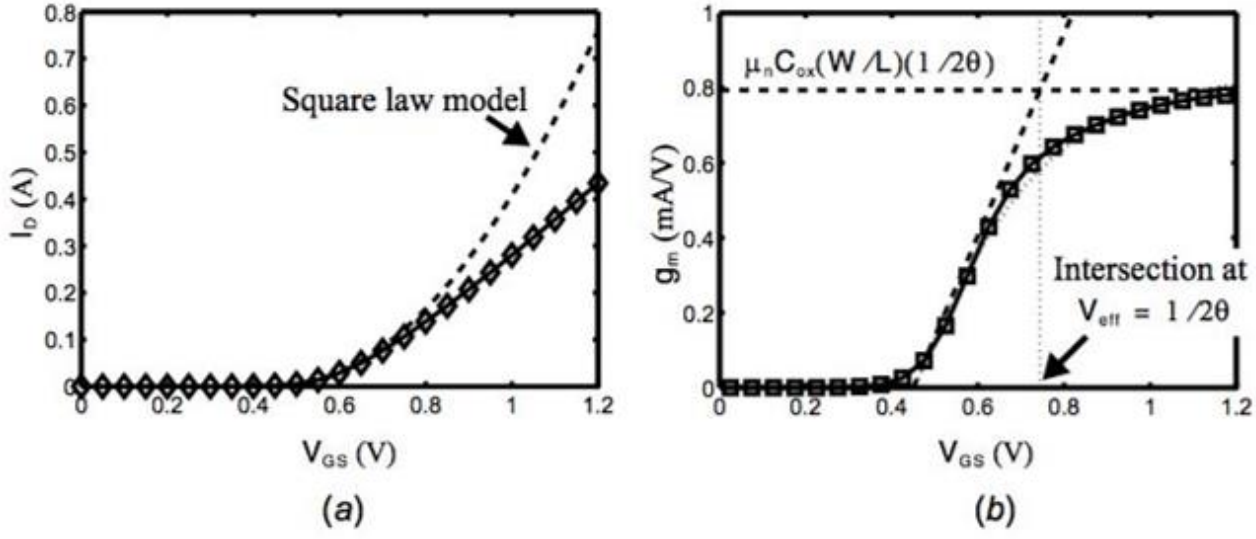
$\frac{1}{\theta V_{EFF}}$

↓ SQUARE LAW

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} \frac{V_{EFF}^{\cancel{2}}}{\theta \cancel{V_{EFF}}}$$

High $V_{eff}$ -> less control of channel
Square law -> linear

# Implications




- Small-signal transconductance limited
- Reduced available signal swing
- Reduction in intrinsic gain $A_i$

Scaling of CMOS -> large constraints on analog design

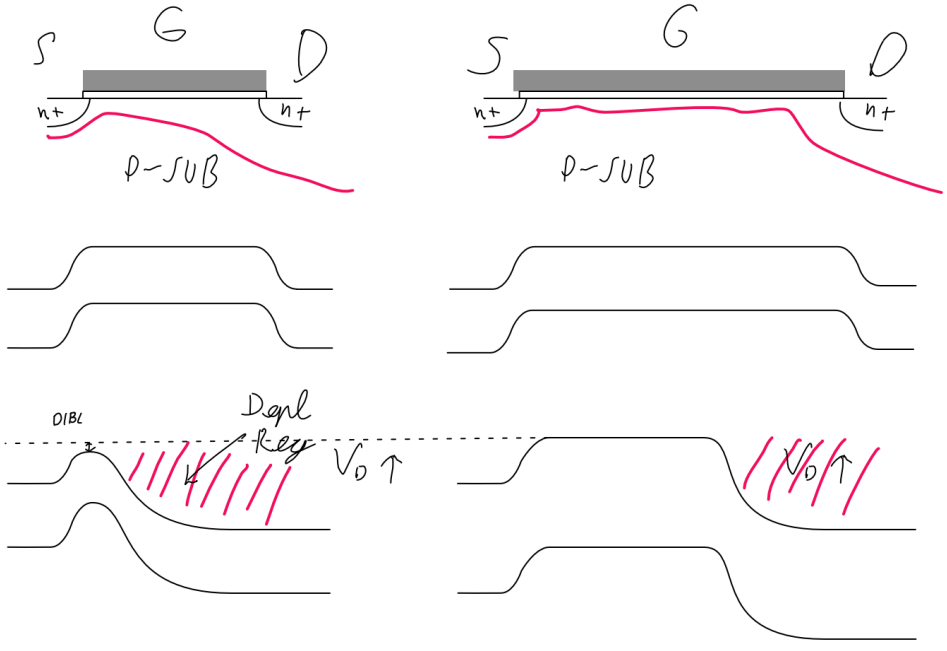
# Example

**1.25** Make a qualitative sketch of transistor intrinsic gain $A_i$ versus $V_{eff}$ for:

a. Constant device width W

In each case what is the relationship between $A_i$ and $V_{eff}$ in weak-inversion, active mode and under mobility degradation

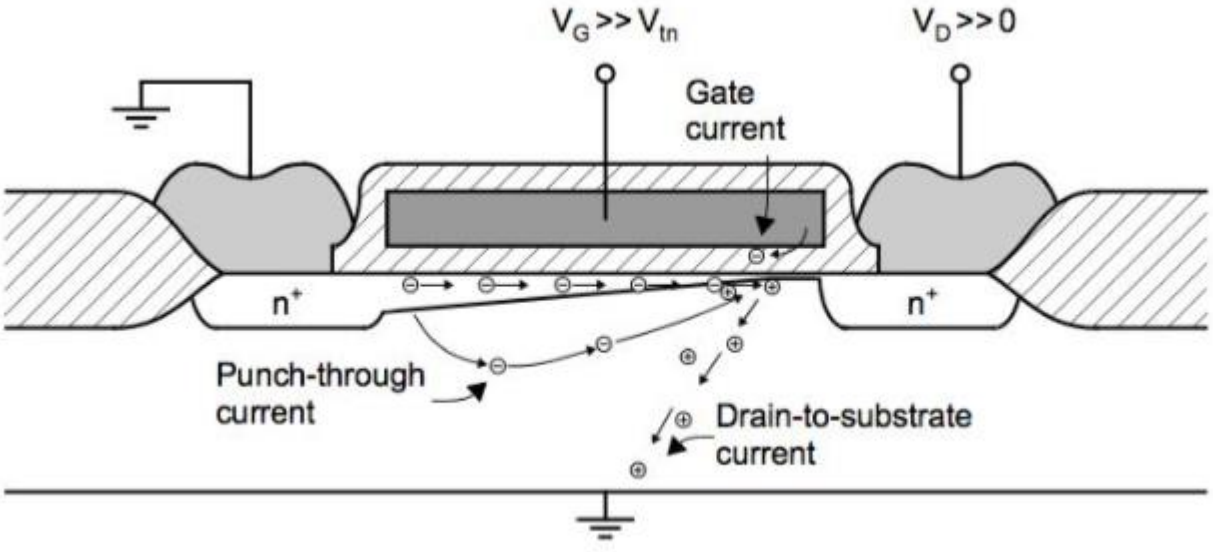
# Drain Induced Barrier Lowering (DIBL)



# Drain Induced Barrier Lowering (DIBL)

- $V_t$ dependence on $V_{ds}$
- Current dependent on $V_{ds}$ -> reduced $r_{ds}$

# Hot carriers




High velocity carriers

- E-H pairs -> Drain-to-substrate current
- Gate oxide tunnel
- Electrons in oxide trapped

# Leakage Current

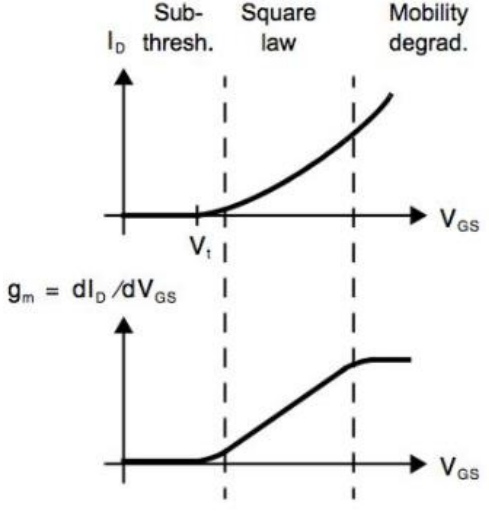
- Gate -> channel quantum-mechanical tunnel

- pn reverse junction leakage

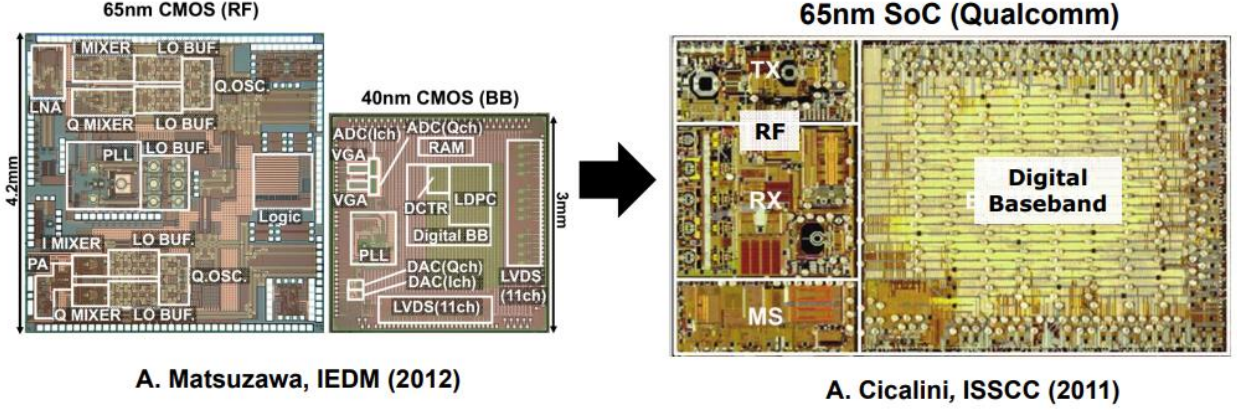
$$I_{in} = \frac{qAn_i x_d}{2\tau_0}$$

# Summary

- In modern CMOS technology a large variety of effects gives a non-ideal transistor behaviour
- Basic models used for "intuition" and design ideas
- Non-ideal characteristics very significant
- When to use simulator?



# SoC integration planar mosfet technology

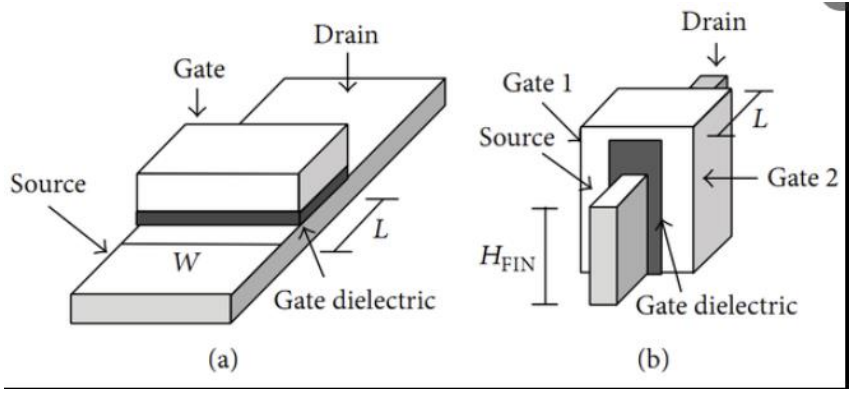


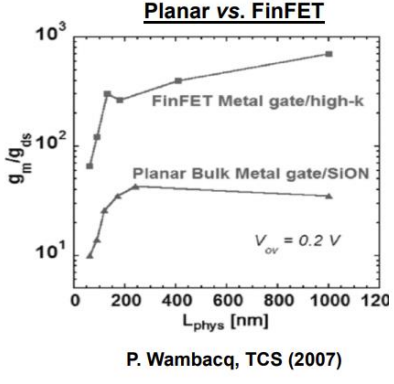

A. Matsuzawa, IEDM (2012)

A. Cicalini, ISSCC (2011)

# Sub 40 nm technologies -> finfet

- Next generation analog / Radio Frequency SoC in finfet technology?



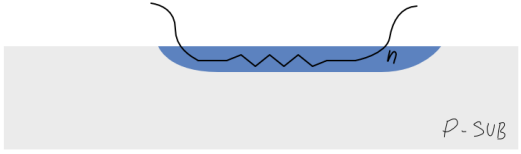




P. Wambacq, TCS (2007)

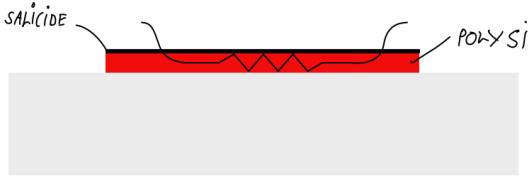
# CMOS passives

# Resistors in CMOS

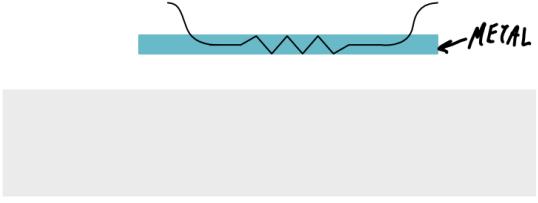
## Diffusion



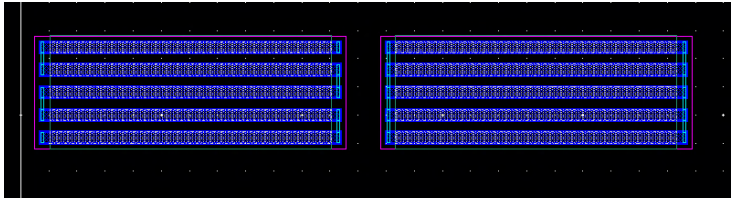

## Polysilicon




## Metal



# Meandering / layout of resistors



**Cadence Instances**

Diffusion:
rpod
rpodwo

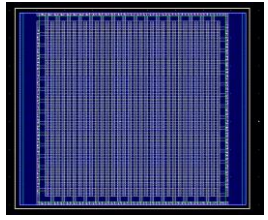
rnod
rnodwo

Poly:
rnpoly
rnpolywo

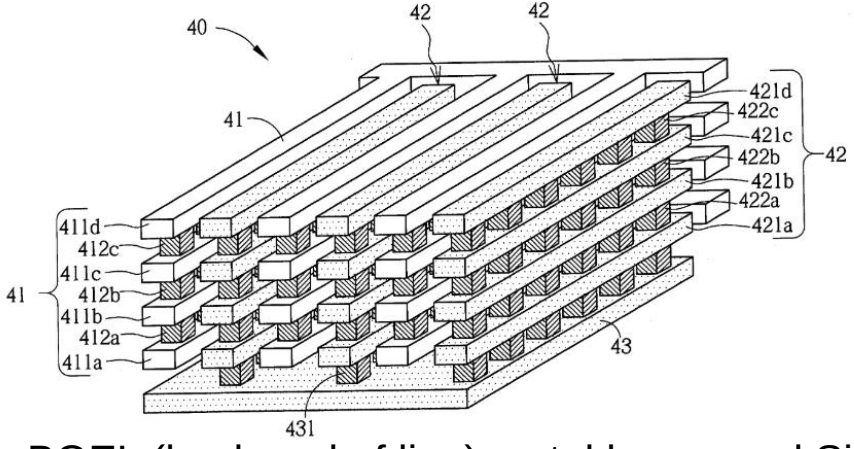
Metal:
rmN (n=metal layer)

Wo = without silicide
-> higher resistrance

**Cadence**
crtmom



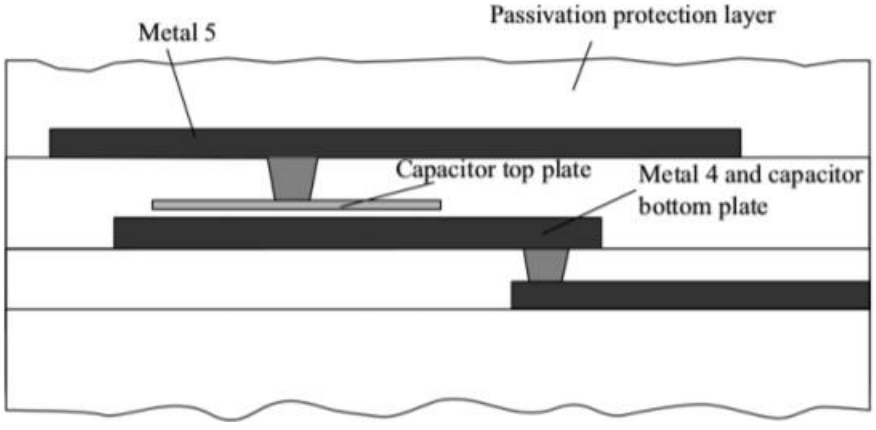
# MOMCAP

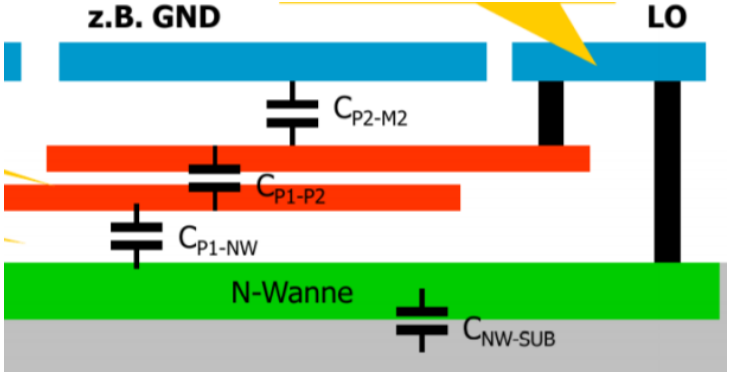



Use the standar BOEL (back end of line) metal layers and Silicon Oxide to form capacitor.

In modern process high density (fF/um3) can be achieved

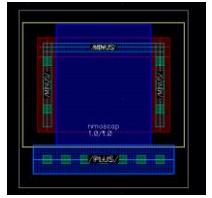
# MIMCAP




Extra high permittivity layer between Met_(n) and Met_(n-1)
Added cost to production with extra steps
Sensitive to antenna errors

**Cadence**
nmoscap



# MOSCAP

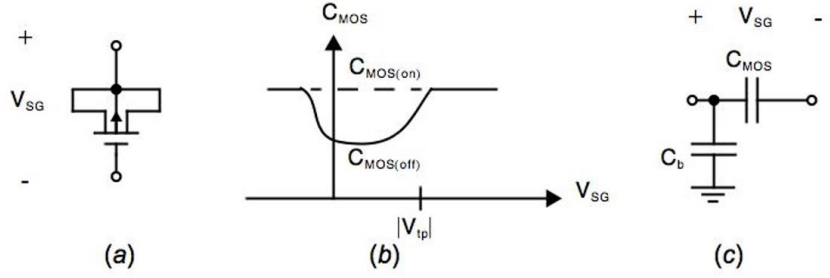
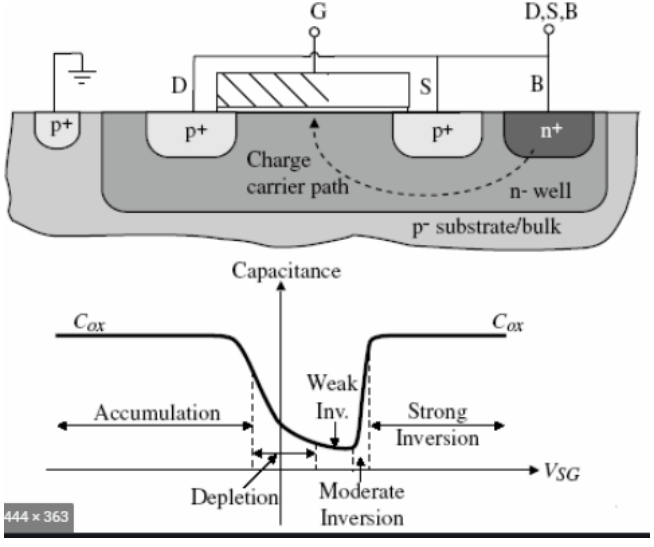


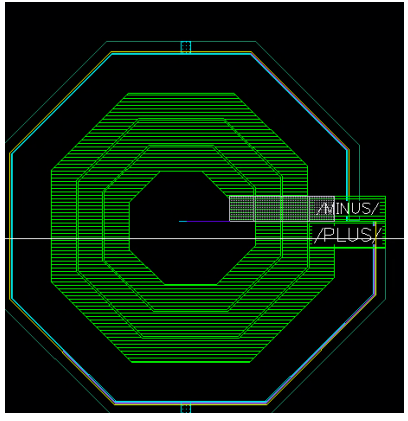

**Fig. 1.36** A PMOS capacitor: (*a*) schematic symbol; (*b*) nonlinear capacitance; (*c*) small-signal model.




- Use transistor gate oxide for capacitor
- Capacitance dependent on voltage
- High C- bulk

# Inductors

- Spiral inductors with and without centre tap
- On chip inductors mainly used for RF applications
- Doping under inductor coil is critical due to eddy currents loss. -> low Q



# Passives summary

Different implantations of passives.

Trade-off between area, quality, cost

IC process is stochastic  -> random variation in values

Layout of passives critical for high precision values.,

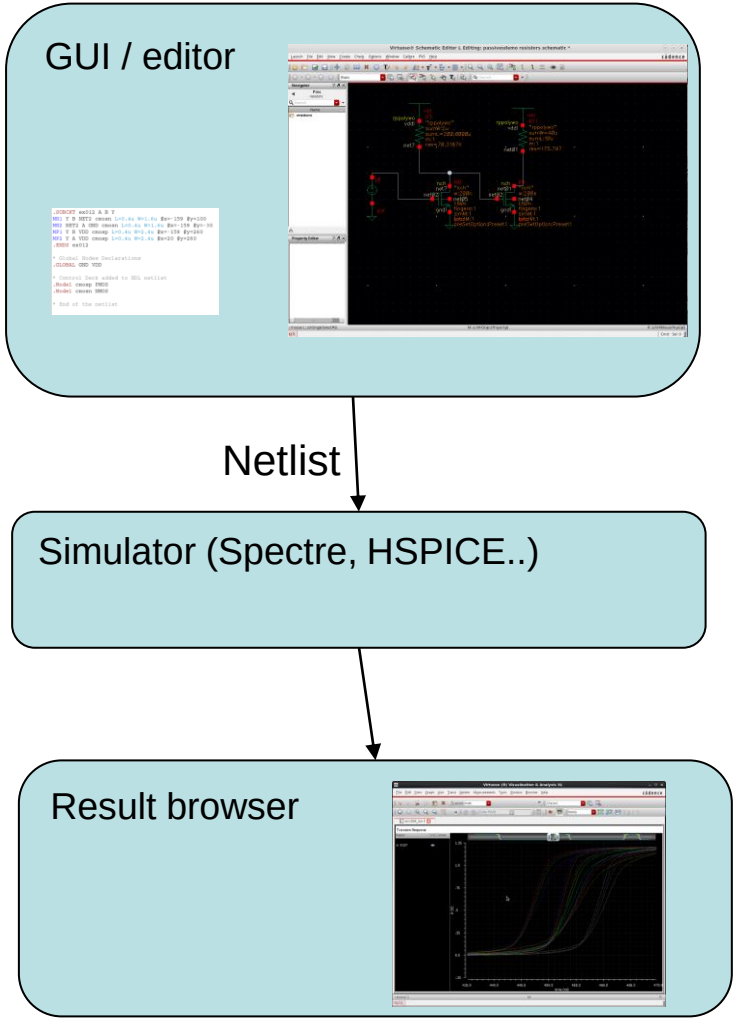
# EDA – Electronic Design Automation

- Modelling of the MOSFET is very complex and too much to consider for analytic expressions and hand calculations
- Numerical computational methods
- Berkeley Short-channel IGFET Model - BSIM widely used developed at Berkeley

```
* PTM High Performance 45nm Metal Gate / High-K / Strained-Si
* nominal Vdd = 1.0V

.model  nmos  nmos  level = 54

+version = 4.0            binunit = 1            paramchk= 1            mobmod  = 0
+capmod  = 2              igcmod  = 1            igbmod  = 1            geomod  = 1
+diomod  = 1              rdsmod  = 0            rbodymod= 1            rgatemod= 1
+permod  = 1              acnqsmod= 0            trnqsmod= 0

+tnom    = 27             toxe    = 1.25e-009    toxp    = 1e-009       toxm    = 1.25e-009
+dtox    = 2.5e-010       epsrox  = 3.9          wint    = 5e-009       lint    = 3.75e-009
+ll      = 0              wl      = 0            lln     = 1            wln     = 1
+lw      = 0              ww      = 0            lwn     = 1            wwn     = 1
+lwl     = 0              wwl     = 0            xpart   = 0            toxref  = 1.25e-009
+xl        = -20e-9

+vth0    = 0.46893        k1      = 0.4          k2      = 0            k3      = 0
+k3b     = 0              w0      = 2.5e-006     dvt0    = 1            dvt1    = 2
+dvt2    = 0              dvt0w   = 0            dvt1w   = 0            dvt2w   = 0
+dsub    = 0.1            minv    = 0.05         voffl   = 0            dvtp0   = 1e-010
+dvtp1   = 0.1            lpe0    = 0            lpeb    = 0            xj      = 1.4e-008
+ngate   = 1e+023         ndep    = 3.24e+018    nsd     = 2e+020       phin    = 0
+cdsc    = 0              cdscb   = 0            cdscd   = 0            cit     = 0
+voff    = -0.13          nfactor = 2.22         eta0    = 0.0055       etab    = 0
+vfb     = -0.55          u0      = 0.054        ua      = 6e-010       ub      = 1.2e-018
+uc      = 0              vsat    = 170000       a0      = 1            ags     = 0
+a1      = 0              a2      = 1            b0      = 0            b1      = 0
+keta    = 0.04           dwg     = 0            dwb     = 0            pclm    = 0.02
+pdiblc1 = 0.001          pdiblc2 = 0.001        pdiblcb = -0.005       drout   = 0.5
+pvag    = 1e-020         delta   = 0.01         pscbe1  = 8.14e+008    pscbe2  = 1e-007
+fprout  = 0.2            pdits   = 0.08         pditsd  = 0.23         pditsl  = 2300000
+rsh     = 5              rdsw    = 155          rsw     = 80           rdw     = 80
+rdswmin = 0              rdwmin  = 0            rswmin  = 0            prwg    = 0
+prwb    = 0              wr      = 1            alpha0  = 0.074        alpha1  = 0.005
+beta0   = 30             agidl   = 0.0002       bgidl   = 2.1e+009     cgidl   = 0.0002
+egidl   = 0.8            aigbacc = 0.012        bigbacc = 0.0028       cigbacc = 0.002
+nigbacc = 1              aigbinv = 0.014        bigbinv = 0.004        cigbinv = 0.004
+eigbinv = 1.1            nigbinv = 3            aigc    = 0.02         bigc    = 0.0025
+cigc    = 0.002          aigsd   = 0.02         bigsd   = 0.0025       cigsd   = 0.002
+nigc    = 1              poxedge = 1            pigcd   = 1            ntox    = 1
+xrcrg1  = 12             xrcrg2  = 5

+cgso    = 1.1e-010       cgdo    = 1.1e-010     cgbo    = 2.56e-011    cgdl    = 2.653e-010
+cgsl    = 2.653e-010     ckappas = 0.03         ckappad = 0.03         acde    = 1
+moin    = 15             noff    = 0.9          voffcv  = 0.02

+kt1     = -0.11          kt1l    = 0            kt2     = 0.022        ute     = -1.5
+ua1     = 4.31e-009      ub1     = 7.61e-018    uc1     = -5.6e-011    prt     = 0
+at      = 33000

+fnoimod = 1              tnoimod = 0

+jss     = 0.0001         jsws    = 1e-011       jswgs   = 1e-010       njs     = 1
+ijthsfwd= 0.01           ijthsrev= 0.001        bvs     = 10           xjbvs   = 1
+jsd     = 0.0001         jswd    = 1e-011       jswgd   = 1e-010       njd     = 1
+ijthdfwd= 0.01           ijthdrev= 0.001        bvd     = 10           xjbvd   = 1
+pbs     = 1              cjs     = 0.0005       mjs     = 0.5          pbsws   = 1
+cjsws   = 5e-010         mjsws   = 0.33         pbswgs  = 1            cjswgs  = 3e-010
+mjswgs  = 0.33           pbd     = 1            cjd     = 0.0005       mjd     = 0.5
+pbswd   = 1              cjswd   = 5e-010       mjswd   = 0.33         pbswgd  = 1
+cjswgd  = 5e-010         mjswgd  = 0.33         tpb     = 0.005        tcj     = 0.001
+tpbsw   = 0.005          tcjsw   = 0.001        tpbswg  = 0.005        tcjswg  = 0.001
+xtis    = 3              xtid    = 3

+dmcg    = 0              dmci    = 0            dmdg    = 0            dmcgt   = 0
+dwj     = 0              xgw     = 0            xgl     = 0

+rshg    = 0.4            gbmin   = 1e-010       rbpb    = 5            rbpd    = 15
+rbps    = 15             rbdb    = 15           rbsb    = 15           ngcon   = 1
```

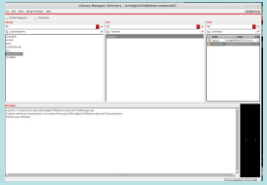
# Circuit simulation

- Spectre – Cadence
- HSPICE – synopsis
- UltraSIM



# IN5180 – Tool flow schematic simulation

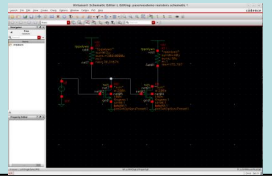
Virtuoso Schematic L / XL



Hierarchy and library organization

Library -> cell -> cellview

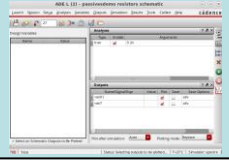
Virtuoso Schematic L / XL



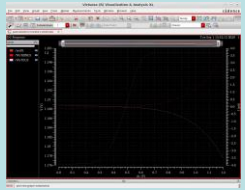
Schematic/symbol cellview

ADE GXL can make adexl cellview for organizing simulations (not needed for ADE L)

Virtuoso Analog Design Environment (ADE L)

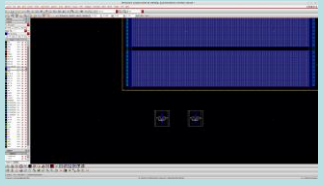


Virtuoso Visualization and analysis XL



# IN5180 – Tool flow layout and DRC

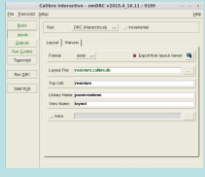
Virtuoso Layout L / XL



Layout cellview

Draw layout / generate from schematic

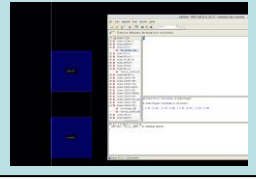
Mentor Calibre nmDRC



Check layout for errors (spacing, widths area etc..)

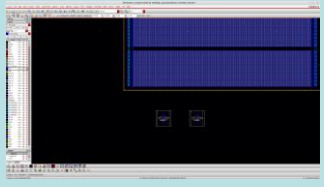
Locate errors in layout and fix

Mentor Calibre RVE

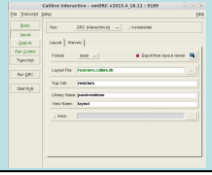


# IN5180 – post layout extraction flow

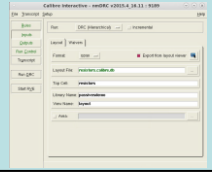
Virtuoso Layout L / XL



Mentor Calibre nmLVS



Mentor Calibre PEX



Virtuoso ADE
Post layout simulation
Calibre cellview