

INTEGRATE AND FIRE NEURON

IN5180 Assignment 2 Fall 2023

Milestone 1: 19. October (Preliminary delivery in devilry)

Final deadline: 15. November (delivery in devilry)

In class project presentation: 23. November (5-10 min)

In this project you will design, simulate, and make layout of a simple integrate and fire neuron model in 65 nm CMOS. (Read through the whole assignment before you start)

In neuromorphic electronics, inspiration from the brain is used to create computational networks. As with the neural networks in the brain, neuromorphic circuits are parallel in nature and has gained a growing interest in applications as image recognition, data classification and machine learning. To implement neural networks, modern analog CMOS with high density of transistors and low power is well suited. The key function a neuron model mimicking neural stimulus is the asynchronous integrate and fire function. In a simplistic model, the neuron fires a spike when the integral of the synaptic input reaches a threshold potential. A schematic of a Leaky Integrate and Fire Neuron with two synapse is shown in **Figure 1 (a)**, the simplified model without leakage in **Figure 1 b)**, and a schematic of a Leaky integrate and fire neuron in **Figure 1 c)** The leakage can be added to improve neuron model, which need a certain spike cluster intensity to fire.

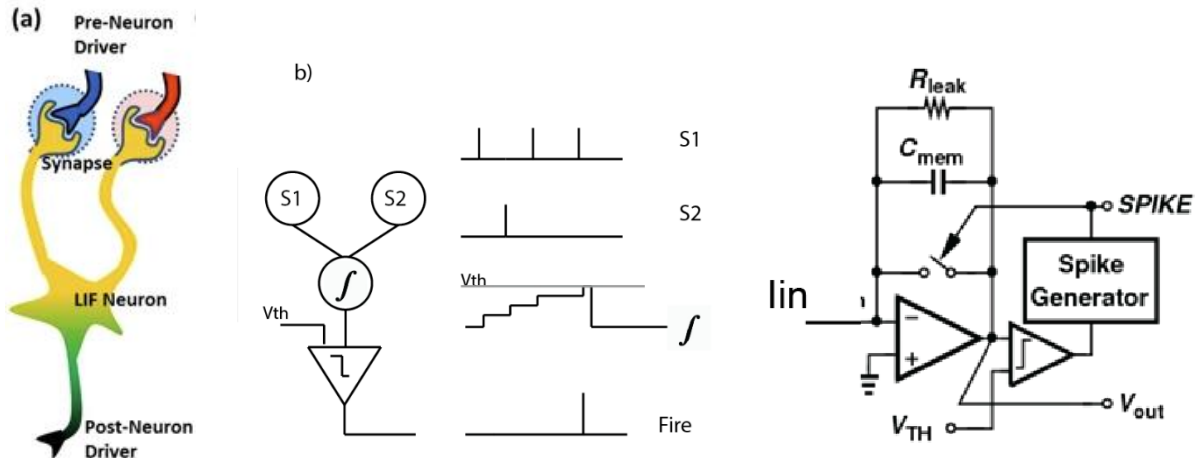


Figure 1 (figures from Sahoo ISCAS2017, Dutta et al, Scientific Reports 7 2017)

The design task is to implement this simple neural model with an opamp integrator and comparator.

The design task is divided in to 4 main parts. The first is designing the amplifier (opamp) according to the given specifications and include compensation to ensure stability. The second part is to design the comparator. Part 3 is verification of the neural model.

1 Opamp schematic and testbench

The first step is designing a two stage opamp. Start with the opamp testbench (cell opamp_tb) which

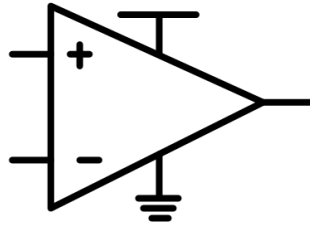


Figure 2

is used to simulate the gain, frequency response and phase margin. Then design a two stage opamp (cell opamp) using the following suggested specifications:

- VDD 1.2 V
- Phase margin > 65 degrees
- UGF > 10 MHz
- Have differential to single ended gain $A_{vd-c} = \frac{V_{out}}{V_+ - V_-} > 45 \text{ dB}$
- Common centroid layout of input transistors
- One ideal 30 uA current source can be used in the design.
- Testbenches can have ideal voltage/current sources

TASK1:

- Include the schematic and describe your design, transistor sizing, compensation strategy and testbench/simulation setup.
- Report **open loop gain, frequency response, phase margin, common-mode rejection ration (CMRR) , power supply rejection ratio (PSRR)**
- Configure as voltage follower and report: **output swing, settling time, slew rate and current consumption.**
- Discuss how these parameters are relevant for the neural model
- Draw layout DRC and LVS error free. Include image of layout and DRC/LVS reports as appendix.

2 Comparator design

To fire the spike a comparator is needed. Choose an appropriate comparator topology, either based on the opamp designed in the previous section, or some other and implement the design. (cell comparator and comparator_tb)

TASK 2:

- Include the schematic and describe your design
- Report **sensitivity, power consumption, response time.**
- Discuss your design process and report the results.

- Draw layout DRC and LVS error free. Include image of layout and DRC/LVS reports as appendix

3 Neuron model verification



Figure 3

The neural input excitation is shown in **Figure 3**, where the two current ipulse current sources model the input spikes, the C0 models the neural membrane, and the resistor R0 is the leakage.

TASK3:

- Build the complete testbench and verify the integrate and fire using only the comparator. The neuron should fire at a membrane potential of 80 mV.
- Implement the SPIKE circuitry that creates a voltage spike (0 to VDD) with a pulse width of 500 ns and reset membrane potential

Project requirements

The main purpose of this project is to design and simulate a neural integrate and fire model, which meets the specifications outlined in section 1/2.

- Other than these specifications, the students have the freedom to choose the methods used to implement the system.

- The students should work in a group of two as the workload in this project is intended for two students. The group members must read this document completely and carefully assess the task. The work must be distributed almost equally among the members of the group and the same must be mentioned in the final report.
- A full schematic for the system and its sub-modules must be drawn. Separate symbol for all sub-modules must be made. The top-level representation should include these sub-modules in a well-organized hierarchical design.
- A full physical layout should be made
- Design Rule Checking (DRC) and Layout Versus Schematic (LVS) for the total system must be completed. These checks must be free of essential errors. The reports should be enclosed in the final report.

Report requirements

- The report should be prepared using LATEX, MS Word or a similar word processor and must document all the different phases of the project. Plots of schematics, layout and simulated results for sub-modules and total system must be included in additions to DRC and LVS cadence output reports.
- A discussion of the project work and results are expected and will count towards your grade.
- The organization of the project and the distribution of responsibility within the group must also be included. Please remember that the report must be considered a stand-alone document that should give the reader a complete view of what you have done. This is important to make sure that the entire picture is included in the final assessment and grading of the project.
- Please remember to include the references that you used to prepare the report.
- Note: DO NOT use "Print screen" to capture the waveforms. Cadence provides a way to capture nice waveforms. In the "Virtuoso Visualization & Analysis" window, select "Graph → Major and Minor Grids" and toggle to disable the grids. This captures a clear waveform. Next, select "File → Print". In the Print window, select the name of the printer as "Print to File (PDF)", select the output file path and then select "Options". In the "Qt-subapplication" window, select "A4" as the Paper and "Landscape" as the orientation. Adjust the margins if you like. Click "OK" to exit window. Finally, select "Print" to print the waveform.

References

Dutta, S., Kumar, V., Shukla, A. *et al.* Leaky Integrate and Fire Neuron by Charge-Discharge Dynamics in Floating-Body MOSFET. *Sci Rep* **7**, 8257 (2017). <https://doi.org/10.1038/s41598-017-07418-y>

B. Datta Sahoo, "Ring oscillator based sub-1V leaky integrate-and-fire neuron circuit," *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, USA, 2017, pp. 1-4, doi: 10.1109/ISCAS.2017.8050980.