Noise in analog circuit design

- You are going to be using LTspice

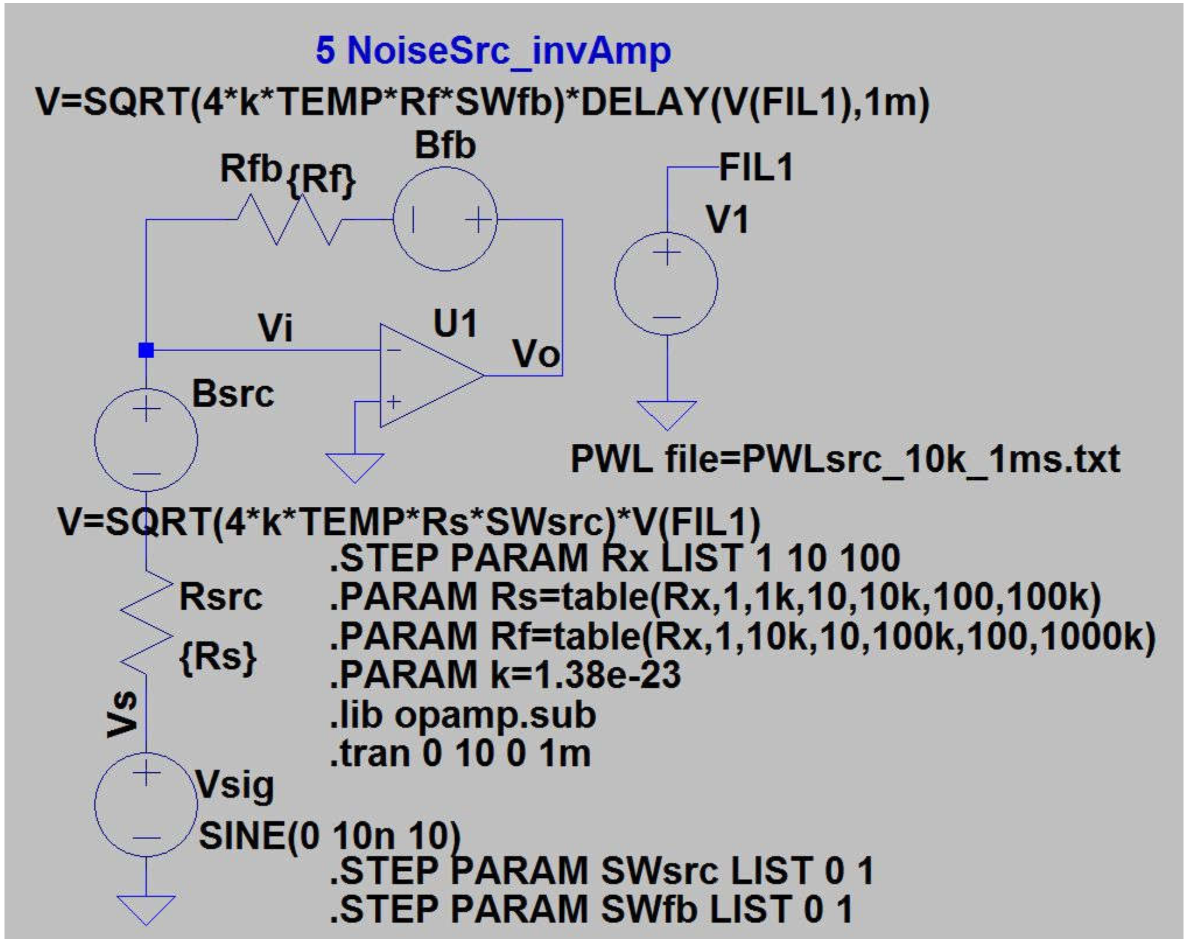
- In the specific, you are going to run NOISE simulations within LTspice

Simulation modes

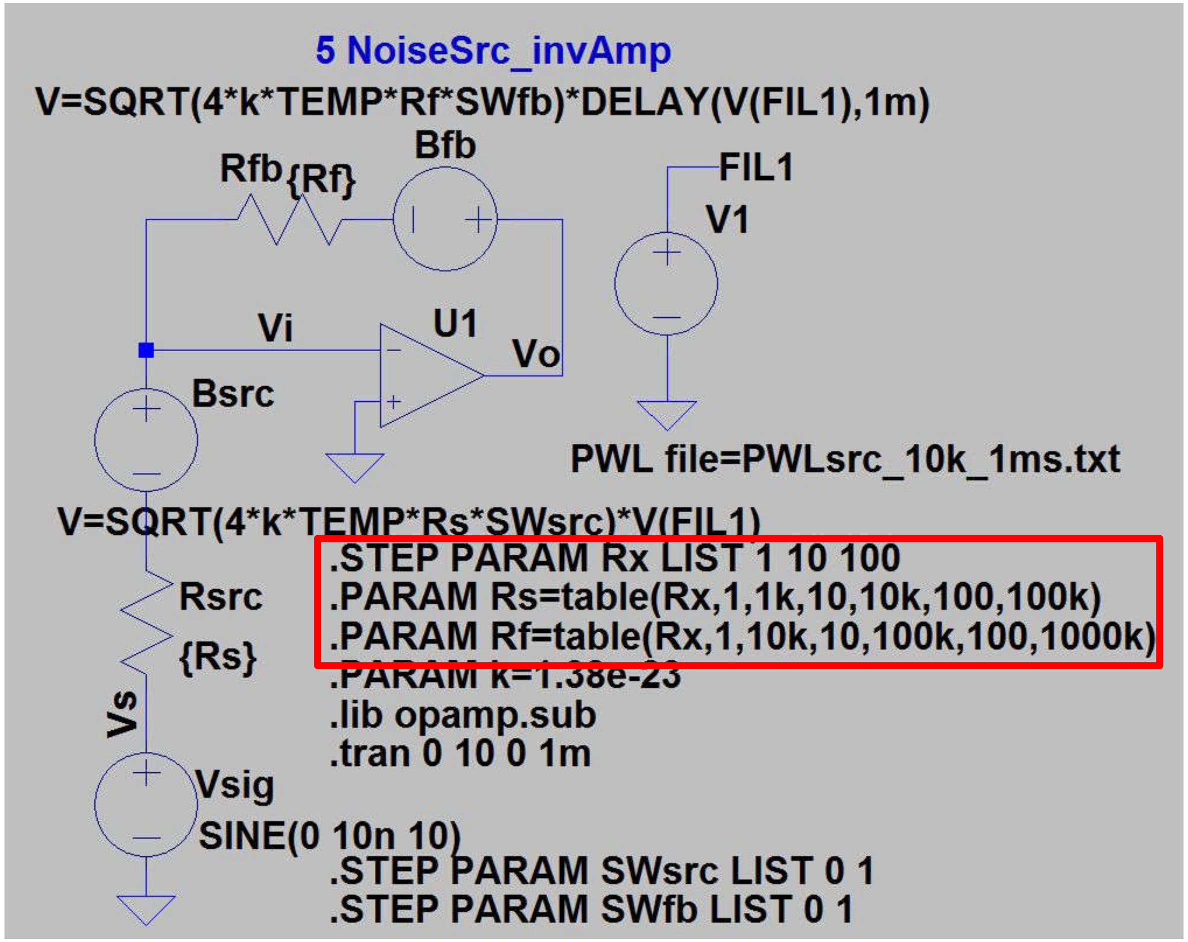
	Time	Frequency
Signal (standard)	.TRAN	.AC
Component noise	.TRAN V (added by user: standard sources or from file) **.NOISETRAN** (noise sources generated by software)	**.NOISE** (noise sources generated by software)
Coupling noise	**.TRAN** --- V (manually added by user: standard V-sources or from file) --- R, C or L modelling parasitic (Extracted by software or manually added by user)	**.AC** --- V (manually added by user: AC) --- R, C or L modelling parasitic (Extracted by software or manually added by user)

LTspice®

Transient component noise simulation



Transient component noise simulation



Preparing CMOS model for mandatory 3

- Will use transistor models for an integrated circuit process: 0.35 μm CMOS from AMS (Austria Micro Systems)

- Preparation:
  a. Include transistor model
  b. Include symbols
  c. Set correct transistor model for transistors in schematic
  d. Set correct length and width for transistors in schematic

Preparing CMOS model for mandatory 3

1. Generally a transistor models can be included as:
    - A model in the standard model library file,
    - As a private library file. Must include link in the schematic, or
    - As “text” in the schematic

    → We chose the first alternative and replace *<program files>/LTC/LTspiceIV/lib/cmp/standard.mos* with our own file

2. Transistor symbols

    - We use our own transistor symbols (that show widths, lengths etc.). They must be on the same directory as we have our schematics (nmos.asy, pmos.asy).

Preparing CMOS model for mandatory 3

3. Correct transistor model:
   - Change the transistor model name for NMOS transistors to MODN and for PMOS to MODP
4. Change transistor width and length
   - Set the correct transistor sizes in each transistor. In figures the transistor sizes are often given as Width/Length. Remember to add “u” or “µ” after the numbers to give correct value. If not the sizes will be interpreted as meters (with no warning). Right click on the component to change height and width.

LTspice: .NOISE analysis

.NOISE is used to simulate component noise in the frequency-domain. The simulator includes by itself noise for all components in the schematic.

Example: **.NOISE V(out) V1 dec 200 1m 1G**

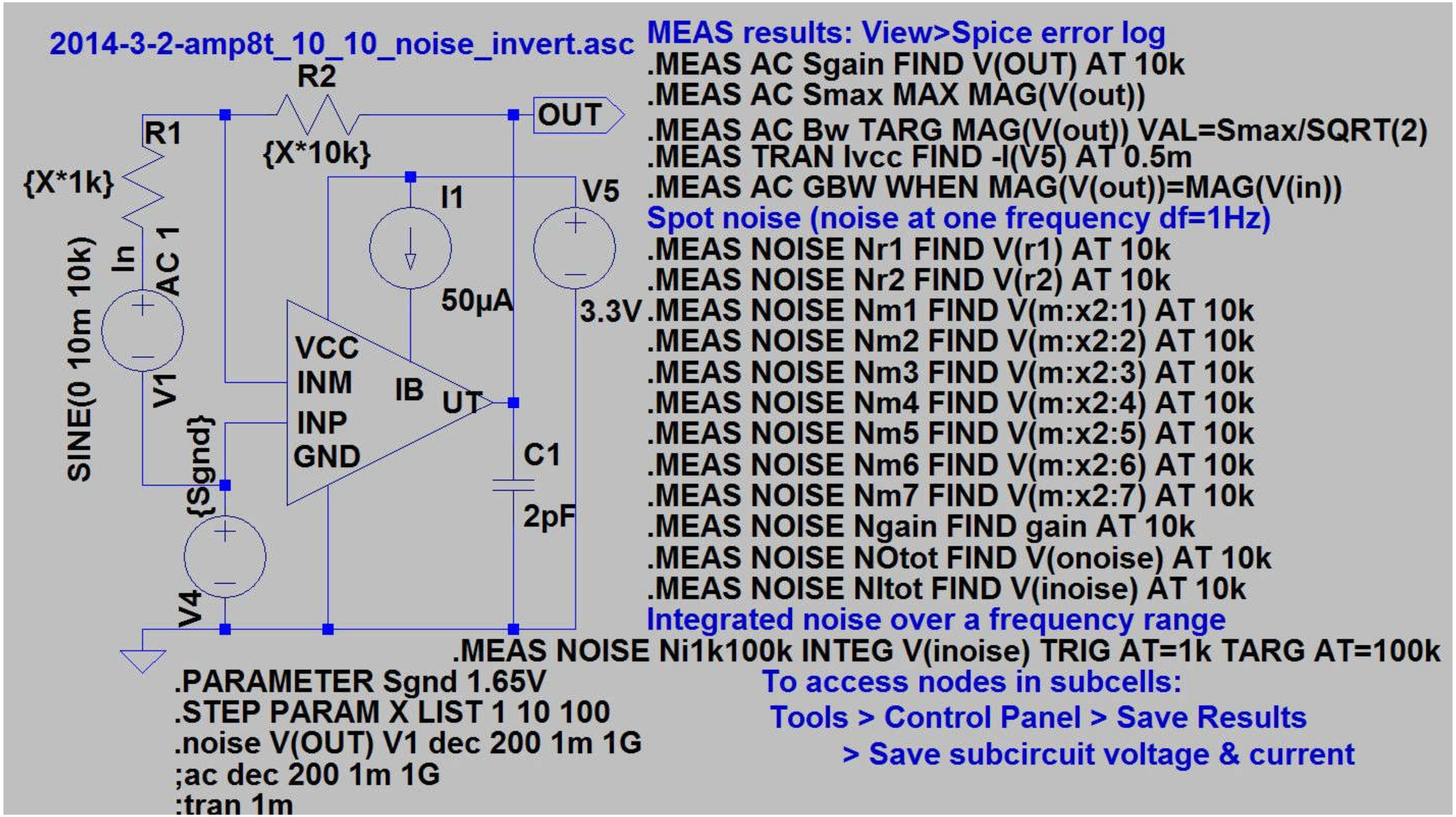
- out: name of network node.
- V1: Name of source. May be voltage or current
- dec: Type of sweep (decade, octave, linear or list)
- 200: Number of points per decade/octave
- 1m: Start frequency (1m=1milli Hz, 1Meg=1Mega Hz)
- 1G: Stop frequency

LTspice: .MEAS – measure and save

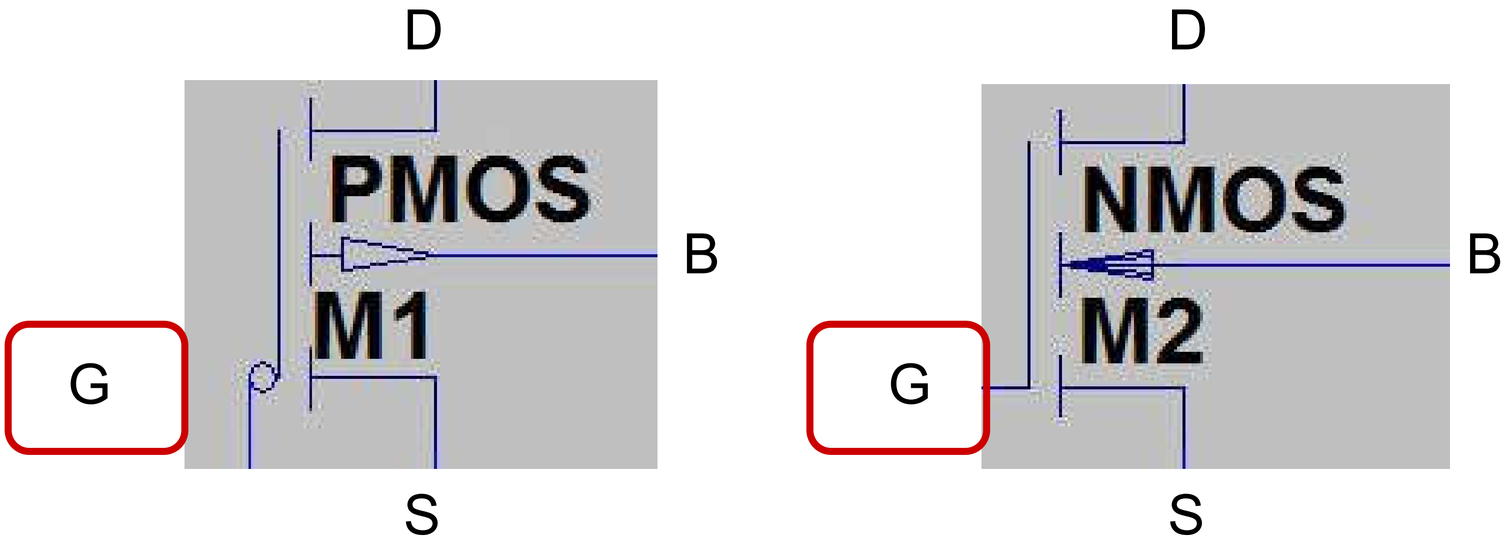
.MEAS directive is used to measure and save some variables in the spice error log (rigth click → View → Spice Error Log

Examples (AC - for AC simulation - NOISE for noise simulation):

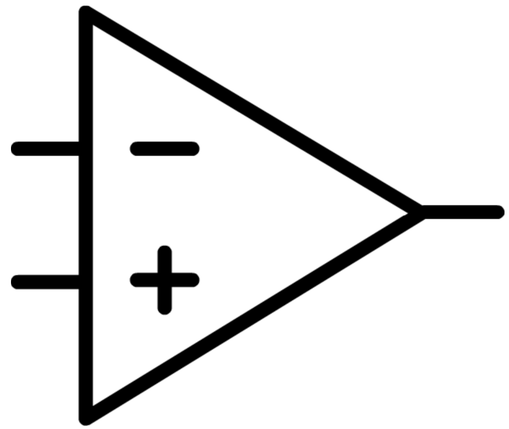
- **.MEAS** AC Smax MAX MAG(V(out))
- **.MEAS** AC BW TARG MAG(V(out)) VAL=Smax/SQRT(2) FALL=1
- **.MEAS** AC GBW WHEN MAG(V(out))=MAG(V(in))
- **.MEAS** NOISE N_R1 FIND V(r1) AT 10k
- **.MEAS** NOISE Ni10k100k INTEG V(inoise) TRIG AT=1k TARG AT=100k


2014-3-2-amp8t_10_10_noise_invert.asc
R2
OUT
R1
{X*10k}
{X*1k}
V5
I1
In
AC 1
SINE(0 10m 10k)
50µA
3.3V
VCC
INM
IB
UT
V1
INP
GND
{Sgnd}
C1
2pF
V4
MEAS results: View>Spice error log
.MEAS AC Sgain FIND V(OUT) AT 10k
.MEAS AC Smax MAX MAG(V(out))
.MEAS AC Bw TARG MAG(V(out)) VAL=Smax/SQRT(2)
.MEAS TRAN Ivcc FIND -I(V5) AT 0.5m
.MEAS AC GBW WHEN MAG(V(out))=MAG(V(in))
Spot noise (noise at one frequency df=1Hz)
.MEAS NOISE Nr1 FIND V(r1) AT 10k
.MEAS NOISE Nr2 FIND V(r2) AT 10k
.MEAS NOISE Nm1 FIND V(m:x2:1) AT 10k
.MEAS NOISE Nm2 FIND V(m:x2:2) AT 10k
.MEAS NOISE Nm3 FIND V(m:x2:3) AT 10k
.MEAS NOISE Nm4 FIND V(m:x2:4) AT 10k
.MEAS NOISE Nm5 FIND V(m:x2:5) AT 10k
.MEAS NOISE Nm6 FIND V(m:x2:6) AT 10k
.MEAS NOISE Nm7 FIND V(m:x2:7) AT 10k
.MEAS NOISE Ngain FIND gain AT 10k
.MEAS NOISE NOtot FIND V(onoise) AT 10k
.MEAS NOISE NItot FIND V(inoise) AT 10k
Integrated noise over a frequency range
.MEAS NOISE Ni1k100k INTEG V(inoise) TRIG AT=1k TARG AT=100k
.PARAMETER Sgnd 1.65V
.STEP PARAM X LIST 1 10 100
.noise V(OUT) V1 dec 200 1m 1G
;ac dec 200 1m 1G
;tran 1m
To access nodes in subcells:
Tools > Control Panel > Save Results
> Save subcircuit voltage & current

CMOS model orientation! Gate always bottom



Exercise 1



1. Ideal amplifier

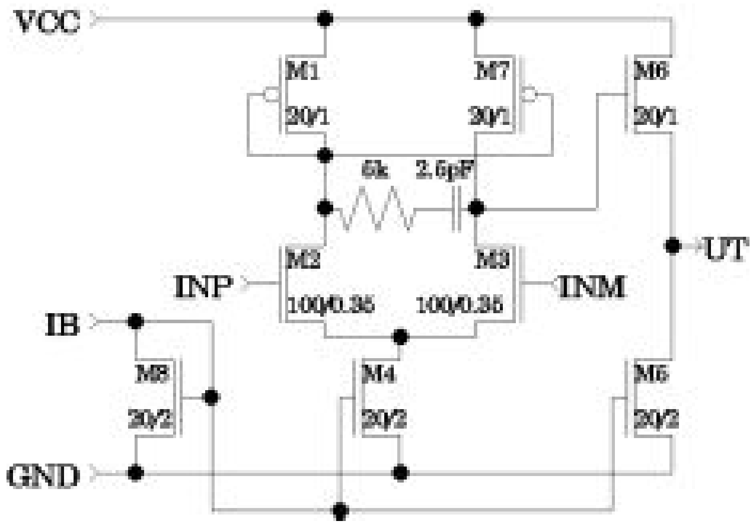
We will first look at an ideal amplifier in an ideal differential amplifier configuration. You can copy the amplifier symbol from the "opamp" circuit in the "Educational" area. *Let the opamp Aol be 100k and the GBW be 10Meg.* Be sure to get the ".include opamp.sub" statement. Build a resistive network around as Figure ii) of Exercise 3 (ground R4). For all cases the relation between the resistors will be R1=R3=Rx and R2=R4=10Rx.

a) Let Rx be 1kΩ, 10kΩ and 100kΩ. Is the gain different in the three cases?
Run .NOISE simulations and find the output noise and equivalent input noise for the three cases at 10kHz. Find the total equivalent input noise both at the positive and the negative input by simulation (in the region where the gain is larger than one). What type of noise is present here?

b) Calculate manually the noise for each of the resistor elements i) locally (at their position), their value at the ii) output and their equivalent value at the iii) input. Use the table below. Which of them has the largest contribution at the output and at the input? Which of these three can you find in the simulation results?

Exercise 2

2. Simple CMOS amplifier



a) Perform AC analysis for the amplifier without feedback (i.e. open-loop). Let the common mode voltage (i.e. DC voltage of input signal) be 1.65V. Do AC analysis with a signal on the positive input (ACpos=1, ACneg=0), on the negative input (ACpos=0, ACneg=-1) and with differential signals on both inputs (ACpos=1, Acneg=-1).

b) Replace the ideal amplifier in the feedback network in task “1 Ideal amplifier” with our new amplifier. Let Rx = 1kΩ. Inspect the simulation results on the positive input and the output. What is the frequency range at which the flicker noise is dominant?

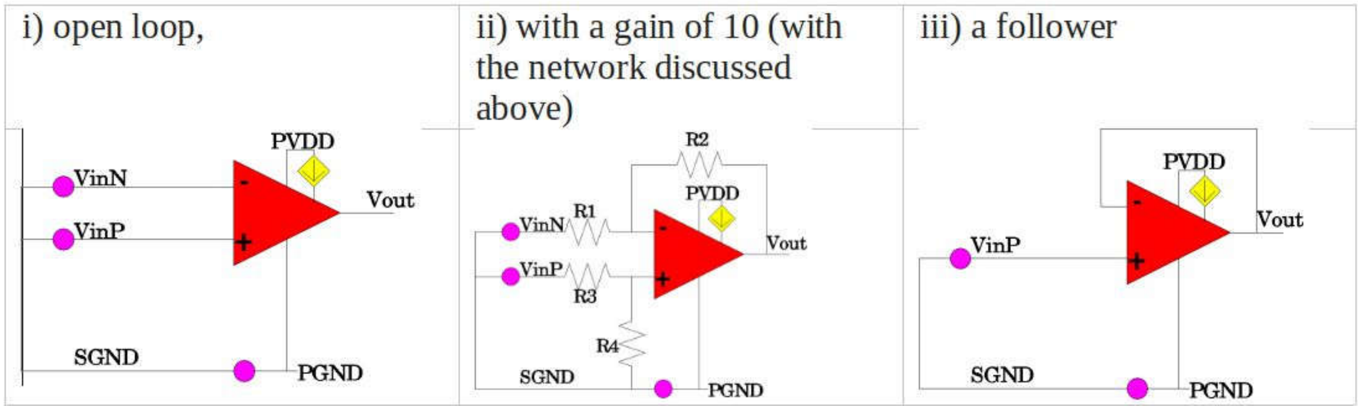
c) We would like to know the (spot) noise at some frequencies and the integrated noise over some frequency ranges. Find the (positive) input and output noise at 1Hz, 1kHz, 1MHz and 1GHz. Then find the noise for the areas 1Hz-1kHz, 1kHz-1MHz and 1Hz-1MHz. (Use the .MEAS statement). How can we manually calculate the noise in the range 1Hz-1MHz from the two subareas we found through simulation?

d) Perform the same NOISE simulation as in task 1 with Rx = 1kΩ, Rx = 10kΩ and Rx = 100kΩ. Simulate with a capacitive load of 1pF. List the six largest sources of noise at 1MHz for all three cases. Comment on the result.

Exercise 3

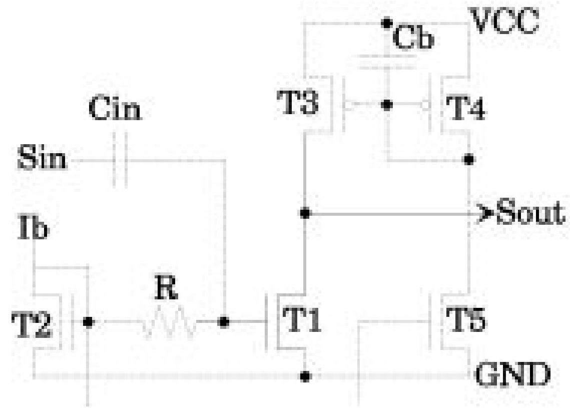
3. Noise in Open-loop, closed-loop, follower configuraiton

In this task you shall find the spot noise at 1MHz and the integrated noise from 1 Hz to 1 MHz at output and the positive equivalent input. Find this for open loop, for 10x (with the network over) as well as a follower. Present your results in a table.



The small pink circles are voltage sources. The voltage sources between SGND and PGND is a 1.65V DC source.

Exercise 4



4. Common source input stage - RF

a) How large must Cin be to not mute the signal more than about 10%? Generate a figure with Cin on the x-axis and signal strength on the Y-axis.

b) How large must R be to not contribute significantly (<10%) of the total noise? (R will have minimum contribution for small and large resistor values. However, at small R values the resistor will mute the input resulting in a low gain. Hence we have to go for a sufficient large resistor value.) You may use .MEAS NOISE N_r1_onoise FIND V(r1)/V(onoise) AT 1Meg to find the relation between R1 noise and total noise.

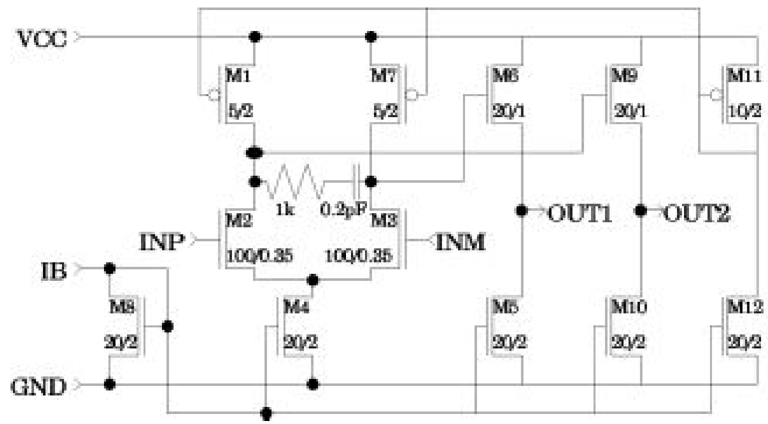
c) What does the Cb do? How much noise reduction can we achieve with Cb and how large must Cb be to achieve this? What is the gain, noise on the output and equivalent input noise now with a large Cb?
Use the values you have found for Cin, R and Cb in the following.

d) Try doubling the width of the NMOS transistor, the length of the NMOS transistor, the PMOS transistor width and length of the PMOS transistor. Find the output noise, equivalent input noise as well as the gain for these 5 setups (reference + 4 variations) at 1MHz and put them up in a table.

e) Increase the power Ib in steps of 10µA from 10µA to 100µA, and find the output noise, equivalent input noise and gain at 1MHz. Plot the equivalent input noise as a function of current.

f) Make copies of the present structure and replace MODN and MODP (3.3V models) with the standard LTspice NPN and PNP transistors. Put up a table with the output noise, equivalent input noise and gain for the two cases and comment on your results.

Exercise 5



5. CMOS amplifier with differential input and output

Use the same input values and the same transistor models as in the previous task.

a) Find the gain for each signal input, the differential gain, output noise and equivalent input noise with a 50μA current bias.

b) Set up a simulation to find the effects of noise from the supply voltage VCC. Find impact on each of the outputs individually and on the difference between the outputs. Do the same simulation first where M2 and M3 are identical (as defined above) and then with the width of the M2 1% greater than the width of M3. Put the results in a table and comment.

d) Try to specify the variation in power consumption at VCC when the input signal is a 1MHz sine with amplitude 10mV.