INF 5230 Electronic Noise – calculation and countermeasures

Mandatory lab.

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Deadlines:

Schematic – subtask 2: 08:00 11th of November
Final Report –08:00 22th of November,

Assessment: Approved / Not approved.
Reports are submitted on an individual basis. The tasks will consist of schematics that are used, simulation results, text EXPLAINING what has been done as well as an analysis of the results. Put up a summary table and comment at the end of each task when relevant. USE WHITE/LIGHT BACKGROUND for the plots! Avoid yellow curves.

1. Ideal amplifier

We will first look at an ideal amplifier in an ideal differential amplifier configuration. You can copy the amplifier symbol from the "opamp" circuit in the "Educational" area. *Let the opamp Aol be 100k and the GBW be 10Meg.* Be sure to get the "include" statement. Build a resistive network around as indicated in Figure 3-4 "Differential amplifier using one op amp" page 56 (figure in Motchenbacher). For all cases the relation between the resistors will be R1=R3=Rx and R2=R4=10Rx..
a) Let Rx be 1kΩ, 10kΩ and 100kΩ. Is the gain different in the three cases?
Run .NOISE simulations and find the output noise and equivalent input noise for the three cases at 10kHz. Find the total equivalent input noise both at the positive and the negative input by simulation (in the region where the gain is larger than one). What type of noise is present here?
b) Calculate manually the noise for each of the resistor elements i) locally (at their position), their value at the ii) output and their equivalent value at the iii) input. Use the table below. Which of them has the largest contribution at the output and at the input? Which of these three can you find in the simulation results?

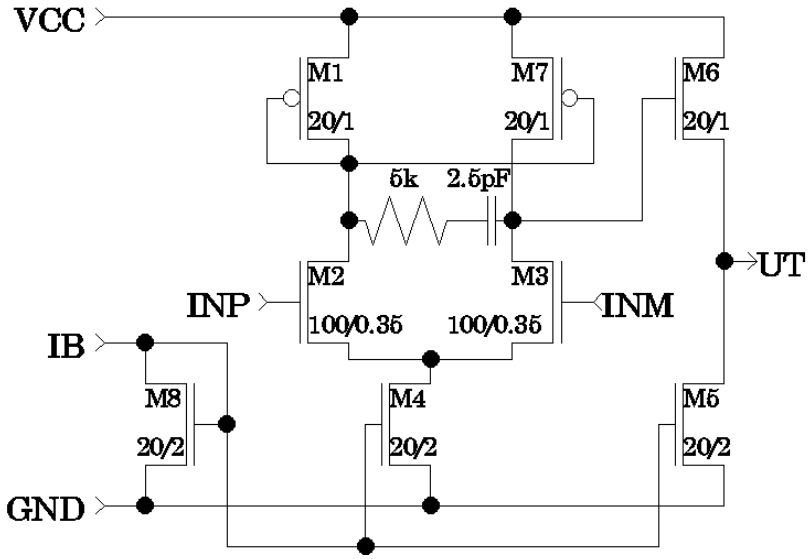
Example table:

	Local noise (nV/√Hz)	Gain to output	Noise at output (nV/√Hz)	Equivalent noise at input(nV/√Hz)
R1				
R2				
R3				
R4				
Total				

2. Simple CMOS amplifier

The ideal amplifier provides unrealistic behaviour at higher frequencies. We will now replace the amplifier with a simple 8 transistor CMOS amplifier.

Before we can draw the amplifier we must install model file and symbols. Download standard.mos and replace the original model file located at <programfiles>/LTC/LTspiceIV/lib/cmp/ with it. Download the symbols for pmos and nmos (pmos4.asy and nmos4.asy) and put these symbols in the directory where you have your schematics. (Links are also provided in the lecture plan.). Then draw the following schematic:



Change model designations respectively to MODP and MODN. (You can copy and modify the schematic INVsd.sch). Let bias reference current IB be 50µA. Remember to connect MODN substrate to low potential (GND) and correspondingly MODP substrate/well to high potential (VCC). The transistor sizes are given as width/length in the figure. Widths and lengths must be specified with µ or u after the size in LTspice! *The supply voltage VCC is 3.3V.*

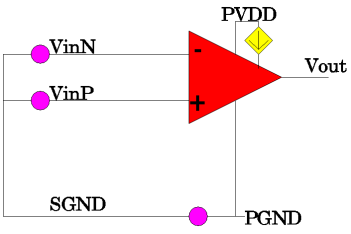
Make a symbol with the same name as the schematic. (When the simulator finds a symbol it looks for a schematic with the same name.)
a) Perform AC analysis for the amplifier without feedback (i.e. open-loop). Let the common mode voltage (i.e. DC voltage of input signal) be 1.65V. Do AC analysis with a signal on the positive input (ACpos=1, ACneg=0), on the negative input (ACpos=0, ACneg=-1) and with differential signals on both inputs (ACpos=1, ACneg=-1).
b) Replace the ideal amplifier in the feedback network in task "1 Ideal amplifier" with our new amplifier. Let Rx = 1kΩ. Inspect the simulation results on the positive input and the output. What is the frequency range at which the flicker noise is dominant?
c) We would like to know the (spot) noise at some frequencies and the integrated noise over some frequency ranges. Find the (positive) input and output noise at 1Hz, 1kHz,

1MHz and 1GHz. Then find the noise for the areas 1Hz-1kHz, 1kHz-1MHz and 1Hz-1MHz. (Use the .MEAS statement). How can we manually calculate the noise in the range 1Hz-1MHz from the two subareas we found through simulation?
d) Perform the same NOISE simulation as in task 1 with Rx = 1kΩ, Rx = 10kΩ and Rx = 100kΩ. Simulate with a capacitive load of 1pF. List the six largest sources of noise at 1MHz for all three cases. Comment on the result.

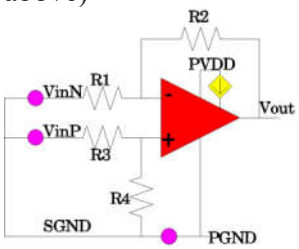
3. Open loop, 10x gain and closed loop.

In this task you shall find the spot noise at 1MHz and the integrated noise from 1 Hz to 1 MHz at output and the positive equivalent input. Find this for open loop, for 10x (with the network over) as well as a follower. Present your results in a table.

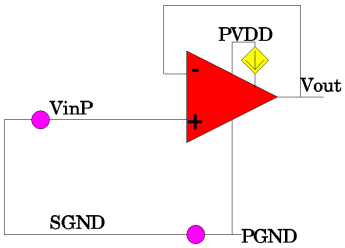
i) open loop,



ii) with a gain of 10 (with the network discussed above)



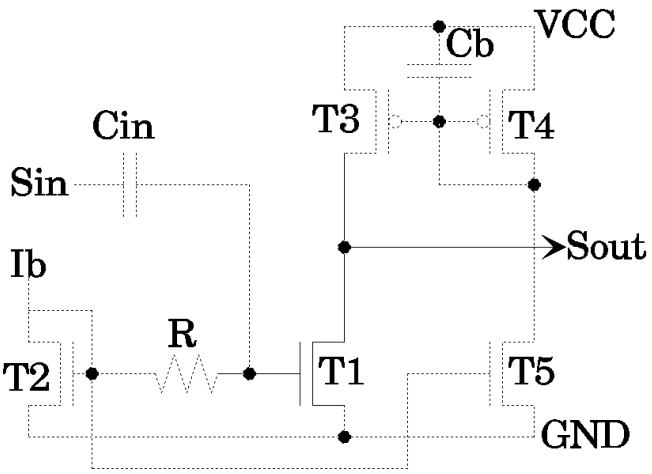
iii) a follower



The small pink circles are voltage sources. The voltage sources between SGND and PGND is a 1.65V DC source.

4. Common source input stage

We will in this subtask look at a Common-Source architecture popular in RF-input stages.



The central element is the transistor T1. The other components are used to provide correct bias. The T1 source is connected to ground (common), while the input signal on the gate will be amplified to the T1 drain.

We wish only to amplify a narrow frequency bandwidth and can ignore the DC-value of the input signal. We leverage this to provide the T1 gate the DC value that provides optimal performance. We place a capacitor (Cin) between Sin (signal input) and the T1 gate to achieve DC isolation. The value of the capacitor must be chosen so that the frequency we want to amplify is not reduced too much by the capacitor.

The T1 working current is decided by an external current source at the input Ib. The circuit is based on multiple current mirrors. The current is reflected from T2 to T1 and T5, and the current through T4 is reflected to T3. In the current mirrors the gate length of T2, T1 and T5 should be equal and the gate length of T4 and T3 should be equal. To simplify we choose to let all NMOS transistors to have the same width and length, and both the PMOS transistors to have the same width and length. Then all the local currents will be equal to the reference current Ib. (In an actual realization, we want currents through T2, T4 and T5 to be minimal in order to save power. Proper current in T1 and T3, will be achieved through the choice of the width ratio of the current mirrors.)

Parameters:

We will focus on the amplification of a signal at 1MHz. During noise analysis, we calculate the noise level between 0.8MHz and 1.2MHz. Let the input signal have an amplitude of 1mV.

Initially we let the NMOS transistor lengths be 0.35µm and the PMOS transistor length to be 2µm. The NMOS transistors may have a width of 35µm and the PMOS transistors 20µm width. We use the models MODN and MODP as in mandatory number 2. VCC is 3.3V. Start by giving Cb a very low value. R can be set to 1kΩ. We start with a bias current Ib = 10µA.

a) How large must Cin be to not mute the signal more than about 10%? Generate a figure with Cin on the x-axis and signal strength on the Y-axis.
b) How large must R be to not contribute significantly (<10%) of the total noise? (R will have minimum contribution for small and large resistor values. However, at small R values the resistor will mute the input resulting in a low gain. Hence we have to go for a sufficient large resistor value.)

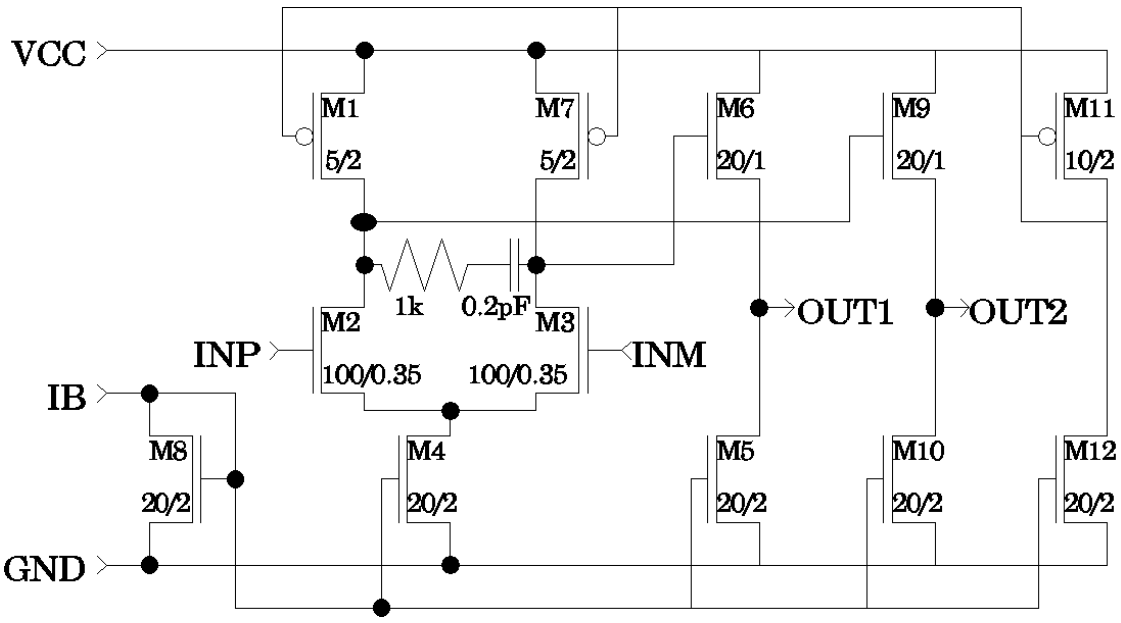
(You may use .MEAS NOISE N_r1_onoise FIND V(r1)/V(onoise) AT 1Meg to find the relation between R1 noise and total noise.)

c) What does the Cb do? How much noise reduction can we achieve with Cb and how large must Cb be to achieve this? What is the gain, noise on the output and equivalent input noise now with a large Cb?

Use the values you have found for Cin, R and Cb in the following.
d) Try doubling the width of the NMOS transistor, the length of the NMOS transistor, the PMOS transistor width and length of the PMOS transistor. Find the output noise, equivalent input noise as well as the gain for these 5 setups (reference + 4 variations) at 1MHz and put them up in a table.
e) Increase the power Ib in steps of 10µA from 10µA to 100µA, and find the output noise, equivalent input noise and gain at 1MHz. Plot the equivalent input noise as a function of current.
f) Make copies of the present structure and replace MODN and MODP (3.3V models) with the standard LTspice NPN and PNP transistors. Put up a table with the output noise, equivalent input noise and gain for the two cases and comment on your results.

5. CMOS amplifier with differential input and output

In this task, we modify the amplifier from task two to have differential output.



Use the same input forces and the same transistor models as in the previous task.
a) Find the gain for each signal input, the differential gain, output noise and equivalent input noise with a 50μA current bias.

b) Set up a simulation to find the effects of noise from the supply voltage VCC. Find impact on each of the outputs individually and on the difference between the outputs. Do the same simulation first where M2 and M3 are identical (as defined above) and then with the width of the M2 1% greater than the width of M3. Put the results in a table and comment.

d) Try to specify the variation in power consumption at VCC when the input signal is a 1MHz sine with amplitude 10mV.