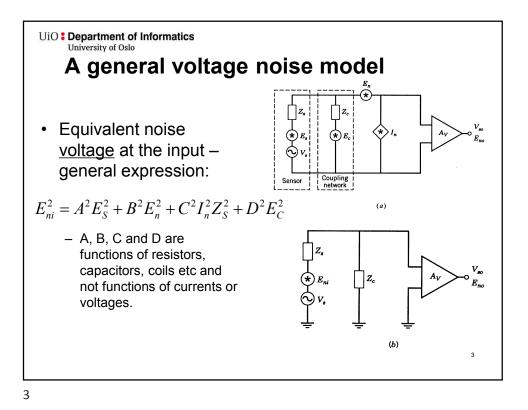


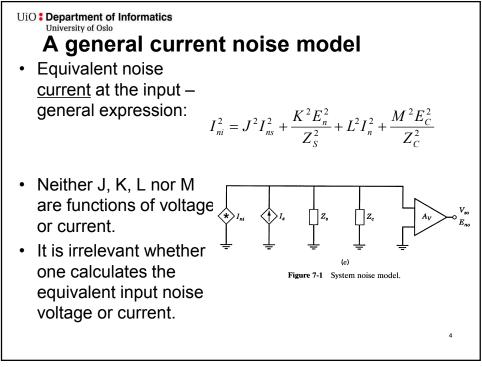
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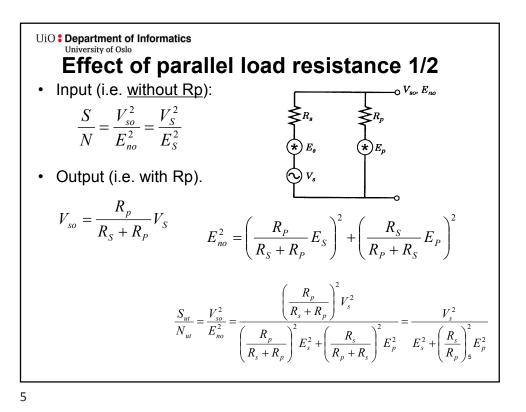
- Modelling of noise must include:
  - Sensors
  - Bias and coupling network
  - Amplifiers

## • We use our standard method:

- 1. Determine the total noise at output: Eno
- 2. Determine the system gain: Kt
- 3. Divide *Eno* with Kt:  $Eni^2 = Eno^2/Kt^2$

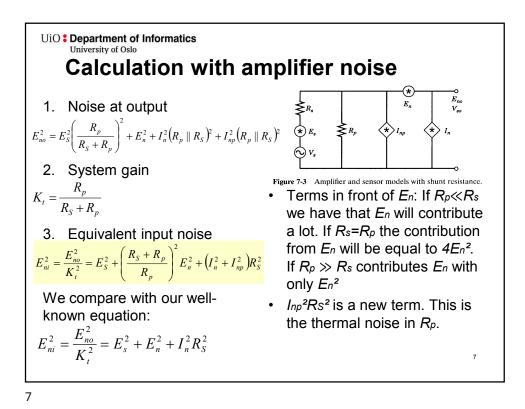


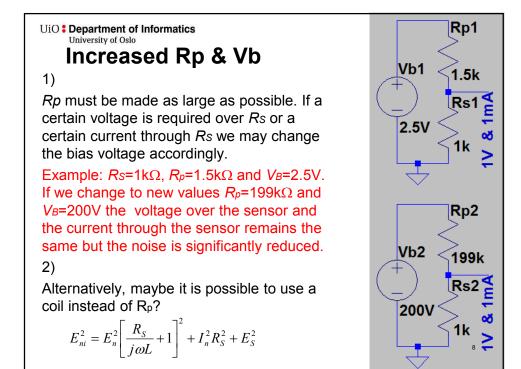


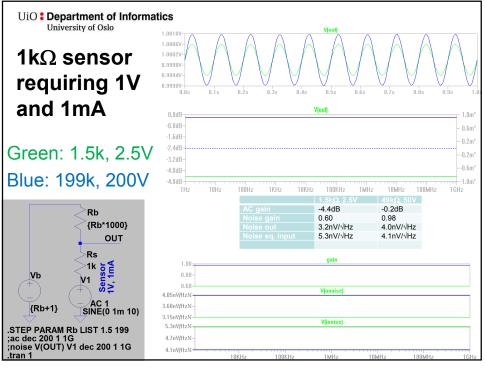


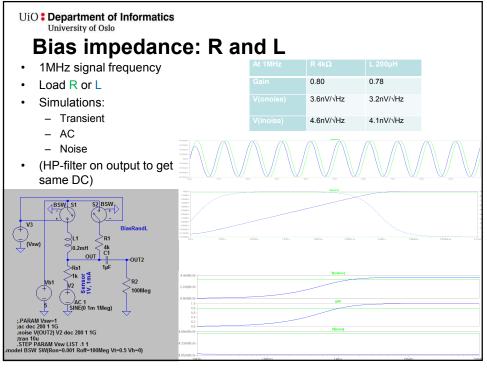
UiO Department of Informatics University of Oslo Effect of parallel load resistance 2/2  $\frac{S_{ut}}{N_{ut}} = \frac{V_{so}^2}{E_{no}^2} = \frac{\left(\frac{R_p}{R_s + R_p}\right)^2 V_s^2}{\left(\frac{R_p}{R_s + R_p}\right)^2 E_s^2 + \left(\frac{R_s}{R_p + R_s}\right)^2 E_p^2} = \frac{V_s^2}{E_s^2 + \left(\frac{R_s}{R_p}\right)^2 E_p^2}$ When  $R_s = R_p$  then  $E_s = E_p$  and we get that (S/N)ut=

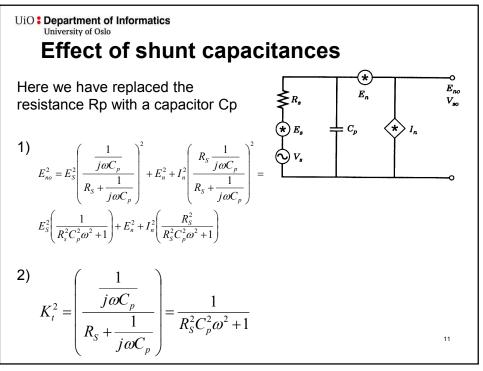
When  $R_s = R_p$  then  $E_s = E_p$  and we get that  $(S/N)_{ut} = \frac{1}{2}(V_s^2/E_s^2) = \frac{1}{2}(S/N)_{inn}$ .  $R_p$  equally reduces  $V_s$  and  $E_s$  but contribute in addition with its own noise. When  $R_s \gg R_p$  decreases  $(S/N)_{ut}$  towards zero, while when  $R_s \ll R_p$  will  $(S/N)_{ut}$  increase towards  $(S/N)_{inn}$  which is the best that can be achieved.











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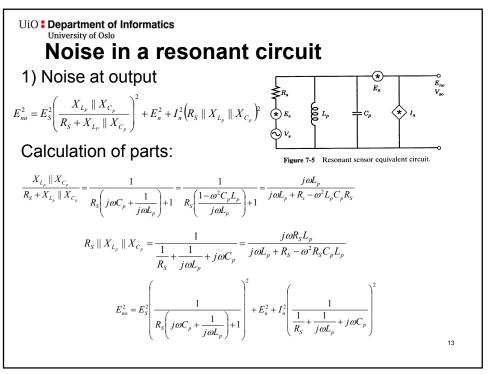
3) 
$$E_{ni}^{2} = \frac{E_{no}^{2}}{K_{t}^{2}} = E_{s}^{2} + E_{n}^{2} \left( R_{s}^{2} C_{p}^{2} \omega^{2} + 1 \right) + I_{n}^{2} R_{s}^{2}$$

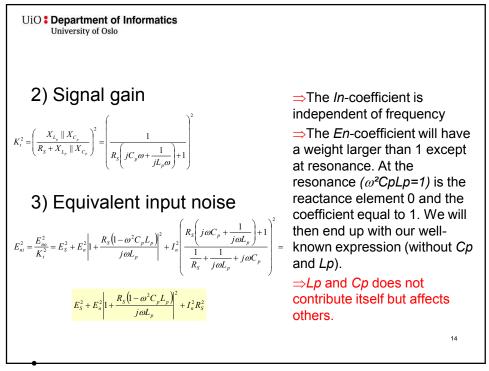
We compare with our well-known expression:

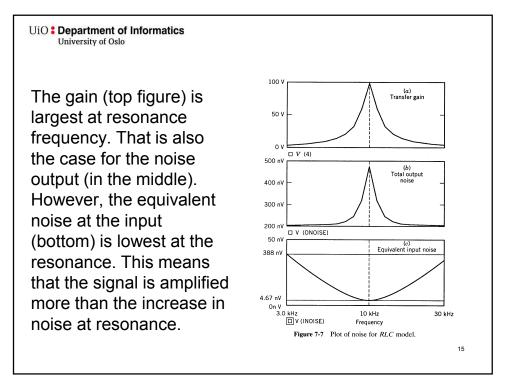
$$E_{ni}^{2} = \frac{E_{no}^{2}}{K_{t}^{2}} = E_{s}^{2} + E_{n}^{2} + I_{n}^{2}R_{s}^{2}$$

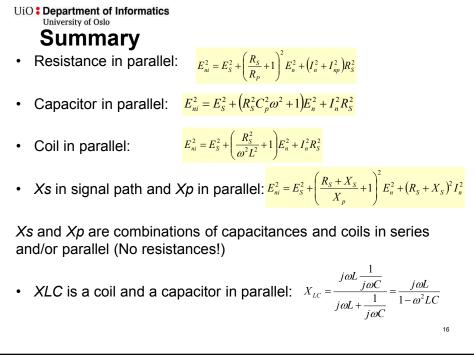
 $\Rightarrow E_n^2$  is multiplied by  $(Rs^2C_p^2\omega^2+1)$ . Note  $! Rs^2C_p^2\omega^2$  will often be substantially less than 1.

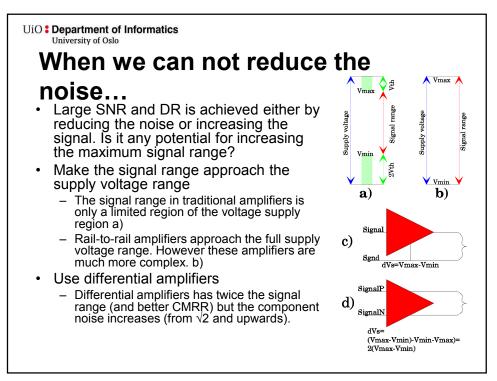
Only the *En*<sup>2</sup> contribution increases. NB! *Cp* is no noise source! Cp is not the input capacitance of the amplifier. This is included in *En*, *In* and *Kt*.

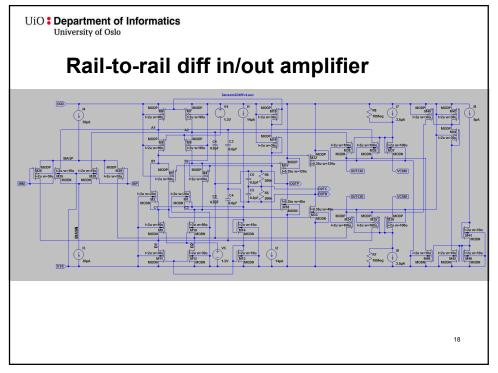


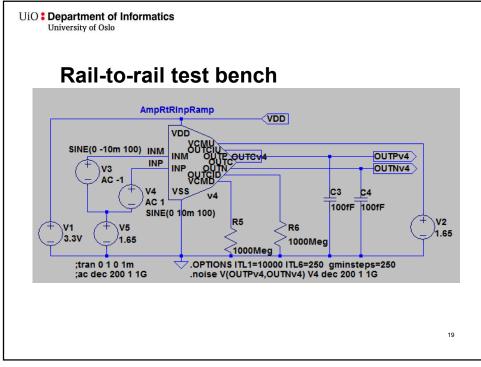


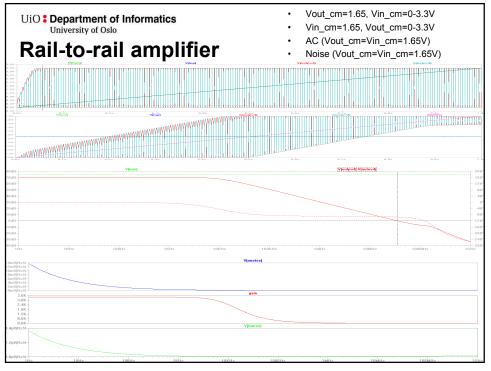


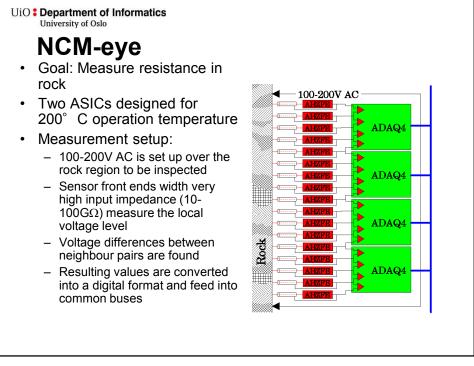


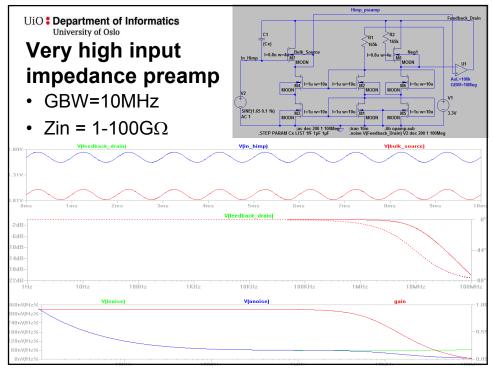


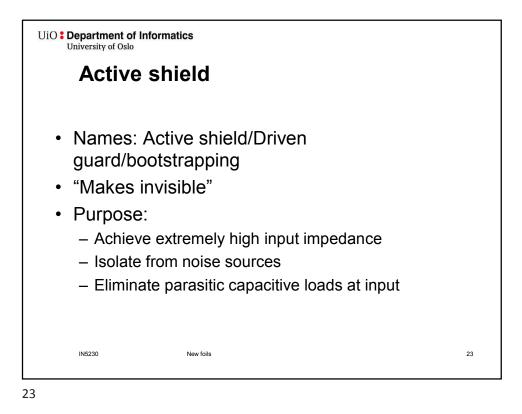


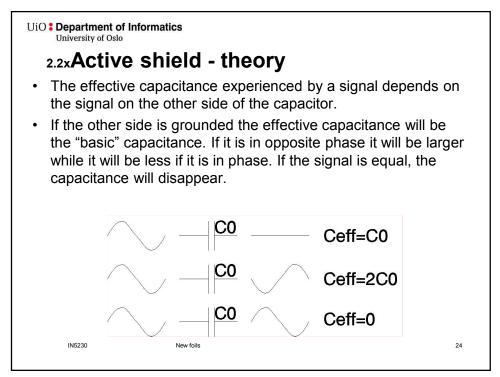


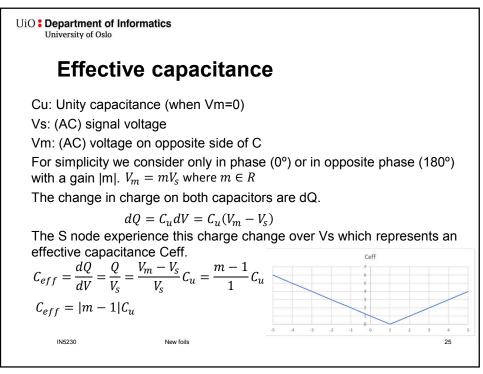


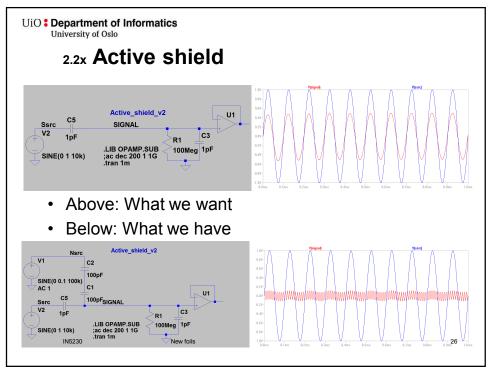


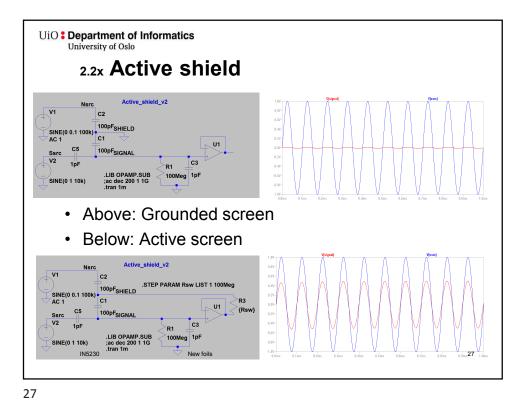


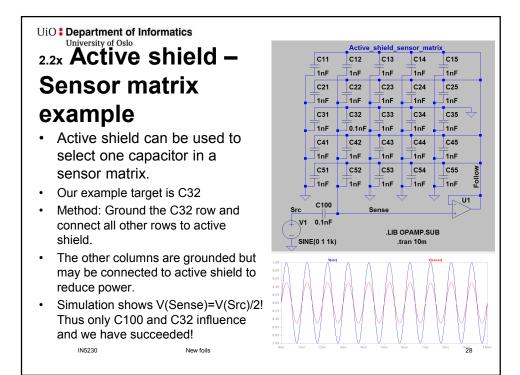


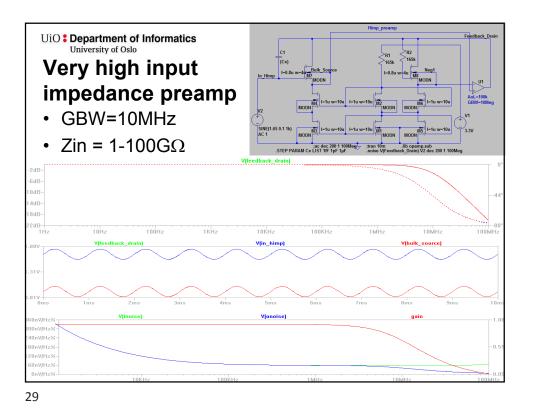












UiO **Department of Informatics** University of Oslo Driven guard pad Pad well connected to driven ٠ guard. ESD connected to buffer ٠ **Driven Guard Pad** output. For this use the guard and D2 D signal have the same DC. U1 ESD PAD • Power (IO-ring) are not ESD crossing signal path. D D1 Driven WELL Bottom figure: Driven guard • pad surrounded by two standard pads. IN5230 New foils 30