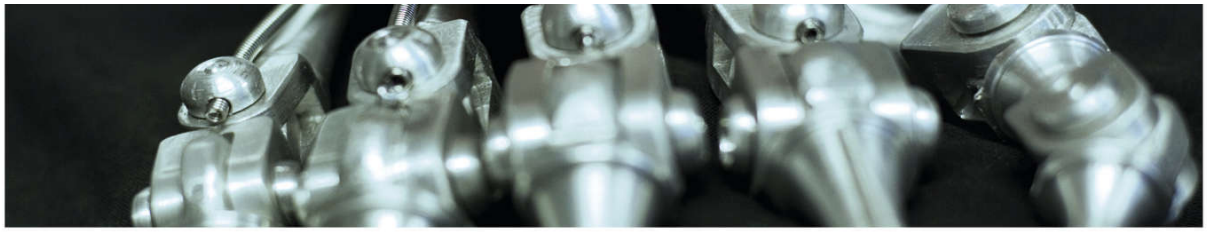

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IN5230
Electronic noise –
Estimates and countermeasures

Lecture 13 (Mot 10)
Amplifier Architectures

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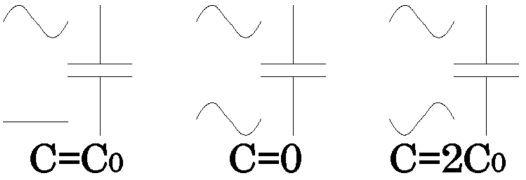
- When a transistor is used in an amplifier, oscillator, filter, sensor, etc. it will also be a need for passive elements like resistors, capacitors and coils to provide biasing so that the transistor has the correct working point. These passive elements will influence on the noise. In the following we will look at some architectures and how they affect the equivalent input noise.

Miller capacitance

Before we look at the transistor configurations we need a fast repetition of the Miller effect.

- When a capacitor is connected between a signal line and a stable potential the signal line will experience a capacitance according to the standard formula ($C=\varepsilon A/t$).
- If the potential on the other side are in phase a smaller capacitance will be experienced. If the signal is exactly equal the capacitance will "disappear".
- If the signal is in opposite phase the experienced capacitance will be larger. If it is in opposite phase and exactly equal the capacitance will be double.



RED

Transistor configurations:

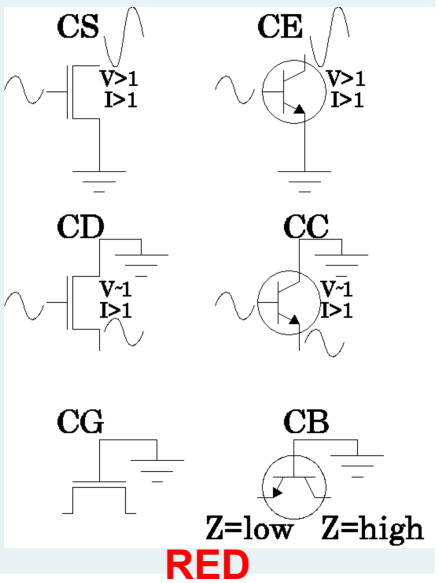
- There are mainly three alternatives for placing a FET/BJT in an architecture:

CS/CE has both voltage and current amplification resulting in the highest gain. But it has also the highest input capacitance (due to the Miller effect)

CD/CC has a high current gain but a voltage gain close to one. It has a low input capacitance (from the Miller effect) resulting in a high input impedance. It also has low output impedance.

CG/CB is used to achieve low input impedance and high output impedance.

FET	BJT	
CS: Common Source	CE: Common Emitter	
CD: Common Drain	CC: Common Collector	
CG: Common Gate	CB: Common Base	



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10-2 Common Emitter

The schematic shows a transistor that is biased for low noise operation between 10Hz and 10kHz.
The noise values are as follows:

	10Hz	10kHz
E_n	2nV	2nV
I_n	2pA	0.3pA
R_0	1000Ω	6700Ω
NF@R_0	1.8dB	0.3dB

The noise schematic shows a hybrid-π model together with passive bias elements.

Note that when V_{EE} and V_{CC} are stable DC-sources, they are merged together with ground during noise analysis.

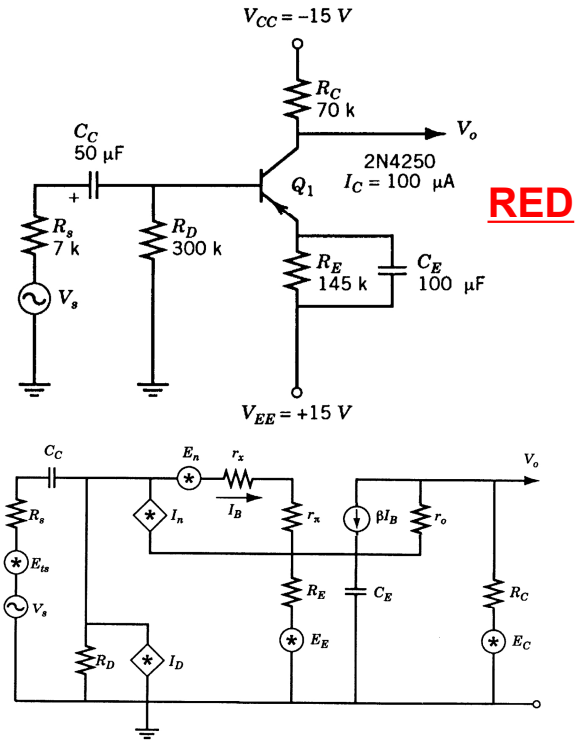

Figure 10-2 Noise and small-signal equivalent circuit for CE stage.

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The voltage gain Kt:

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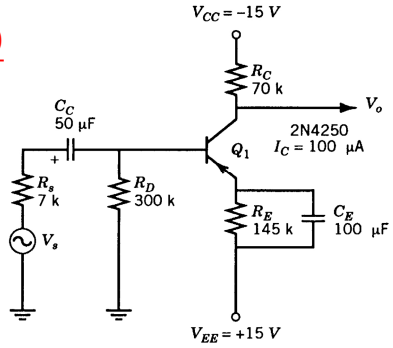


$$K_t \cong \left(\frac{-\beta R_L}{Z_i}\right)\left(\frac{Z_i \parallel R_D}{Z_S + Z_i \parallel R_D}\right)$$

Kt is the voltage gain from *Vs* to *Vo*. The first parenthesis is the voltage gain within the transistor (β is I_{CE}/I_{BE}) while the second parenthesis is the network in front of the base.

$$Z_i = r_x + r_\pi + (\beta + 1)Z_E$$

The input resistance Z_i includes the resistance you can see through the base towards emitter.

$$R_L \cong R_C \parallel r_0 \parallel R_{i2}$$

The load resistance consists of the collector bias resistance, the transistor internal resistance and the input resistance of the next stage: R_{i2}.

$$Z_E = R_E \parallel -jX_E$$

The emitter impedance consists of a real part and an imaginary part (a resistance and a capacitance in parallel).

$$Z_S = R_S - jX_C$$

The source impedance is a resistance in series with a capacitor.

If we assume ignorable loss in biasing, coupling and feedback we can simplify the expression for *Kt* to:

$$K_t \cong -\frac{\beta R_L}{Z_S + r_x + r_\pi + \beta Z_E}$$

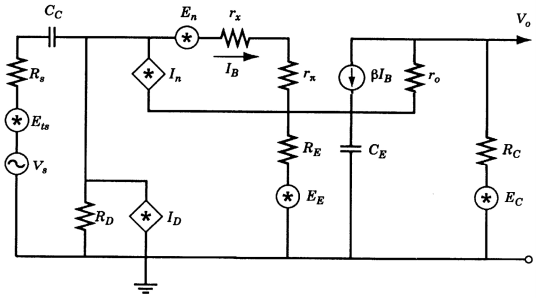


Figure 10-2 Noise and small-signal equivalent circuit for CE stage.

If $Zs \ll r_\pi$ and $Z_E \ll r_e$ the expression is simplified to:

$$K_t \cong -\frac{R_L}{r_e} = -g_m R_L$$

If we simplify and ignore the external load we have:

$$K'_t = K_t \quad for \quad R_L = R_C$$

We will then have the following expression for the equivalent input noise:

$$E_{ni}^2 \cong E_{ns}^2 + E_n^2\left(\frac{R_S+R_D}{R_D}\right)^2 + (I_n^2 + I_D^2)(R_S - jX_C)^2 + \frac{E_E^2}{1+(\omega R_E C_E)^2} + \left(\frac{E_C}{K'_t}\right)^2.$$

In the expression, we recognise the first part (say from section. 7.3). Last term is also known. The second last term, however, needs some comments. The noise voltage over R_E will not be E_E for higher frequencies, because C_E will "attempt to short-circuit" this. To find the expression we first model the thermal noise in R_E as a current noise of size $I_E=E_E/R_E$. The noise current over R_E and C_E will be:

$$E'^2_E = I_E^2 \cdot (C_E \parallel R_E) = \frac{E_E^2}{R_E^2}\left|\frac{R_E}{j\omega R_E C_E + 1}\right|^2 = \frac{E_E^2}{1+(\omega R_E C_E)^2}$$

YELLOW

Back to the expression for *Eni*:

$$E_{ni}^2 \cong E_{ns}^2 + E_n^2\left(\frac{R_S + R_D}{R_D}\right)^2 + (I_n^2 + I_D^2)(R_S - jX_C)^2 + \frac{E_E^2}{1 + (\omega R_E C_E)^2} + \left(\frac{E_C}{K'_t}\right)^2$$

From the expression we find that to have low noise:

⇒ R_D should be large relative to R_S.

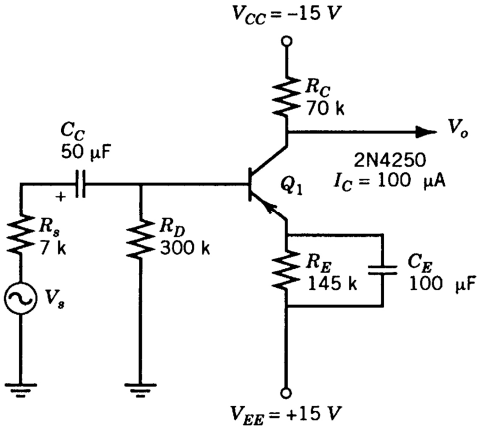
⇒ C_C should be large.

⇒ R_s should be small.

⇒ R_E should be small if C_E is not large

⇒ C_E should be large.

⇒ K_t should be large.



If the AC-coupling is not needed, we can remove R_D and C_C.
CE (Common Emitter) has the greatest power amplification.
Thus noise from stages following the amplifier can probably be ignored.

Choice of capacitance values

C_C is a high pass filter together with the resistances at the transistor gate (I.e. bias resistance in parallel with the transistor input resistance).
With regard to noise, $1/(\omega C_C)$ should be much less than R_S at the lowest relevant frequency. This is because these are added and determines the contribution of *In*: $In \cdot (R_S + j/(\omega C_C))$. Obviously, the last term should be tried made small (<1/100) relative to R_S. NB! Hence due to noise C_C must not be used intentionally for filter functions!

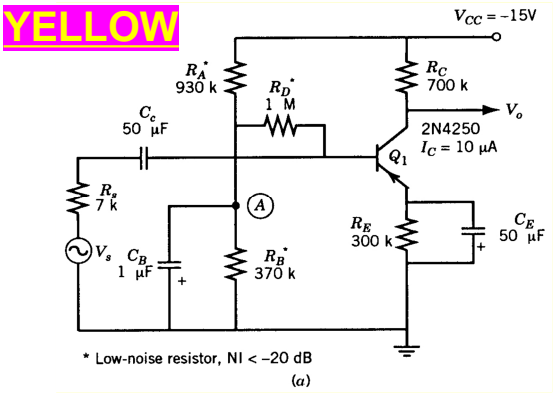
C_E should short-circuit the emitter AC-wise to ground. The impedance of C_E should be small relative to the internal resistance in the emitter: r_e.
Basically noise in R_E has the same weight as the noise in the source (gain=1), however C_E will reduce the contribution from R_E.

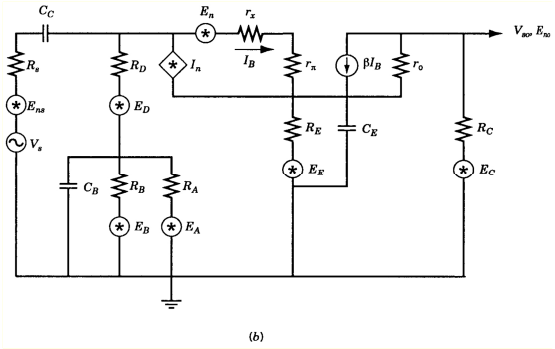
$$\frac{E_{tE}^2}{1 + \omega^2 R_E^2 C_E^2} << E_S^2$$ YELLOW

Common-emitter with one voltage supply

Here a point A is established supplying a stable DC potential for the base. The point A is AC-wise short circuited to ground through C_B.

YELLOW



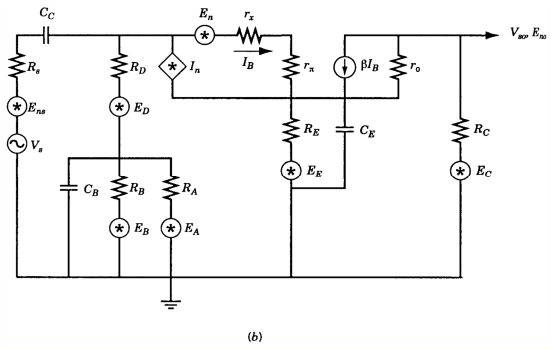


	10Hz	10kHz
En	4.5nV	4.5nV
In	0.3pA	0.1pA
R0	10kΩ	45kΩ
NF@R0	0.68dB	0.35dB
Kt	280	
Ri	780	

The equivalent input noise can be expressed as:

$$E_{ni}^2 \cong E_{ns}^2 + E_n^2\left(\frac{R_S + R_D}{R_D}\right)^2 + I_n^2\left(R_S - jX_C\right)^2$$

$$+\left[\frac{E_A^2}{1+\left(\omega R_A C_B\right)^2} + \frac{E_B^2}{1+\left(\omega R_B C_B\right)^2} + E_D^2\right]\frac{R_S^2}{R_D^2} + \frac{E_E^2}{1+\left(\omega R_E C_E\right)^2} + \left(\frac{E_C}{K'_t}\right)^2$$



In addition to the known terms, we have now a new term in square parenthesis due to the base bias network. The parenthesis is weighted with the R_S/R_D ratio.

The DC-voltage at the base is determined by the relationship between R_A and R_B as follows:

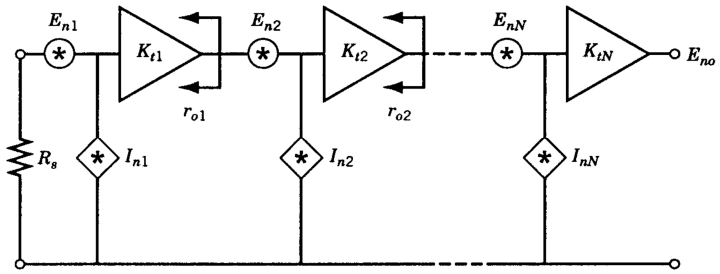
$$V_A = \frac{R_B V_{CC}}{R_A + R_B}$$

The contributing noise from the resistors R_A and R_B should be relatively small. A good starting point is to choose C_B so large that the noise in the relevant frequency range satisfies the inequality:

$$E_{tD}^2 >> \frac{E_{tA}^2}{1+\omega^2 R_A^2 C_B^2} + \frac{E_{tB}^2}{1+\omega^2 R_B^2 C_B^2}$$

Noise in cascaded stages

We have previously studied the noise figure for cascaded amplifiers. We will now look at the equivalent input noise:



The expression for equivalent input noise can be expressed as follows

$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2 + I_{n1}^2 R_S^2 + \frac{E_{n2}^2 + I_{n2}^2 r_{o1}^2}{K_{t1}^2} + \frac{E_{n3}^2 + I_{n3}^2 r_{o2}^2}{K_{t1}^2 K_{t2}^2} + \cdots\cdots$$

YELLOW

Here r_{o1} is the output resistance of stage 1. Similarly for r_{o2}, r_{o3} etc. K_{ti} is as earlier the voltage gain.

As previously if the gain is large enough in the first stage, noise from subsequent stages can be ignored.

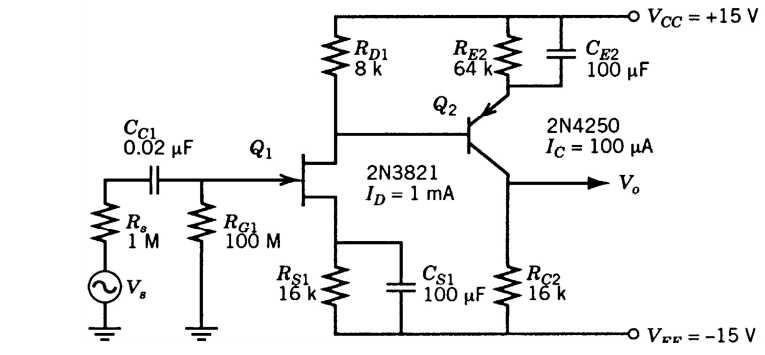
There are three methods one can use for noise analysis of more complex systems such as cascaded network:

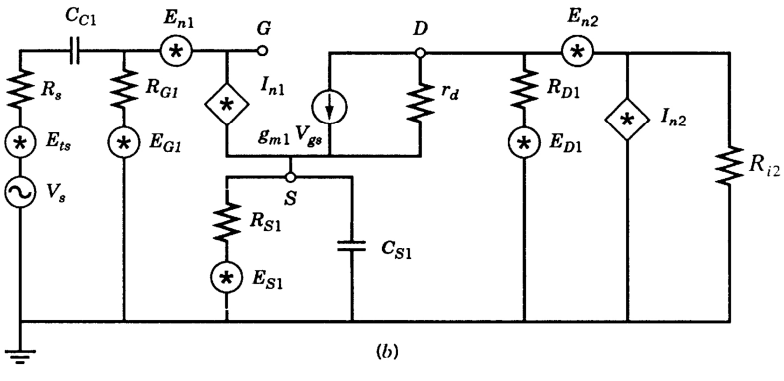
- Manual network analysis (hand calculations),
- use a simulator (like LTspice), or
- measure the system after realisation.

Trick for simulation (and measurement):
If you are unsure of the impact of noise from a source - simulate with this source only and inspect the simulation results at the output.

Common-source --- common-emitter couple

- CS provides high input impedance (compared to CE) and high voltage gain.
- The example uses a JFET but the considerations does also apply to MOSFETs.





	10Hz	10kHz
E_n	8nV	4nV
I_n	7fA	7fA
R_0	1.1MΩ	570kΩ
NF@R_0	0.03dB	0.015dB

The voltage amplification for the CS-stage is:

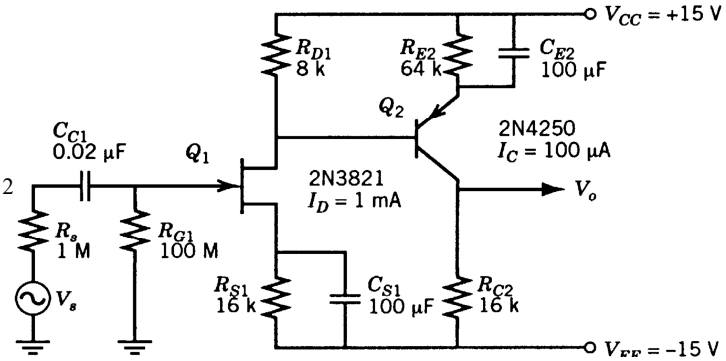
$$K_{t1} \cong -\frac{g_{m1}R_{L1}}{1+g_{m1}Z_{S1}}$$

R_{L1} and Z_{S1} are given by:

$$R_{L1} = R_{D1} \parallel r_d \parallel R_{i2}$$

and

$$Z_{S1} = R_{S1} \parallel -jX_{S1}$$



The total voltage gain is:

$$K_{tc} \cong \frac{g_{m1}R_{L1}\beta R_{C2}}{(1+g_{m1}Z_{S1})(r_{x2}+r_{\pi 2})}$$

When $r_{\pi 2} \gg R_{D1}$ and $R_{C2} \gg r_{o2}$ we have that:

$$K_{tc} \cong \frac{g_{m1}R_{D1}R_{C2}}{r_{e2}}$$

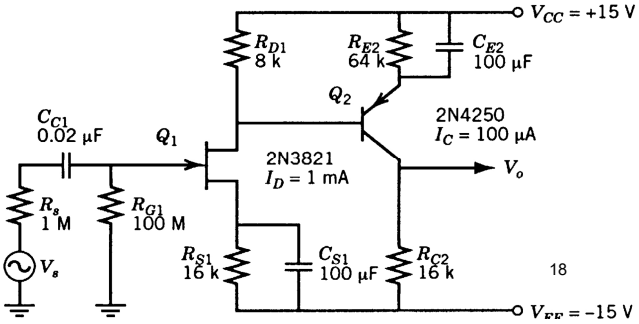
To reduce the E_{n1}-noise contribution from the FET we may consider increasing I_{D1}. But this requires a smaller R_{D1} which means less total gain.

The expression for the equivalent input noise for this circuit is:

$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2\left(\frac{R_{G1}+R_S}{R_{G1}}\right)^2 + I_{n1}^2(R_S - jX_{C1})^2 + \frac{E_{G1}^2R_S^2}{R_{G1}^2}$$

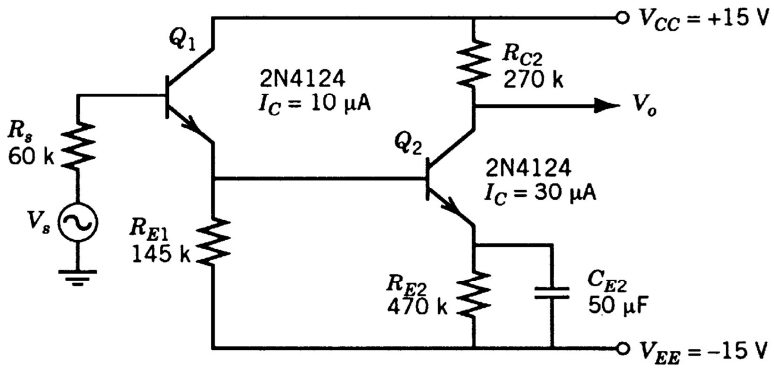
$$+\frac{E_{S1}^2}{1+(\omega R_{S1}C_{S1})^2} + \frac{1}{K_{t1}^2}\left(E_{D1}^2 + E_{n2}^2 + I_{n2}^2R_{D1}^2\right) + \frac{E_{C2}^2}{K_{tc}^2}$$

- R_{G1} must be large compared to R_S
- C_{C1} must be large compared to R_S
- C_{S1} must be sufficient large
- K_{t1} should be large and
- K_{tc} should be large.



Common-collector --- Common-emitter

CC-CE has only a little larger *En* than a pure CE stage but can offer higher input impedance.



First stage has a gain of approx. 1. The total gain is:

$$K_{tc} = -\frac{\beta_1\beta_2 R_{L1} R_{C2}}{\left(R_S + r_{x1} + r_{\pi 1} + \beta_1 R_{L1}\right)\left(r_{x2} + r_{\pi 2} + \beta_2 Z_{E2}\right)}$$

Where

$$R_{L1} = R_{E1} \,||\, \left(r_{x2} + r_{\pi 2} + \beta_2 Z_{E2}\right)$$

The expression for K_{tc} can be simplified when $\beta_1 R_{L1} \gg (R_S + r_{x1} + r_{\pi 1})$ and $r_{\pi 2} \gg r_{x2} + \beta_2 Z_{E2}$:

$$K_{tc} \cong -\frac{R_{C2}}{r_{e2}}$$

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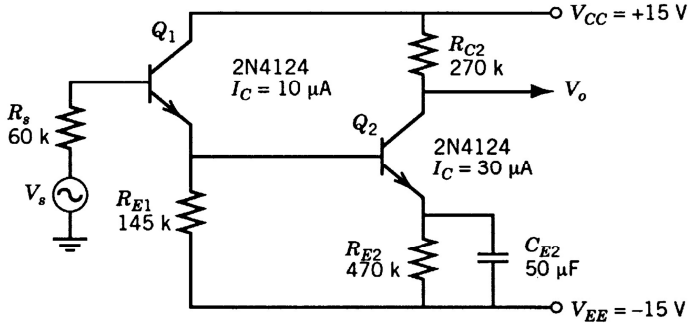
Equivalent input noise is:

$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2 + I_{n1}^2 R_S^2 + \frac{E_{n2}^2}{K_{t1}^2} + \left(\frac{I_{n2} R_{E1}}{K'_{t1}}\right)^2 + \left(\frac{E_{E1}}{K'_{t1}}\right)^2 + \frac{E_{C2}^2}{K_{tc}^2}$$

K'_{t1} is the gain in the first CC stage with R_{E1} as load.

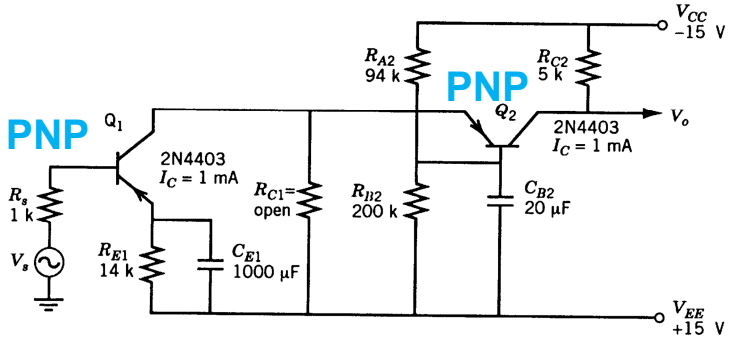
$$K'_{t1} = \frac{\beta_1 R_{E1}}{R_S + r_{x1} + r_{\pi 1}} \cong \frac{R_{E1}}{r_{e1} + R_S/\beta_1}$$

- In CC and CD should the emitter/source resistance be large.



Common-Emitter --- Common-Base

CE-CB has low input capacitance and high output impedance. Due to the low input resistance of the second stage the voltage gain of the first stage will be low. This reduces the high frequency feedback (Miller effect) through $C\mu$ as discussed before. The input capacitance is thus much less than for a regular CE step.

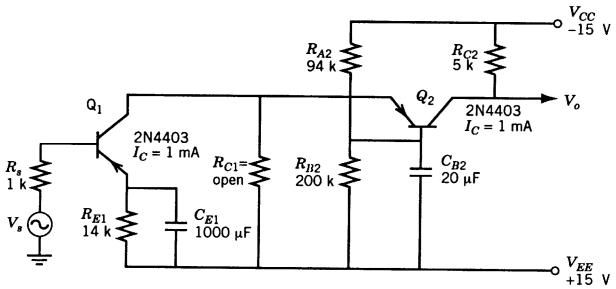


Q1 provides power amplification but not voltage gain (i.e. Q1 provides a current gain.) Q2 provides a large voltage gain.
RC1 is used to provide extra collector current to Q2 when there is a need for large gain-bandwidth.

The total power gain can be expressed as:

$$K_{tc=} = -\frac{\beta_1 R_{L1}}{(r_{x1}+r_{\pi 1}+R_S+\beta_1 Z_{E1})}\frac{\beta_2 R_{C2}}{(r_{\pi 2}+r_{x2}+Z_{B2})} =$$

$$-\frac{\beta_1\beta_2 R_{L1}R_{C2}}{(r_{x1}+r_{\pi 1}+R_S+\beta_1 Z_{E1})(r_{\pi 2}+r_{x2}+Z_{B2})}$$



Where

$$R_{L1} = R_{C1} \parallel \frac{r_{x2}+r_{\pi 1}+Z_{B2}}{\beta_2} \cong r_{e2}$$

When $R_S=0$ and $R_{C1} \gg r_\pi/\beta_2$ we can simplify K_{tc} to:

$$K_{tc} \cong -\frac{R_{C2}}{r_{e1}}$$

The equivalent input noise is:

$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2 + I_{n1}^2 R_S^2 + \frac{1}{K_{t1}^2}\left[E_{C1}^2 + E_{n2}^2 + I_{n2}^2 (R_{L1}+Z_{B2})^2\right]$$

$$+\frac{E_{A2}^2}{K_{t1}^2\left[1+(\omega C_{B2}R_{A2})^2\right]}+\frac{E_{B2}^2}{K_{t1}^2\left[1+(\omega C_{B2}R_{B2})^2\right]}+\frac{E_{C2}^2}{K_{tc}^2}$$

	CE-3pow		CE-2pow		CS-CE		CC-CE		CE-CB	
	10Hz	10kHz	10Hz	10kHz	10Hz	10kHz	10Hz	10kHz	10Hz	10kHz
En	2nV	2nV	4.5nV	4.5nV	8nV	4nV	6nV	5.8nV	1.6nV	1.4nV
In	2pA	0.3pA	0.3pA	0.1pA	7fA	7fA	0.3pA	0.1pA	20pA	1.5pA
R0	1kΩ	6.7kΩ	15kΩ	45kΩ	1.1MΩ	570kΩ	20kΩ	58kΩ	80Ω	930Ω
NF@R0	1.8dB	0.3dB	0.68dB	0.35dB			0.9dB	0.3dB	7dB	1dB

(Ignore colour)

Integrated BJT cascade amplifier

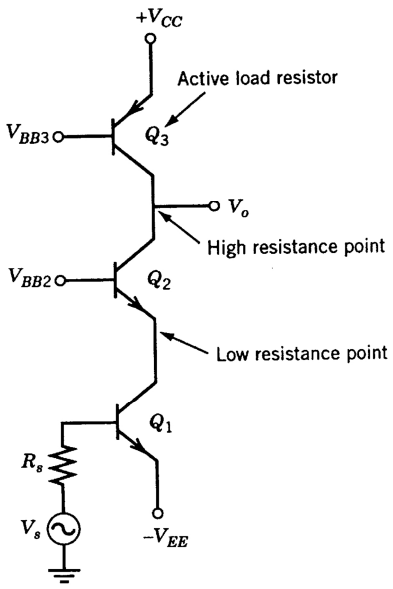
Here Q1 acts as a CE-stage and Q2 as a CB-stage. Q3 is load. The total voltage gain is:

$$K_{tc} \cong -\frac{r_{o3}}{r_{e1}}$$

The equivalent input noise is:

$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2 + I_{n1}^2 R_S^2 + \frac{1}{K_{t1}^2}\left[E_{n2}^2 + I_{n2}^2 (r_{e2} + Z_{B2})^2\right] + \frac{E_{o3}^2}{K_{tc}^2}$$

Here is $K_{t1}=r_{e2}/r_{e1}$. Since the collector currents are equal is $K_{t1}=1$. Z_{B2} is the impedance to V_{BB2} (should be low). Since r_{e2} also is small the contribution from I_{n2} should also be ignorable.



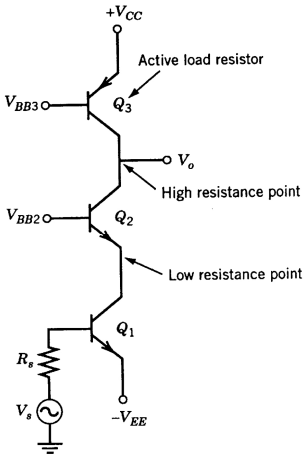
The noise voltage from Q3 at the output is:

$$E_{o3} = E_{n3} K_{t3}$$

The gain in Q3 is:

$$K_{t3} = \frac{r_{o2}}{r_{e3}} \cong K_{tc}$$

With these simplifications and assuming all transistors are equal the expression for the equivalent input noise is reduced to:



$$E_{ni}^2 = E_{ns}^2 + E_{n1}^2 + I_{n1}^2 R_S^2 + E_{n2}^2 + E_{n3}^2$$
$$\cong E_{ns}^2 + 3E_n^2 + I_{n1}^2 R_S^2$$

YELLOW

Differential amplifiers – two sources

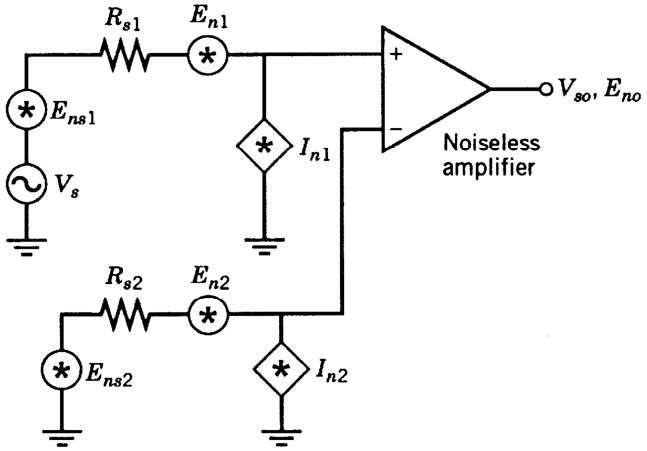
The two input signals V_1 and V_2 can be defined relative to a common value (common-mode) V_C, and a difference value V_D.

$$V_C = \frac{V_1 + V_2}{2} \quad \text{and} \quad V_D = V_1 - V_2$$

We will then have:

$$V_1 = V_C + \frac{V_D}{2} \quad \text{and} \quad V_2 = V_C - \frac{V_D}{2}$$

The figure shows the noise schematic.



The equivalent input noise is:

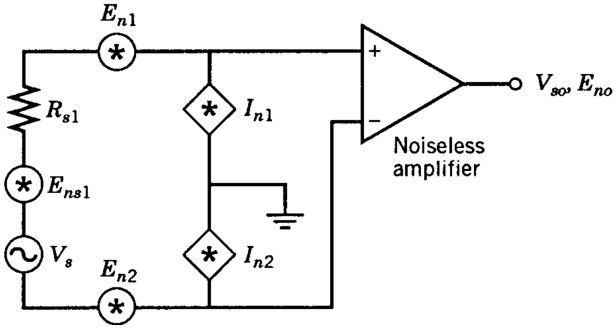
$$E_{ni}^2 = E_{ns1}^2 + E_{ns2}^2 + E_{n1}^2 + E_{n2}^2 + I_{n1}^2 R_{S1}^2 + I_{n2}^2 R_{S2}^2$$

Differential connection – one source

We assume that the positive and negative input has the same noise characteristics and adds together the En and In-values for the amplifier.

$$E_{nT}^2 = E_{n1}^2 + E_{n2}^2 = 2E_{n1}^2$$

$$I_{nT}^2 R_S^2 = I_{n1}^2 \left(\frac{R_S}{2}\right)^2 + I_{n2}^2 \left(\frac{R_S}{2}\right)^2 = \frac{I_{n1}^2}{2} R_S^2$$



When we add together with the noise from the source resistance, we obtain the equivalent input noise:

$$E_{ni}^2 = E_{ns}^2 + 2E_{n1}^2 + \frac{I_{n1}^2 R_S^2}{2}$$

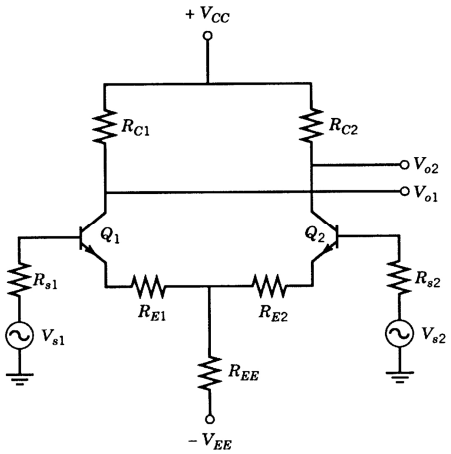
Noise model for the differential amplifier

Example of differential stage:

a)

Voltage gain of differential signal:

$$K_{dm} = \frac{V_{o2} - V_{o1}}{V_{s2} - V_{s1}} = \frac{-2R_C}{\frac{1}{g_m} + R_E + \frac{R_S}{\beta}}$$

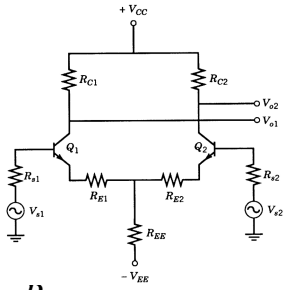


Here is $g_m = 1/r_e$ for each of the transistors.

Assuming identical transistors and $R_{C1}=R_{C2}=R_C$, $R_{E1}=R_{E2}=R_E$ and $R_{S1}=R_{S2}=R_S$.

For the typical cases where $R_E=0$ and $R_S \ll r_\pi$ we can simplify K_{dm} to:

$$K_{dm} \cong \frac{-2R_C}{r_e}$$



b)

Gain for the common mode voltage signal:

$$K_{cm} = \frac{V_{o2} + V_{o1}}{V_{s2} + V_{s1}} = \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_S}{\beta} + 2R_{EE}}$$

When R_{EE} is large we get:

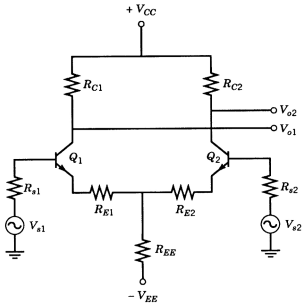
$$K_{cm} \cong \frac{-R_C}{2R_{EE}}$$

c)

Differential voltage gain between outputs with common input signal:

$$K_{dc} = \frac{V_{o2} - V_{o1}}{2V_S} = \frac{R_{C1}\left(\frac{R_{S2}}{\beta_2} + \frac{1}{g_{m2}} + R_{E2}\right) - R_{C2}\left(\frac{R_{S1}}{\beta_1} + \frac{1}{g_{m1}} + R_{E1}\right)}{2R_{EE}\left(\frac{R_{S2}}{\beta_2} + \frac{1}{g_{m2}} + R_{E2} + \frac{R_{S1}}{\beta_1} + \frac{1}{g_{m1}} + R_{E1}\right)}$$

Ideally if the inputs were completely symmetrical K_{dc} should be 0. When this is not the case one can reduce K_{dc} say by increasing R_{EE}.



Eni:

$$E_{ni}^2 = E_{S1}^2 + E_{S2}^2 + E_{n1}^2 + E_{n2}^2 + I_{n1}^2 R_{S1}^2 + I_{n2}^2 R_{S2}^2$$
$$+ E_{E1}^2 + E_{E2}^2 + \frac{E_{C1}^2 + E_{C2}^2}{K_{dm}^2} + \frac{E_{EE}^2 + E_{VEE}^2 + E_{VCC}^2}{K_{dc}^2}$$

Here is E_{VEE} and E_{VCC} noise on the voltage supplies.

Integrated BJT differential amplifier

It can be relatively large variation in process parameters for integrated circuits from production to production. However between the elements on the same circuit the variation can be made very small. This is exploited by using design strategies based more on the symmetry between the elements than on their actual values.

In integrated circuits the common-mode noise rejection is improved. On the other hand, integrated circuits require compromises that may give more noise than when optimizing a process for a single isolated component. Examples of these compromises are:

- long diffusion insulations,
- active loads, and
- power sources.

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University of Oslo

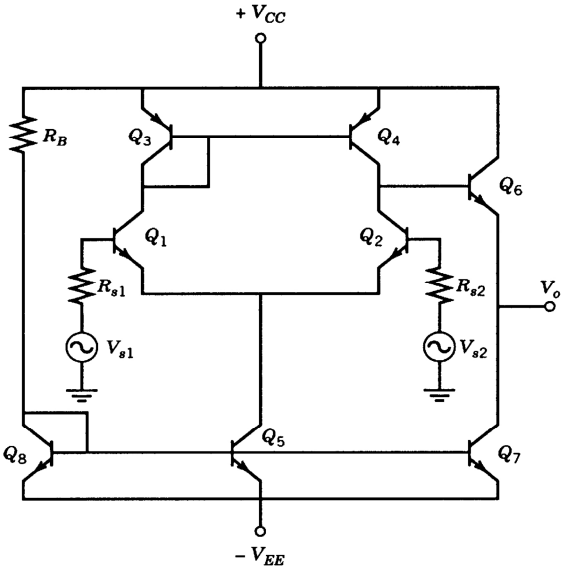
The figure shows the integrated version of the differential amplifier we studied previously.

Equivalent input noise:

$$E_{ni}^2 = E_{s1}^2 + E_{s2}^2 + E_{n1}^2 + E_{n2}^2 + I_{n1}^2 R_{s1}^2 + I_{n2}^2 R_{s2}^2 + E_{n3}^2 + E_{n4}^2 + \frac{E_{n5}^2 + E_{VEE}^2 + E_{VCC}^2}{K_{dc}^2}$$

Since common-mode rejection is high and all active circuits have approximately the same geometry and noise mechanisms, E_{ni} will be reduced to:

$$E_{ni}^2 = 2E_S^2 + 4E_n^2 + 2I_n^2 R_S^2$$



Parallel amplifier stages

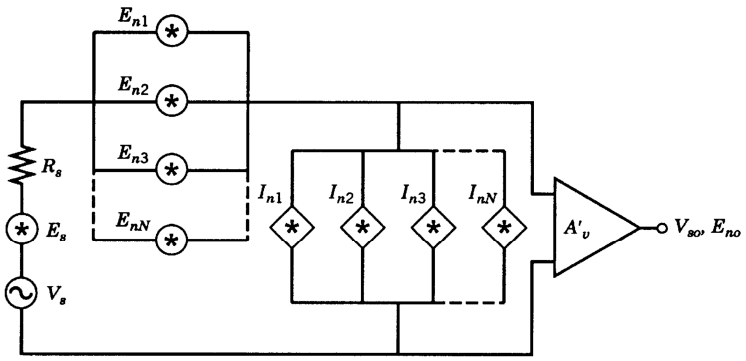
What when several amplifiers are placed in parallel? Schematically, we can draw noise sources as in the figure.

We have: $E'_n = \frac{E_n}{\sqrt{N}}$ and $I'_n = I_n\sqrt{N}$

A new optimal source resistance can be defined as:

$R'_o = \frac{E'_n}{I'_n} = \frac{R_o}{N}$

Gain is given by: $A'_v = NA_v$



A significant contribution to the En -noise in a BJT is the base resistance r_x. The base resistance can be reduced by placing base contacts all the way around the emitter and closest possible to the emitter. In FETs it is determined by the channel resistances, and by g_m. Low resistance and high g_m can be achieved by having a large W/L ratio. Through parallelising, both the $C'\mu$ and the Miller effect is increased.