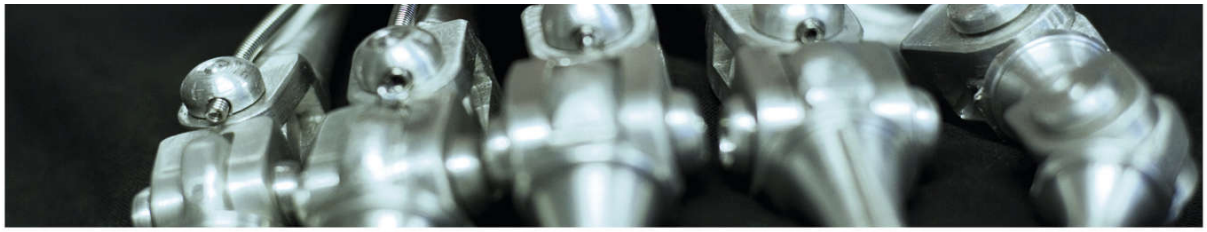

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IN5230
Electronic noise – estimates and countermeasures

Lecture no 9 (Mot 6)
Noise in field effect transistors

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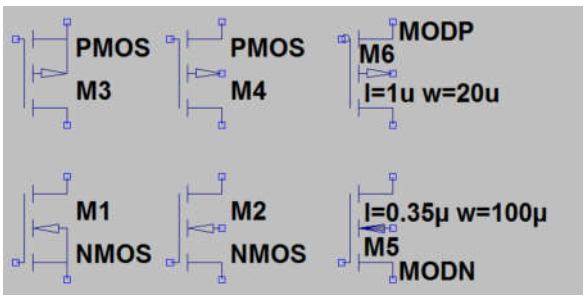
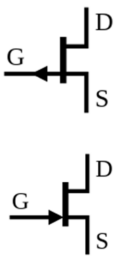
Two types of field effect transistors:
• MOSFET: Capacitive control of the channel
• JFET: Variation of the width of a reversed biased depletion zone that determines the width of the channel. GaAs FETs have a similar behaviour.



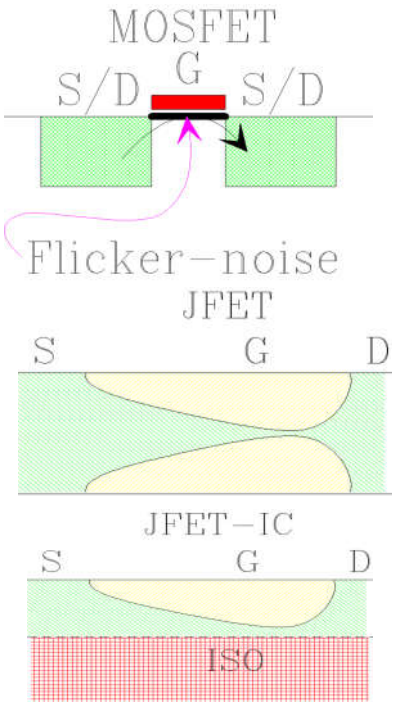


MOS and JFET

RED: All figures and text

FET (Field Effect Transistor) implies that a channel is created/throttled as a result of the voltage on a control terminal. There are essentially two ways to do this:

- MOS: The gate sets up a field that creates a channel on the other side of an insulator
- JFET (Junction FET): The voltage on the gate controls the width of the depletion zone which opens/closes the channel. JFETs are available in two variants
  - Discrete components: the gate is present on both sides of the channel.
  - ASIC: the gate is on one side while it is an insulator on the other side of the channel.



Noise Mechanisms

RED: Figure

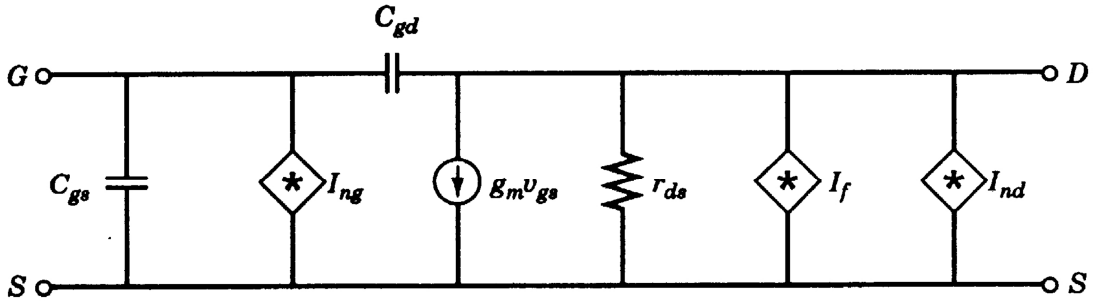


Figure 6-1 Small-signal noise equivalent circuit for a FET.

The figure shows a simple FET-model extended with noise models.

Elements of a typical model:
C_{gs}, C_{gd}: Capacitance between gate and source and between gate and drain.
$g_m V_{gs}$: Current between source and drain.
R_{DS}: Resistance in the channel between drain and source.

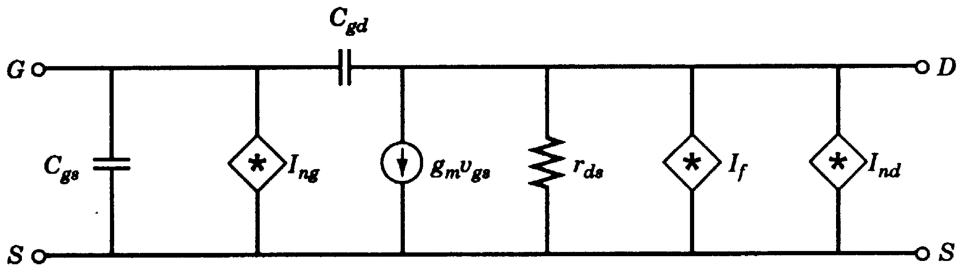


Figure 6-1 Small-signal noise equivalent circuit for a FET.

Noise models:
Gate:

- Shot-Noise in leakage current through the gate (especially JFET and newer small linewidth CMOS) and
- thermal fluctuations from the drain node, which affects the gate node

Drain:

- I_{nd}: Thermal noise in the channel.
- I_f: Flicker noise in the channel

The gate and I_{nd} thermal noises are both due to thermal noise in the channel and they are partially correlated at higher frequencies.

En-In representation of noise

RED: Figure

The figure show the typical trends for *En* and *In* in a FET. *En* is flat at high frequencies but grows at lower frequencies due to flicker noise. *In* is flat at low frequencies but grows linearly with frequency above a corner frequency.

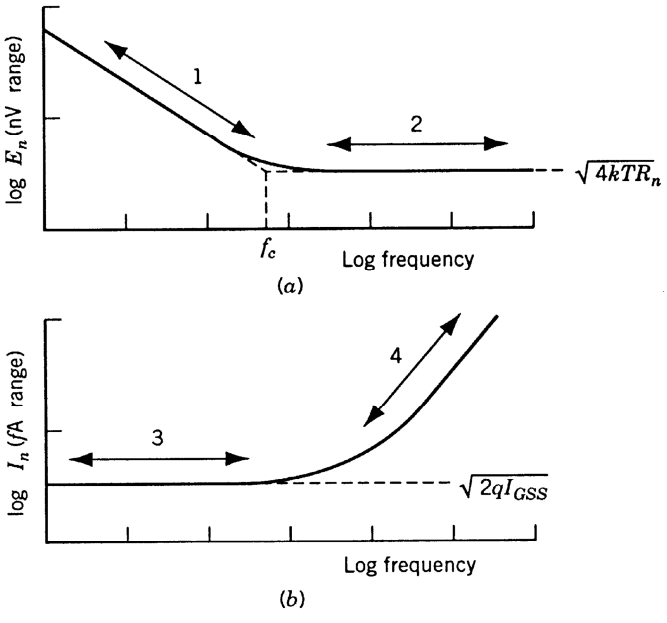


Figure 6-2 Typical noise behavior of a FET.

Simple FET model

RED: Figure

First, we ignore the noise and consider a standard MOSFET.

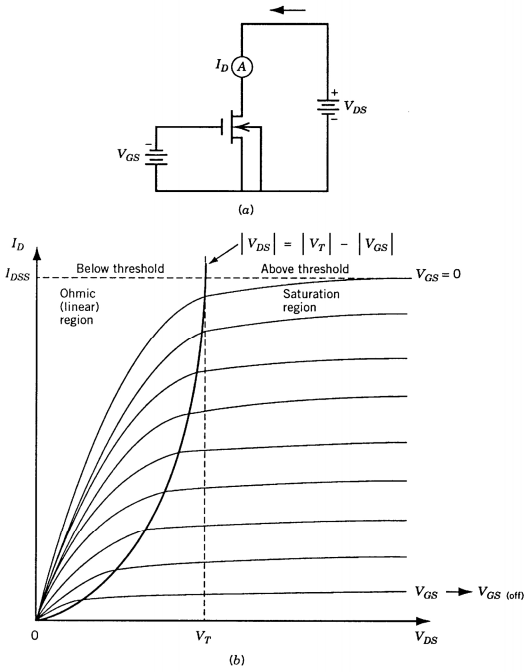


Figure 6-7 Determination of *n*-channel MOSFET *V–I* characteristics: (*a*) test circuit and (*b*) output characteristics.

The transistor can be in cut-off, linear region or in saturation. In the linear region the current *Ids* has a strong dependence on *Vds*, while in saturation the dependence is weaker. The linear range is often named the resistive or ohmic region.

In saturation *Ids* can be expressed as follows:

$$I_D = K_p \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

Here λ modulates the dependence on the channel length, V_T is the threshold voltage, W is the channel width, while L is the channel length. The transconductance value K_P can be expressed as:

$$K_p = \frac{\mu_0 C_{ox}}{2}$$

Here is μ_0 the mobility of the channel and Cox the capacitance over the gate oxide.

Some examples of sizes from the book:

	N-channel	p-channel	Denomination
K_P	41.8	15.5	μA/V²
V_T	0.79	-0.93	V
λ	0.01	0.01	1/V

Key parameters are transconductance ...

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{Q-point} = 2K_p\left(\frac{W}{L}\right)(V_{GS} - V_T)(1 + \lambda V_{DS}) = \frac{2I_D}{V_{GS} - V_T}$$

.. and output conductance ...

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \left.\frac{1}{r_{ds}}\right|_{Q-point} = \lambda K_p\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS}) = \lambda I_D$$

The capacitances Cgd and Cgs.
These capacitances will vary depending on the region:

	Region		
	Cut-off	Linear	Saturation
Cgd	$C_{OX}WL_D$	$C_{OX}WL_D$ + (1/2) WLC_{OX}	$C_{OX}WL_D$
Cgs	$C_{OX}WL_D$	$C_{OX}WL_D$ + (1/2) WLC_{OX}	$C_{OX}WL_D$ + (2/3) WLC_{OX}

Cox may be defined as:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{SiO_2}}{t_{ox}}$$

... and stated i fF/um ²

Ind in short length devices

We learnt in the previous that the thermal noise in the channels could be expressed as: $I_{nd}^2 = \frac{8kTg_m}{3}$

However in newer technologies with smaller transistor lengths it is a little more complicated and more correct will be:

$$I_{nd}^2 = 4kT\gamma g_m$$

where γ is 2/3 for long L and increasing for short L. An example measurement shows γ=2.5 for L=0.25µm.

When Vds=0 the expression is $I_{nd}^2 = 4kT\gamma g_{ds}$ NB! g_{ds}!
where $g_{ds} = 1/R_{on}$ for short L and $g_{ds} = g_m$ for long L in saturation.

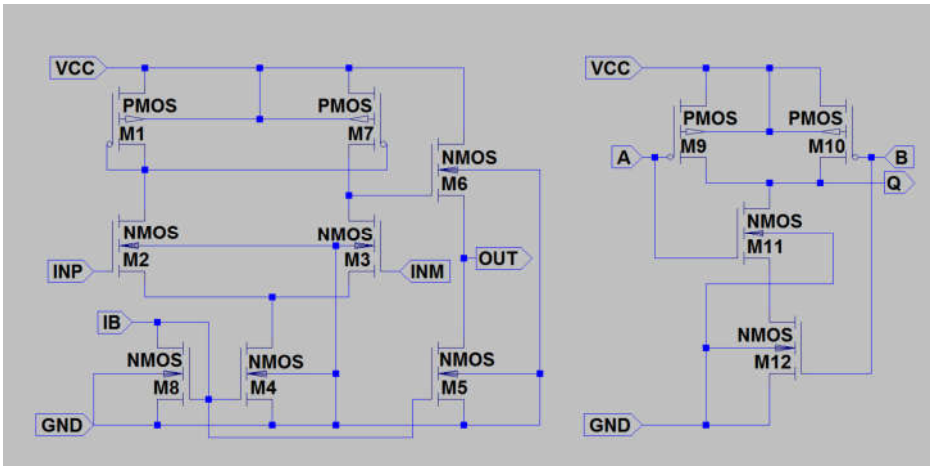
Ref: Razavi *Design of Analog CMOS Integrated Circuits*

MOS noise sources

- Flicker noise in channel
- Thermal noise in channel
- Shot-noise in leakage channel-gate
- Coupled thermal noise at gate
- Thermal noise in gate
- Thermal noise in bulk
- Thermal noise in source
- Thermal noise in drain
- Shot-noise drain-bulk
- Shot-noise source-bulk
- (Coupling noise to bulk)

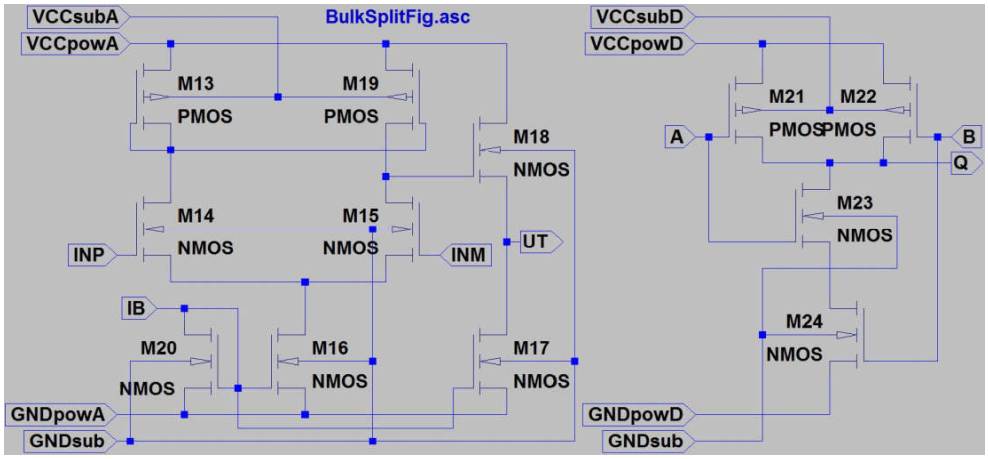
CMOS Standard bulk connection

- The schematics shows an amplifier and a digital NAND gate with standard sub connections.
- NMOS bulk terminals are connected to the lowest potential, while PMOS bulk are connected to the highest.



CMOS low noise bulk connection

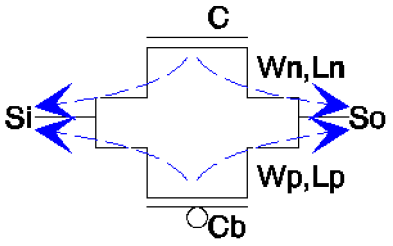
- For low noise the NMOS bulk and PMOS bulk are split from the power lines.

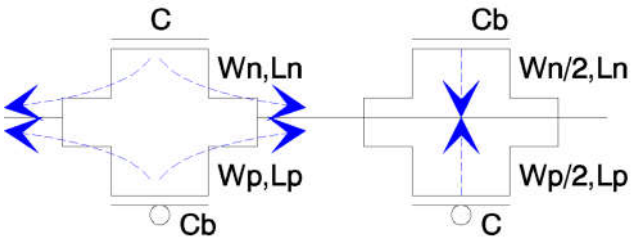


- Little current will pass through the bulk terminal. However the transistor is sensitive to noise on this terminal.
- By splitting the power wires we reduce the noise on the sensitive bulk terminal. This will prevent digital source/drain noise to reach the analog bulk terminal.

CMOS switch charge injection

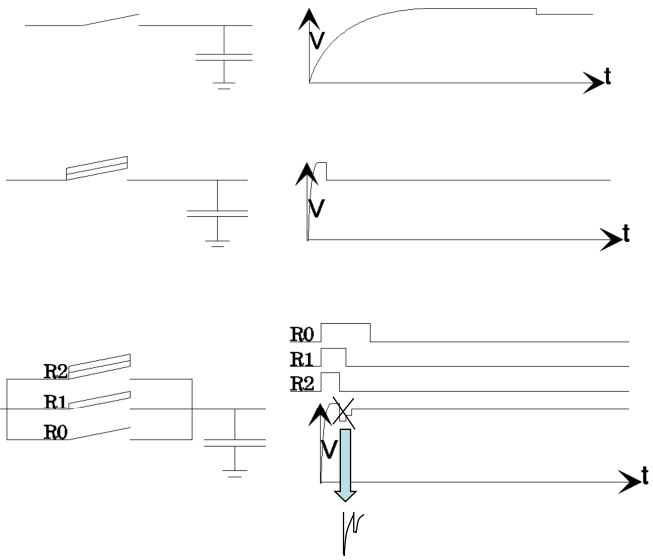
- A conducting CMOS transistor keeps some charge in the channel
- When turned off this charge is released through the source/drain and generates an (unpredictable) voltage change
- A proposal is to add a pair of half-sized "opposite" dummy transistors. However this solution requires impedance symmetry.





CMOS switch charge injection

- The injected charge is a function of transistor size and voltage level
- Small transistor gives slow response but small step.
- Large transistors gives fast response but large step.
- Parallel, different sized transistors with different pulse termination times may give both fast response and minimum step.

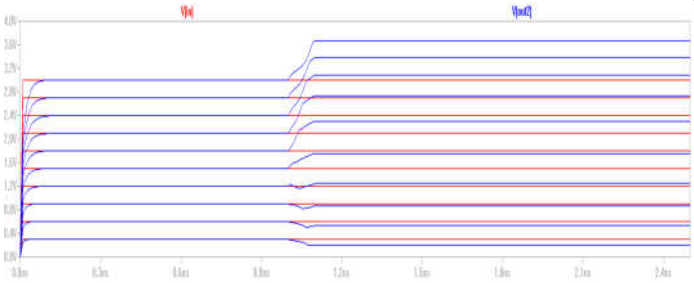


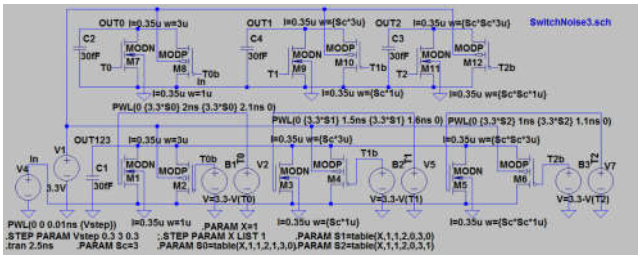
CMOS switch charge injection

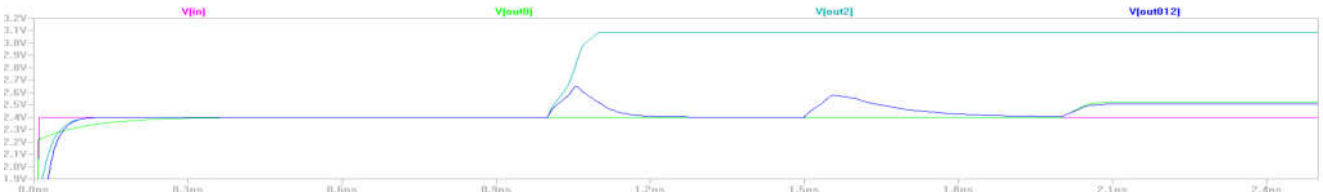
- Sharp input pulse at 0ns, all switches closed (conducting)
- R2 (large) opens at 1ns
- R1 (medium) opens at 1.5ns
- R0 (small) opens at 2ns
- OUT0 : R0
- OUT2 : R2
- OUT012: R0+R1+R2

Observations:

- Generated voltage step depends on signal level
- OUT0: Slow but minimum step
- OUT2: Fast but large step
- OUT012: Fast and minimum step







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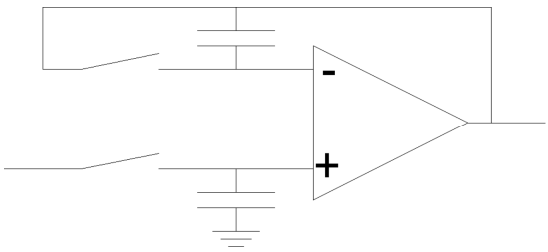
Sampler with switch charge cancelation

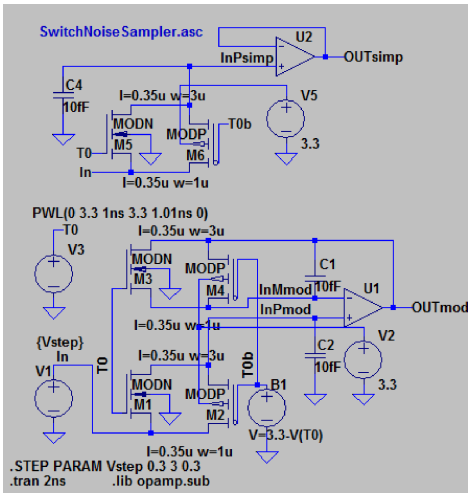
- A differential sampler with same sized switches on both inputs may almost eliminate the influence by the charge injection.
- At sampling both transistors have the same potential and generates similar charge on both inputs.

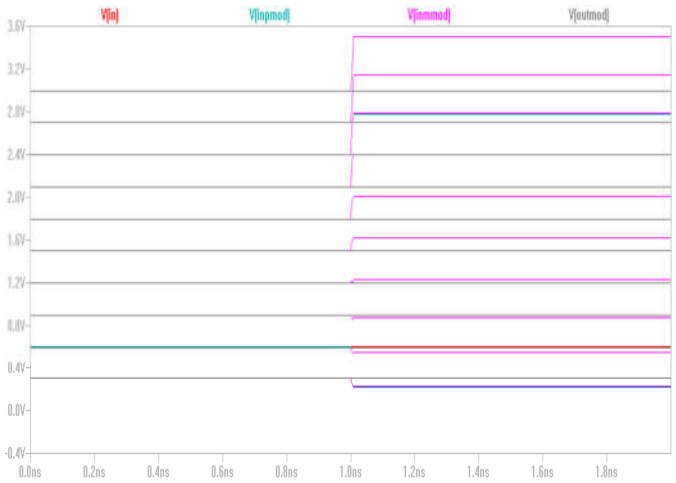
RED: Figure

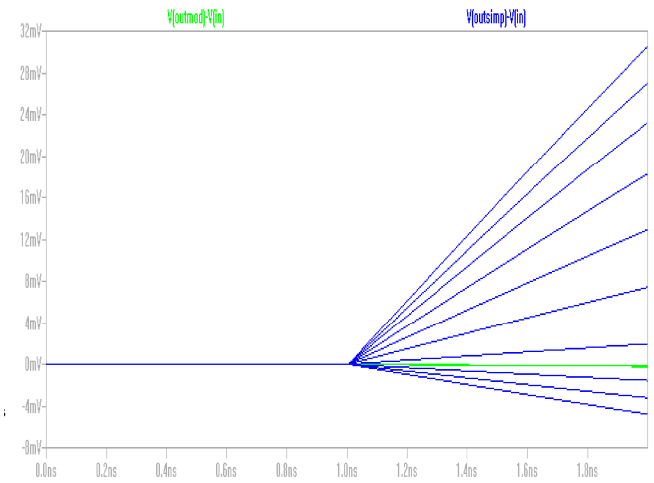


Sampler with injection compensation

- OUTsimp: standard
- OUTmod: with charge injection compensation
- The inputs experience a very equal step resulting in a stable output







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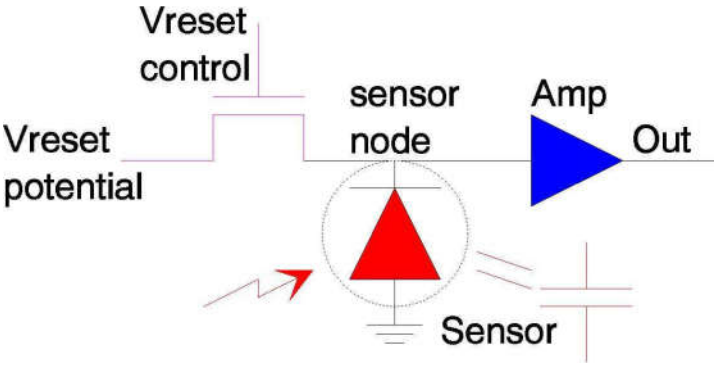
Correlated double sampling

YELLOW: Figure

- Photo diodes (CMOS pixel cells) consist of a reversed biased diode operating as a capacitor.

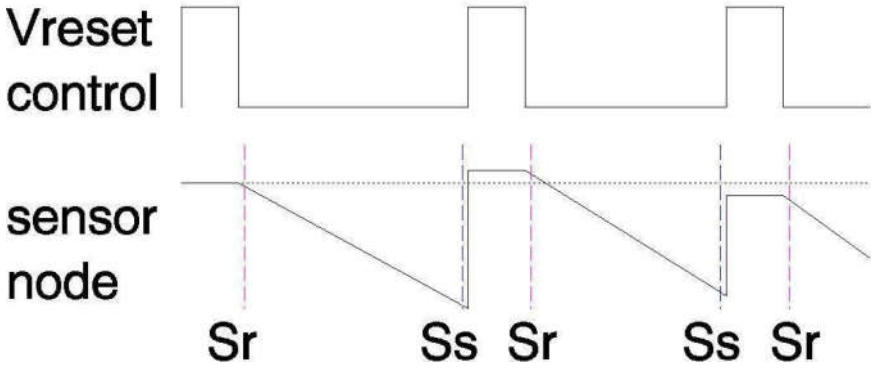


- A switched reset potential is placed on the sensor node. Accumulated electrons generated from light photons reduces the sensor node potential.

Correlated double sampling

YELLOW: Figure

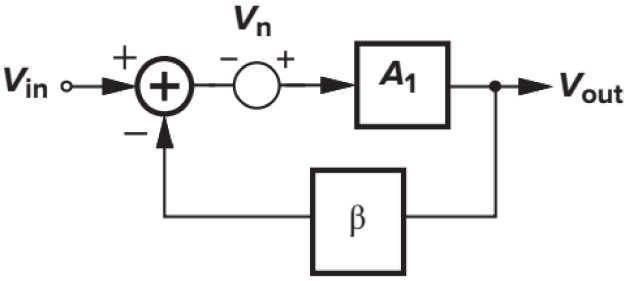
Due to charge injection and thermal noise the sensor node will be resat to unpredictable levels.



With correlated double sampling the value is measured both immediately after reset and before next reset. The difference is used.

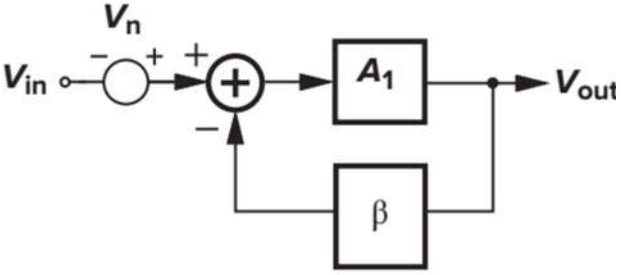
Effect of Feedback on Noise 8.3

- We represent the noise in the amplifier by Vn. We simplify and assume that the feedback is noiseless.
- The resulting expression shows that Vn can be placed in the same position as Vin and that the feedback does not improve the noise performance. If the feedback has noise generating elements the total noise will be worse.
- Note that the output of interest is the same as the quantity sensed by the feedback network.



$$(V_{in} - \beta V_{out} + V_n)A_1 = V_{out}$$

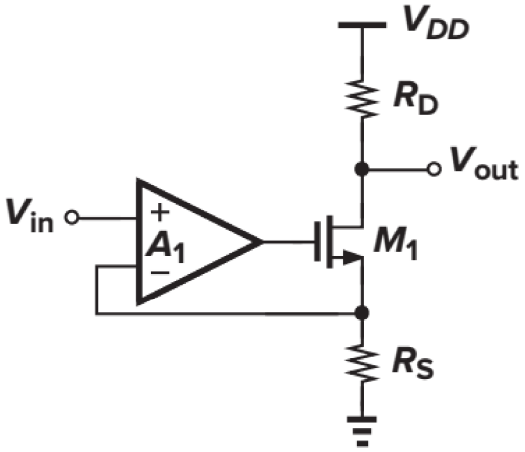
$$V_{out} = (V_{in} + V_n)\frac{A_1}{1 + \beta A_1}$$



Effect of Feedback on Noise 8.3

- When the output and feedback points are different, input referred noise for open-loop and closed loop may also be different.
- In this schematice this is the case and we simplify and calculate the noise for R_D only.
- The closed loop voltage gain is:

$$-A_1 g_m R_D / [1 + (1 + A_1) g_m R_S]$$



and hence the input referred noise:

$$\left|V_{n,in,closed}\right| = \frac{|V_{n,RD}|}{A_1 R_D}\left[\frac{1}{g_m} + (1 + A_1) R_S\right]$$

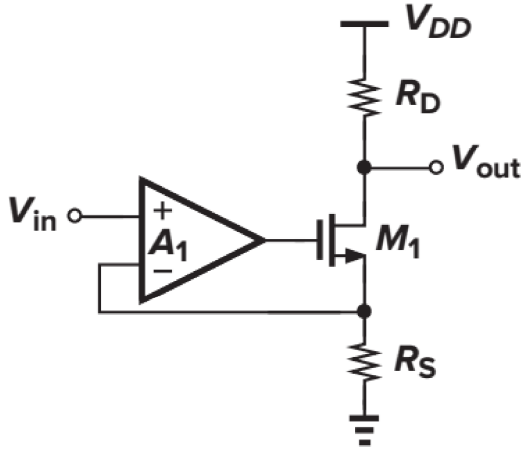
While the open-loop input referred noise is:

$$\left|V_{n,in,open}\right| = \frac{|V_{n,RD}|}{A_1 R_D}\left[\frac{1}{g_m} + R_S\right]$$

Effect of Feedback on Noise 8.3

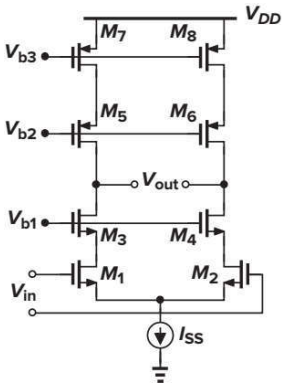
$$\left|V_{n,in,closed}\right| = \frac{|V_{n,RD}|}{A_1 R_D}\left[\frac{1}{g_m} + (1 + A_1) R_S\right]$$

$$\left|V_{n,in,open}\right| = \frac{|V_{n,RD}|}{A_1 R_D}\left[\frac{1}{g_m} + R_S\right]$$



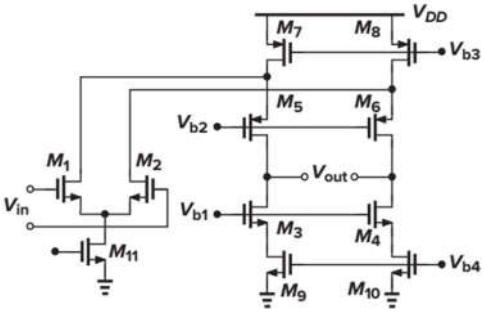
- If $A_1 \to \infty$,
- We have that $|V_{n,in,closed}| \to |V_{n,RD}| R_S / R_D$
- while $|V_{n,in,open}| \to 0$

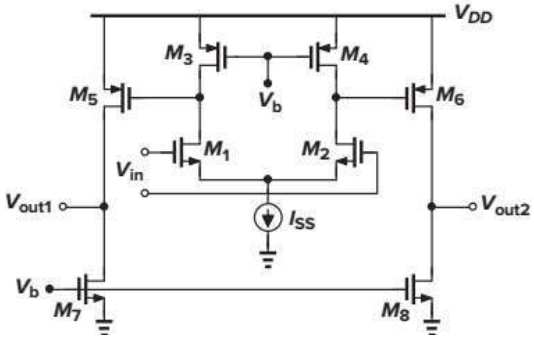
Noise in Op Amps 9.12



- How to analyse for noise in more complex amplifier structures?
- ⇒ Find which gate voltages that influence most on the output!
- ⇒ Analyse manually or by simulation!

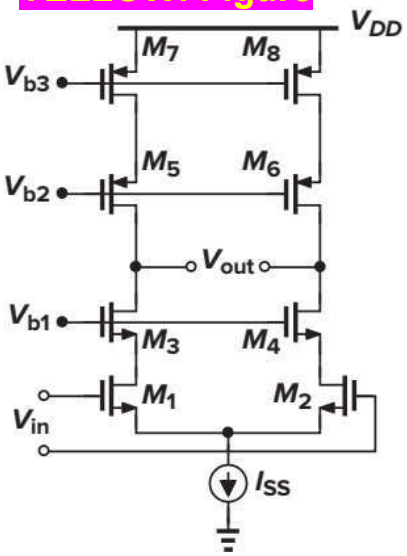
- Upper right: Telescopic
- Lower left: Folded cascode
- Lower right: Two-stage opamp





Noise in Op Amps 9.12

YELLOW: Figure



Telescopic

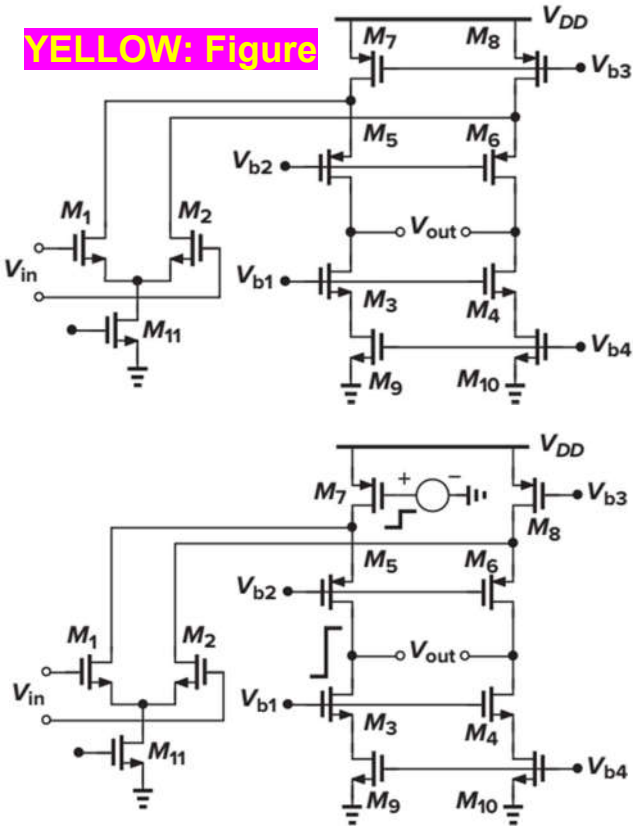
- M7-M8 give a coarse regulation of current while M5-M6 gives fine tuning i.e. M7-M8 has larger influence
- M1-M2 is the signal inputs, obviously more sensitive than M3-M4.
- ⇒ M1-M2 and M7-M8 are the most noise sensitive.

- Resulting expression below:

$$\overline{V_n^2} = 4kT\left(2\frac{\gamma}{g_{m1,2}} + 2\frac{\gamma g_{m7,8}}{g_{m1,2}^2}\right) + 2\frac{K_N}{(WL)_{1,2}C_{ox}f} + 2\frac{K_P}{(WL)_{7,8}C_{ox}f}\frac{g_{m7,8}^2}{g_{m1,2}^2}$$

Noise in Op Amps 9.12

YELLOW: Figure



Folded-cascode

- The gate voltage of M1-M2, M7-M8, M9-M10 will give the largest influence on the output and are hence most noise sensitive. (We test by making a small step on M7 and keep the others fixed etc.)
- We calculate (thermal) noise from M7-M8 and M9-M10 to output.

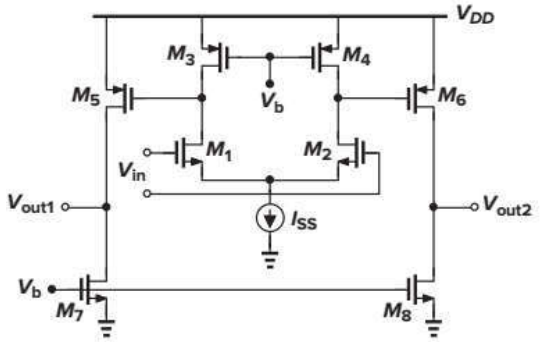
$$\overline{V_{n,out}^2}\big|_{M7,8} = 2\left(4kT\frac{\gamma}{g_{m7,8}}g_{m7,8}^2R_{out}^2\right)$$

$$\overline{V_{n,out}^2}\big|_{M9,10} = 2\left(4kT\frac{\gamma}{g_{m9,10}}g_{m9,10}^2R_{out}^2\right)$$

- Then we add M1-M2 contribution and calculate back to the input Vin

$$\overline{V_{n,int}^2} = 8kT\left(\frac{\gamma}{g_{m1,2}} + \gamma\frac{g_{m7,8}}{g_{m1,2}^2} + \gamma\frac{g_{m9,10}}{g_{m1,2}^2}\right)$$

Noise in Op Amps 9.12



Two-stage opamp

- Gain to Vout1:

$$g_{m1}(r_{O1}\|r_{O3}) \times g_{m5}(r_{O5}\|r_{O7})$$

- Noise from M5-M8 on input

YELLOW: Figure

$$\overline{V_n^2}\big|_{M5-8} = 2\times 4kT\gamma(g_{m5}+g_{m7})(r_{O5}\|r_{O7})^2\frac{1}{g_{m1}^2(r_{O1}\|r_{O3})^2g_{m5}^2(r_{O5}\|r_{O7})^2} = 8kT\gamma\frac{g_{m5}+g_{m7}}{g_{m1}^2g_{m5}^2(r_{O1}\|r_{O3})^2}$$

YELLOW: Equation

- Noise from M1-M4 on input

$$\overline{V_n^2}\big|_{M1-4} = 2\times 4kT\gamma\frac{g_{m1}+g_{m3}}{g_{m1}^2}$$

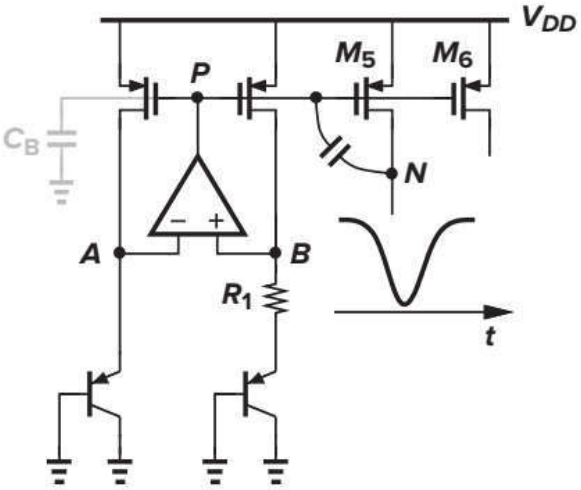
- Total noise on output (???)⇒input

$$\overline{V_{n,tot}^2} = 8kT\gamma\frac{1}{g_{m1}^2}\left[g_{m1}+g_{m3}+\frac{g_{m5}+g_{m7}}{g_{m5}^2(r_{O1}\|r_{O3})^2}\right]$$

???⇒Vn,tot at input

Bandgap - Speed and Noise Issues 12.6

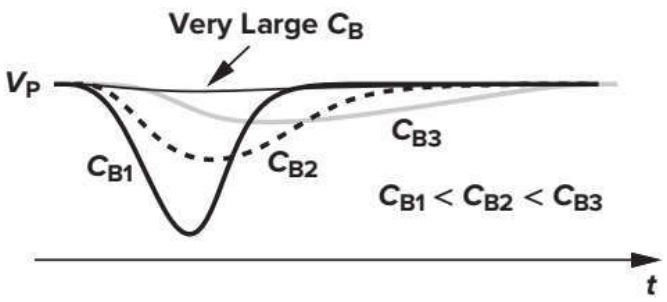
- The bandgap reference generates a stable voltage on P independent of temperature variations. This is used to generate stable currents on M5, M6 etc.
- An unwanted voltage spike on N may be transferred to P and further on to M6 and other parts using the reference.
- In a low power implementation the amplifier will be slow but this makes it less resistant towards noise



YELLOW: Figure

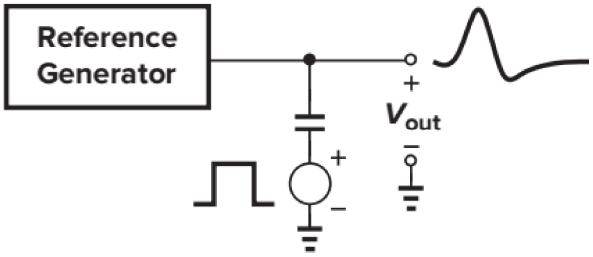
Bandgap - Speed and Noise Issues 12.6

- Using a faster amplifier will reduce the noise but increase the power consumption
- An alternative is to add a capacitor C_B in node P. A large C_B reduces the noise spike but makes it last for a longer time. It also increases the time before the circuit is settled after power on. This is a disadvantage in particular when the reference is normally off and only turned on when it should be used.



Bandgap - Speed and Noise Issues 12.6

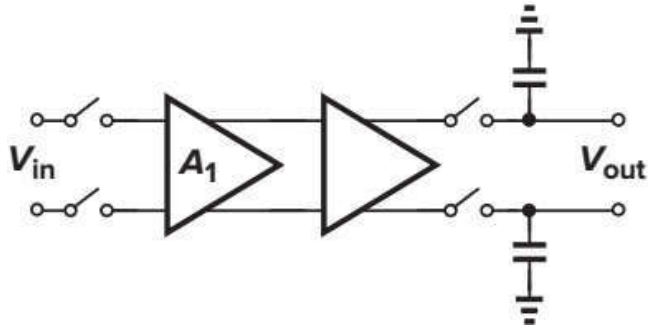
- Whether a fast amplifier or large capacitance (or a combination) should be used will depend on the application.
- The noise resistivity towards this type of noise can be modelled by adding a voltage pulse on a capacitor connected to the generated reference voltage.



RED: Figure

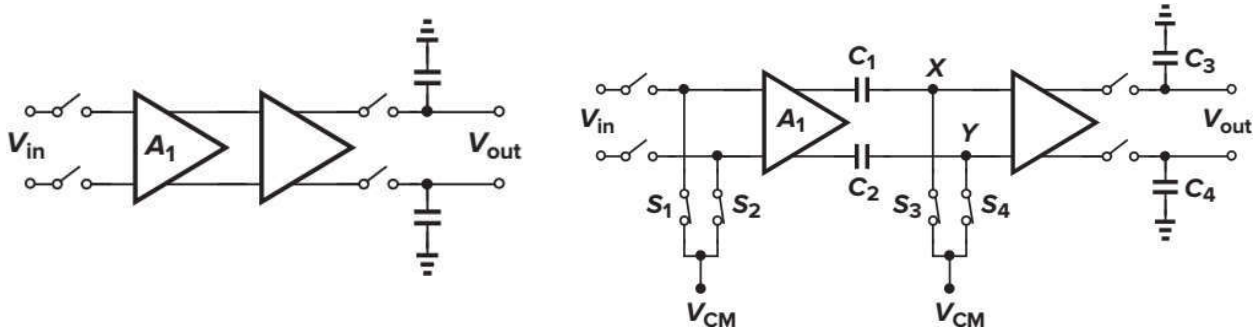
Reduction of Noise by Offset Cancellation 14.2.3

- DC-offset ≈ low frequency
- Periodic cancellation?



- Noise of A1 corrupts V_{in}

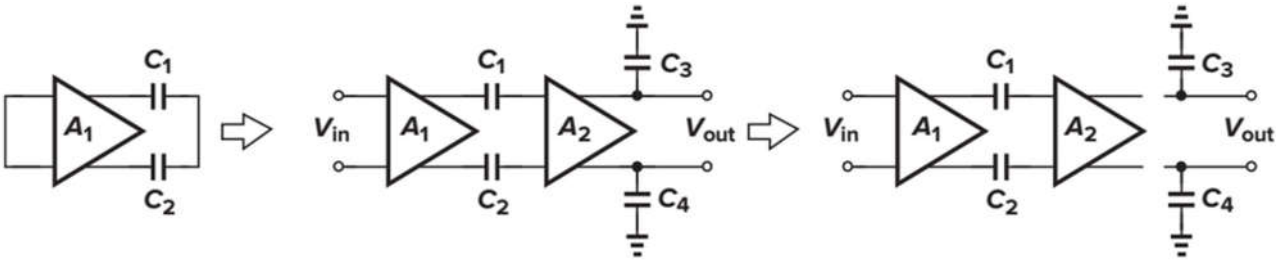
Reduction of Noise by Offset Cancellation 14.2.3



- Offset cancellation before every sampling
- CDS: Correlated Double Sampling
  - (Leads to aliasing of wideband noise)

Reduction of Noise by Offset Cancellation 14.2.3

YELLOW: Figure



1. S1-S4 closed, S5-S8 open: Offset of A_1 stored on C_1 and C_2
2. S1-S4 open, S5-S8 closed: Input sets C_3 and C_4
3. S1-S6 open, S7-S8 closed: C_3 and C_4 keeps sampled value

Reduction of Noise by Offset Cancellation 14.2.3

- $\Delta t = t_2 - t_1 = 10$ ns
- Offset/noise under $1/\Delta t$ is supressed
- Sinus maximum slew rate: $2\pi fA$, maximum voltage change: $\Delta V = 2\pi fA\Delta t$.
- 1MHz: $\Delta V_1/A = 6.3\%$
- 10MHz: $\Delta V_1/A = 63\%$
- Low frequency has not time to change