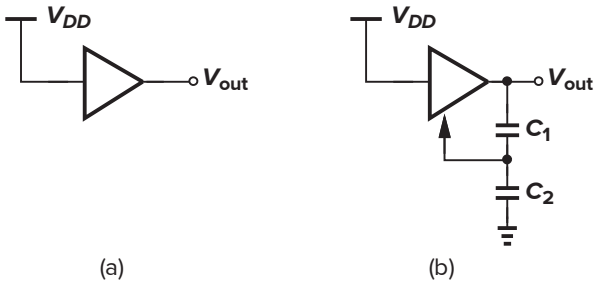

Figure 9.83 Equivalent circuits for path from V_{DD} to output.

9.12 ■ Noise in Op Amps

In low-noise applications, the input-referred noise of op amps becomes critical. We now extend the noise analysis of differential amplifiers in Chapter 7 to more sophisticated topologies. With many transistors in an op amp, it may seem difficult to intuitively identify the dominant sources of noise. A simple rule for inspection is to (mentally) change the gate voltage of each transistor by a small amount and predict the effect at the output.

Let us first consider the telescopic op amp shown in Fig. 9.84. At relatively low frequencies, the cascode devices contribute negligible noise, leaving M_1–M_2 and M_7–M_8 as the primary noise sources. The input-referred noise voltage per unit bandwidth is therefore similar to that in Fig. 7.59(a) and given by

$$\overline{V_n^2} = 4kT\left(2\frac{\gamma}{g_{m1,2}} + 2\frac{\gamma g_{m7,8}}{g_{m1,2}^2}\right) + 2\frac{K_N}{(WL)_{1,2}C_{ox}f} + 2\frac{K_P}{(WL)_{7,8}C_{ox}f}\frac{g_{m7,8}^2}{g_{m1,2}^2} \tag{9.88}$$

where K_N and K_P denote the $1/f$ noise coefficients of NMOS and PMOS devices, respectively.

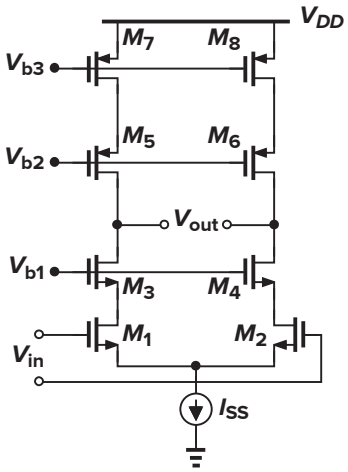

Figure 9.84 Noise in a telescopic op amp.

Next, we study the noise behavior of the folded-cascode op amp of Fig. 9.85(a), considering only thermal noise at this point. Again, the noise of the cascode devices is negligible at low frequencies, leaving M_1–M_2, M_7–M_8, and M_9–M_{10} as potentially significant sources. Do both pairs M_7–M_8 and M_9–M_{10} contribute noise? Using our simple rule, we change the gate voltage of M_7 by a small amount [Fig. 9.85(b)], noting that the output indeed changes considerably. The same observation applies to M_8–M_{10} as well. To determine the input-referred thermal noise, we first refer the noise of M_7–M_8 to the

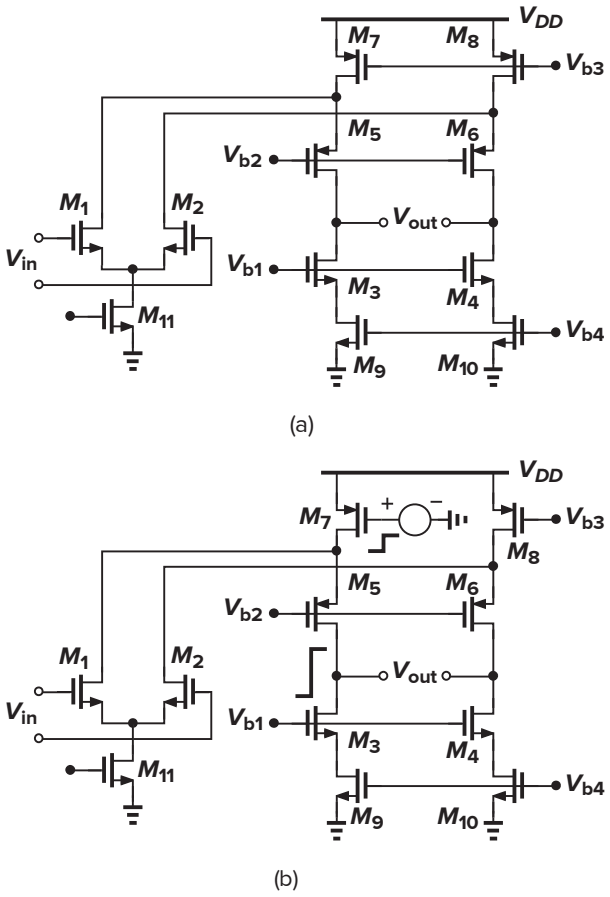

Figure 9.85 Noise in a folded-cascode op amp.

output:

$$\overline{V_{n,out}^2}\big|_{M7,8} = 2\left(4kT\frac{\gamma}{g_{m7,8}}g_{m7,8}^2R_{out}^2\right) \tag{9.89}$$

where the factor 2 accounts for the (uncorrelated) noise of M_7 and M_8 and R_{out} denotes the open-loop output resistance of the op amp. Similarly,

$$\overline{V_{n,out}^2}\big|_{M9,10} = 2\left(4kT\frac{\gamma}{g_{m9,10}}g_{m9,10}^2R_{out}^2\right) \tag{9.90}$$

Dividing these quantities by $g_{m1,2}^2R_{out}^2$ and adding the contribution of M_1–M_2, we obtain the overall noise:

$$\overline{V_{n,int}^2} = 8kT\left(\frac{\gamma}{g_{m1,2}} + \gamma\frac{g_{m7,8}}{g_{m1,2}^2} + \gamma\frac{g_{m9,10}}{g_{m1,2}^2}\right) \tag{9.91}$$

The effect of flicker noise can be included in a similar manner (Problem 9.15). Note that the folded-cascode topology potentially suffers from greater noise than its telescopic counterpart. In applications

where flicker noise is critical, we opt for a PMOS-input op amp as PMOS transistors typically exhibit less flicker noise than do NMOS devices.

As observed for the differential amplifiers in Chapter 7, the noise contribution of the PMOS and NMOS current sources *increases* in proportion to their transconductance. This trend results in a trade-off between output voltage swings and input-referred noise: for a given current, as implied by $g_m = 2I_D/(V_{GS} - V_{TH})$, if the overdrive voltage of the current sources is minimized to allow large swings, then their transconductance is maximized.

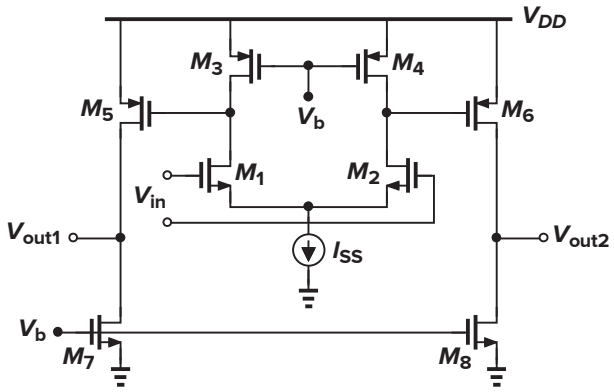

Figure 9.86 Noise in a two-stage op amp.

As another case, we calculate the input-referred thermal noise of the two-stage op amp shown in Fig. 9.86. Beginning with the second stage, we note that the noise current of M_5 and M_7 flows through $r_{O5} \| r_{O7}$. Dividing the resulting output noise voltage by the total gain, $g_{m1}(r_{O1} \| r_{O3}) \times g_{m5}(r_{O5} \| r_{O7})$, and doubling the power, we obtain the input-referred contribution of M_5–M_8:

$$\overline{V_n^2}\big|_{M5-8} = 2 \times 4kT\gamma(g_{m5} + g_{m7})(r_{O5} \| r_{O7})^2 \frac{1}{g_{m1}^2(r_{O1} \| r_{O3})^2 g_{m5}^2(r_{O5} \| r_{O7})^2} \tag{9.92}$$

$$= 8kT\gamma \frac{g_{m5} + g_{m7}}{g_{m1}^2 g_{m5}^2 (r_{O1} \| r_{O3})^2} \tag{9.93}$$

The noise due to M_1–M_4 is simply equal to

$$\overline{V_n^2}\big|_{M1-4} = 2 \times 4kT\gamma \frac{g_{m1} + g_{m3}}{g_{m1}^2} \tag{9.94}$$

It follows that

$$\overline{V_{n,tot}^2} = 8kT\gamma \frac{1}{g_{m1}^2} \left[g_{m1} + g_{m3} + \frac{g_{m5} + g_{m7}}{g_{m5}^2 (r_{O1} \| r_{O3})^2} \right] \tag{9.95}$$

Note that the noise resulting from the second stage is usually negligible because it is divided by the gain of the first stage when referred to the main input.

▶ Example 9.26

A simple amplifier is constructed as shown in Fig. 9.87. Note that the first stage incorporates diode-connected—rather than current-source—loads. Assuming that all of the transistors are in saturation and $(W/L)_{1,2} = 50/0.6$, $(W/L)_{3,4} = 10/0.6$, $(W/L)_{5,6} = 20/0.6$, and $(W/L)_{7,8} = 56/0.6$, calculate the input-referred noise voltage if $\mu_n C_{ox} = 75\ \mu\text{A/V}^2$, $\mu_p C_{ox} = 30\ \mu\text{A/V}^2$, and $\gamma = 2/3$.

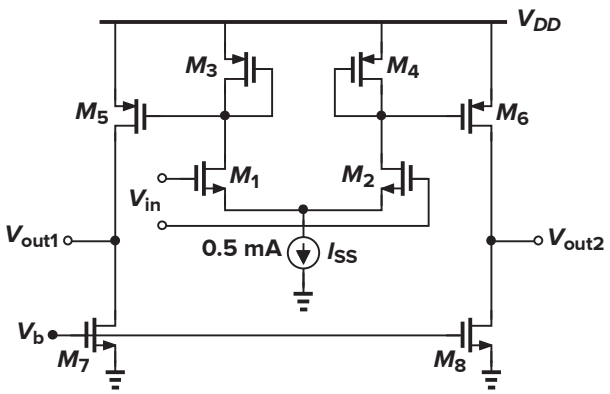

Figure 9.87

Solution

We first calculate the small-signal gain of the first stage:

$$A_{v1} \approx \frac{g_{m1}}{g_{m3}} \tag{9.96}$$

$$= \sqrt{\frac{50 \times 75}{10 \times 30}} \tag{9.97}$$

$$\approx 3.54 \tag{9.98}$$

The noise of M_5 and M_7 referred to the gate of M_5 is equal to $4kT(2/3)(g_{m5} + g_{m7})/g_{m5}^2 = 2.87 \times 10^{-17}$ V^2/Hz, which is divided by A_{v1}^2 when referred to the main input: $\overline{V_n^2}|_{M5,7} = 2.29 \times 10^{-18}$ V^2/Hz. Transistors M_1 and M_3 produce an input-referred noise of $\overline{V_n^2}|_{M1,3} = (8kT/3)(g_{m3} + g_{m1})/g_{m1}^2 = 1.10 \times 10^{-17}$ V^2/Hz. Thus, the total input-referred noise equals

$$\overline{V_{n,in}^2} = 2(2.29 \times 10^{-18} + 1.10 \times 10^{-17}) \tag{9.99}$$

$$= 2.66 \times 10^{-17} \text{ V}^2/\text{Hz} \tag{9.100}$$

where the factor of 2 accounts for the noise produced by both odd-numbered and even-numbered transistors in the circuit. This value corresponds to an input noise voltage of 5.16 nV/$\sqrt{\text{Hz}}$. ◀

The noise-power trade-off described in Chapter 7 is present in op amps as well. Specifically, the devices and bias currents in an op amp can be linearly scaled so as to trade power consumption for noise. For example, if all of the transistor widths and I_{SS} in Fig. 9.87 are halved, then so is the power, while $\overline{V_{n,in}^2}$ is doubled and the voltage gain and swings remain unchanged. This simple scaling can be applied to all of the op amps studied in this chapter. We exploit this principle in the nanometer op amps designed in Chapter 11.

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[1] R. G. Eschauzier, L. P. T. Kerklaan, and J. H. Huising, "A 100-MHz 100-dB Operational Amplifier with Multipath Nested Miller Compensation Structure," *IEEE J. of Solid-State Circuits*, vol. 27, pp. 1709–1717, December 1992.

[2] R. M. Ziazadeh, H. T. Ng, and D. J. Allstot, "A Multistage Amplifier Topology with Embedded Tracking Compensation," *CICC Proc.*, pp. 361–364, May 1998.