



Mandatory lab 3 : Component noise with LTspice



Mandatory lab 3

Send report by email to joar@ifi.uio.no.

Deadlines:

- Final Report – 08:00 Friday 15th of November,

Assessment: Approved / Not approved.

- Reports are submitted on an individual basis.
- The reports should contain the schematics that are used, simulation results, text EXPLAINING what has been done as well as an analysis of the results.
- Put up a summary table and comment at the end of each task when relevant.
- USE WHITE/LIGHT BACKGROUND for the plots!
- Avoid yellow curves.

Mandatory 3: Purpose and tools

- Purpose: Get experience with component noise simulation
- Technology: 350nm CMOS from AMS (Austria Microsystems)
 - Requires model-file
- Simulation tool: LTspice
 - Simulation modes: .tran, .noise, .ac
 - Use our own transistor symbols (that show W, L and model)
- Can be done on private PC

Mandatory 3

- You are going to be using LTspice
- In the specific, you are going to run NOISE simulations within LTspice



Simulation modes

	Time	Frequency
Signal (standard)	.TRAN	.AC
Component noise	.TRAN V (added by user: standard sources or from file) .NOISE TRAN (noise sources generated by software)	.NOISE (noise sources generated by software)
Coupling noise	.TRAN --- V (manually added by user: standard V-sources or from file) --- R, C or L modelling parasitic (Extracted by software or manually added by user)	.AC --- V (manually added by user: AC) --- R, C or L modelling parasitic (Extracted by software or manually added by user)



5

Preparing CMOS model for mandatory 3

Will use transistor models for an integrated circuit: 0.35m CMOS from AMS (Austria Micro Systems)

Preparation

1. Include transistor model card
2. Include symbols
3. Set correct model for transistors in schematic
4. Set correct length and width for transistors in schematic

6

Preparing CMOS model for manatory 3

1. Generally, transistor models can be included as:
 - o A model in the standard library file,
 - o As a private library file. Must include link (as text) in schematic, or
 - o As entire model as «text» in the schematic

⇒ You may first try the first alternative and replace <program files>/LTC/LTspiveIV/lib/cmp/standard.mos with our own file. If that does not work, place the model-fil in the same folder as your design and add a link in the schematice
2. Transistor symbols
 - o We use our own transistor symbols (that show widths, lengths etc.). They must be on the same directory as we have our schematics (nmos4.asy, pmos4.asy)

7

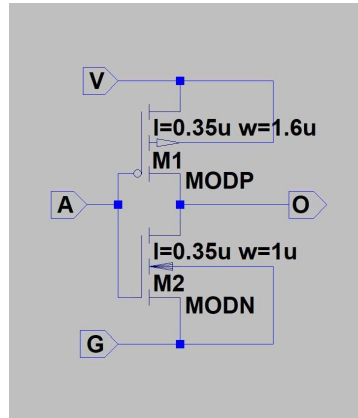
Preparing CMOS model for manatory 3

3. Correct transistor model:
 - o Change the transistor model name for NMOS transistors to MODN and for PMOS to MODP
4. Change transistor width and length
 - o Set the correct transistor sizes in each transistor. In figures the transistor sizes are often given in Width/Length. Remember to add «u» or «μ» after the numbers to give correct value. If not the sizes will be interpreted as meters (with no warning). Right click on the component to change height and width.

8

Inverter transistor example

- PMOS: Outgoing arrow connected to high supply
- NMOS: Incoming arrow connected to low potential



9

LTspice: .NOISE analysis

.NOISE is used to simulate component noise in the frequency-domain. The simulator includes by itself noise for all components in the schematic.

Example: **.NOISE V(out) V1 dec 200 1m 1G**

- Out: Name of network node
- V1: Name of source instance. May be voltage or current
- Dec: Type of sweep (decad, octave, linear or list)
- 200: Number of points per decade/octave
- 1m: Start frequency (1m = 1 milli Hz, 1Meg = 1 Mega Hz)
- 1G: Stop frequency

10

LTspice: .NOISE analysis

- Simulation results:
 - Onoise: Total coupling noise at node «V(out)»
 - Gain: Gain from V1 to V(out).
 - Inoise: Equivalent input noise at V1. Noise at output divided by gain.
 - Noise contributions from all other component noise contributing elements.
- Spot/integrated noise
 - The simulation shows the spot noise at each frequency
 - Integrated noise can be found by:
 - Right clicking on the selected signal. NB: this gives the noise for the entire simulated frequency range.
 - Use the .meas function
 - Warning! For integrating inoise, dont use frequency regions where gain < 1.

11

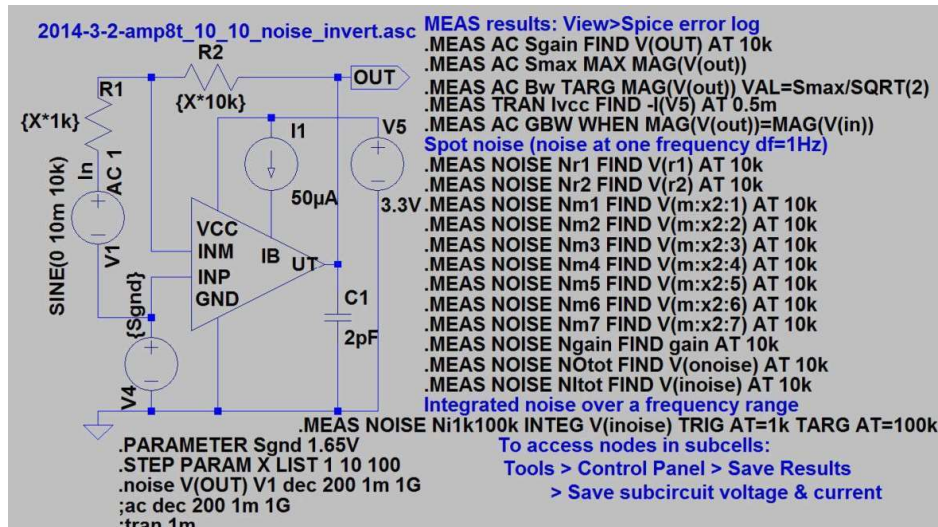
LTspice: .MEAS – measure and save

.MEAS directive is used to measure and save some variables in the spice «error log» (right click →View→Spice Error Log)

Examples (AC – for AC simulation – NOISE for noise simulation):

- **.MEAS** AC Smax MAX MAG(V(out))
- **.MEAS** AC BW TARG MAG(V(out)) VAL=Smax/SQRT(2) FALL=1
- **.MEAS** AC GBW WHEN MAG(V(out))=MAG(V(in))
- **.MEAS** NOISE N_R1 FIND V(r1) AT 10k
- **.MEAS** NOISE Ni10k100k INTEG V(inoise) TRIG AT=1k TARG AT=100k

12

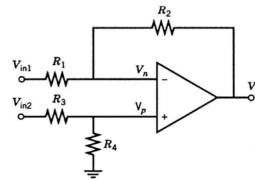


13

14

Task 1. Ideal amplifier

$$V_o = \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_1} \right) V_{in2} - \left(\frac{R_2}{R_1} \right) V_{in1}$$



We will first look at an ideal amplifier in an ideal differential amplifier configuration. You can copy the amplifier symbol from the "opamp" circuit in the "Educational" area. Let the opamp Aol be 100k and the GBW be 10Meg. Be sure to get the "include" statement. Build a resistive network around as indicated in Figure 3-4 "Differential amplifier using one op amp" page 56 (figure in Motchenbacher). For all cases the relation between the resistors will be $R_1=R_3=R_x$ and $R_2=R_4=10R_x$.

a) Let R_x be 1kΩ, 10kΩ and 100kΩ. Is the gain different in the three cases?

Run .NOISE simulations and find the output noise and equivalent input noise for the three cases at 10kHz. Find the total equivalent input noise both at the positive and the negative input by simulation (in the region where the gain is larger than one). What type of noise is present here?

b) Calculate manually the noise for each of the resistor elements i) locally (at their position), their value at the ii) output and their equivalent value at the iii) input. Use the table below. Which of them has the largest contribution at the output and at the input? Which of these can you find in the simulation results?

Example table:

	Local noise (nV/√Hz)	Gain to output	Noise at output (nV/√Hz)	Equivalent noise at input(nV/√Hz)
R1				
R2				
R3				
R4				
Total				

15

Task1: Ideal Amplifier

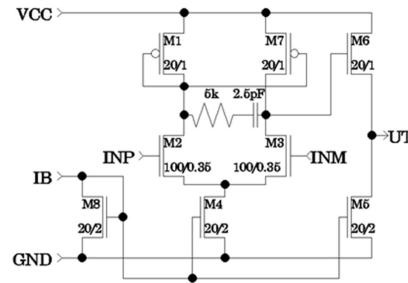
- Studying the performance of the ideal amplifier in a resistive feedback loop
- Copy the amplifier symbol from the "Educational" area. Include ".lib opamp.sub" on the schematic
- Opamp settings: Gain = 100k and GBW = 10Meg
- Fill out the table based both on hand calculations and simulations
- Disadvantage/advantage of small/large R? (Hint: Noise ⇔ Power)

$$V_o = \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_1} \right) V_{in2} - \left(\frac{R_2}{R_1} \right) V_{in1}$$

	Local noise (nV/√Hz)	Gain to output	Noise at output (nV/√Hz)	Equivalent noise at input(nV/√Hz)
R1				
R2				
R3				
R4				
Total				



Task 2. Simple CMOS amplifier



- Perform AC analysis for the amplifier without feedback (i.e. open-loop). Let the common mode voltage (i.e. DC voltage of input signal) be 1.65V. Do AC analysis with a signal on the positive input (ACpos=1, ACneg=0), on the negative input (ACpos=0, ACneg=-1) and with differential signals on both inputs (ACpos=1, ACneg=-1).
- Replace the ideal amplifier in the feedback network in task "1 Ideal amplifier" with our new amplifier. Let $R_x = 1\text{k}\Omega$. Inspect the simulation results on the positive input and the output. What is the frequency range at which the flicker noise is dominant?
- We would like to know the (spot) noise at some frequencies and the integrated noise over some frequency ranges. Find the (positive) input and output noise at 1Hz, 1kHz, 1MHz and 1GHz. Then find the noise for the areas 1Hz-1kHz, 1kHz-1MHz and 1Hz-1MHz. (Use the .MEAS statement). How can we manually calculate the noise in the range 1Hz-1MHz from the two subareas we found through simulation?
- Perform the same NOISE simulation as in task 1 with $R_x = 1\text{k}\Omega$, $R_x = 10\text{k}\Omega$ and $R_x = 100\text{k}\Omega$. Simulate with a capacitive load of 1pF. List the six largest sources of noise at 1MHz for all three cases. Comment on the result.

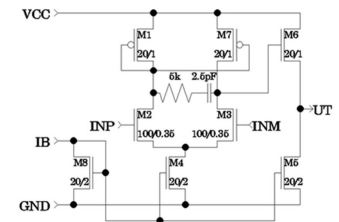
Task2: Simple CMOS Amplifier

	$R_x=1\text{k}\Omega$	$R_x=10\text{k}\Omega$	$R_x=100\text{k}\Omega$
1.	<Strongest noise source>	<Strongest noise source>	<Strongest noise source>
2.	<2nd strongest noise source>	<2nd strongest noise source>	<2nd strongest noise source>
3.	<3th strongest noise source>	<3th strongest noise source>	<3th strongest noise source>
4.	<4th strongest noise source>	<4th strongest noise source>	<4th strongest noise source>
5.	<5th strongest noise source>	<5th strongest noise source>	<5th strongest noise source>
6.	<6th strongest noise source>	<6th strongest noise source>	<6th strongest noise source>

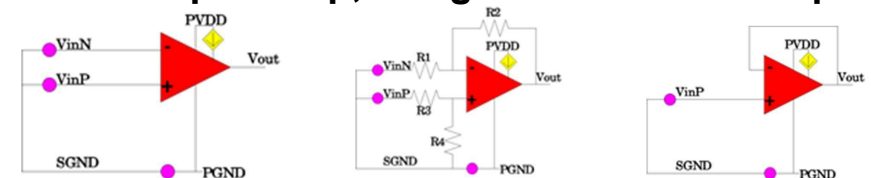
- Fill out the table above with the identity and contributions within each cell. (Use the same transistor indexing as in previous figure.)
- Hint: In the rightmost column the resistors will be dominating while in the leftmost column amplifier transistors will dominate.

Task2: Simple CMOS Amplifier

- .ac analysis for the open loop circuit without the feedback
- Perform the .ac analysis for the resistive network of task 1 when you replace the ideal amplifier by this amplifier
- Finding the spot noise (.noise) at 1Hz, 1kHz, 1MHz, and 1GHz and integrated noise for the areas of 1Hz-1kHz, 1kHz-1MHz, and 1Hz-1MHz
- Repeat the task 1 with this amplifier
 - Find the 6 strongest noise sources



Task 3. Open loop, 10x gain and closed loop

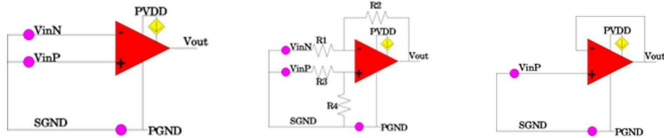


In this task you shall find the spot noise (.noise) at 1MHz and the integrated noise from 1 Hz to 1 MHz at output and the positive equivalent input. Find this for open loop, for 10x (copy results from previous task!) as well as a follower. Present your results in a table.

The small pink circles are voltage sources. The voltage sources between SGND and PGND is a 1.65V DC source.

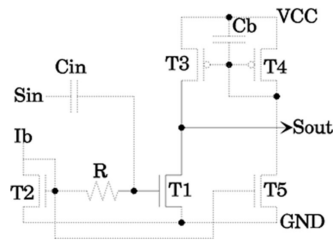
Task3: Open loop, 10x gain and closed loop

- Fining spot noise and integrated noise for three different structures



	Spot noise 1 MHz (nV/√Hz)	Integrated noise 1Hz – 1 MHz (μV)
Open loop		
Equivalent input noise		
Gain		
Output noise		
10x gain		
Equivalent input noise		
Gain		
Output noise		
Follower		
Equivalent input noise		
Gain		
Output noise		

Task 4. Common source input stage - RF



- How large must C_{in} be to not mute the signal more than about 10%? Generate a figure with C_{in} on the x-axis and signal strength on the Y-axis.
- How large must R be to not contribute significantly (<10%) of the total noise? (R will have minimum contribution for small and large resistor values. However, at small R values the resistor will mute the input resulting in a low gain. Hence, we have to go for a sufficient large resistor value.)
(You may use .MEAS NOISE N_r1_onoise FIND V(r1)/V(onoise) AT 1Meg to find the relation between R 1 noise and total noise.)
- What does the C_b do? How much noise reduction can we achieve with C_b and how large must C_b be to achieve this? What is the gain, noise on the output and equivalent input noise now with a large C_b ?

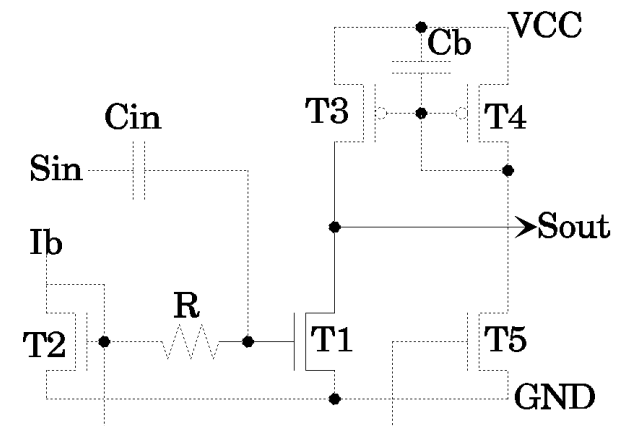
Use the values you have found for C_{in} , R and C_b in the following.

- Try doubling the width of the NMOS transistor, the length of the NMOS transistor, the PMOS transistor width and length of the PMOS transistor. Find the output noise, equivalent input noise as well as the gain for these 5 setups (reference + 4 variations) at 1MHz and put them up in a table.
- Increase the power I_b in steps of $10\mu A$ from $10\mu A$ to $100\mu A$, and find the output noise, equivalent input noise and gain at 1MHz. Plot the equivalent input noise as a function of current.

Task 3. Open loop, 10x gain and closed loop

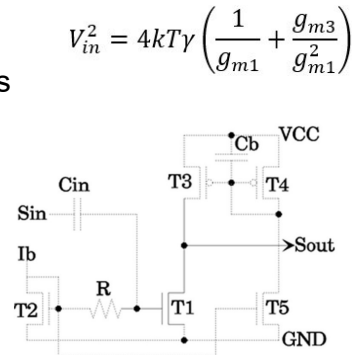
- Comment: Here you will find that the follower (gain=1) and open loop (large gain) has the same equivalent input noise. Does that mean they are equally good? Will their gain influence on the noise contributions from subsequent circuitry?

Task 4. Common source input stage - RF

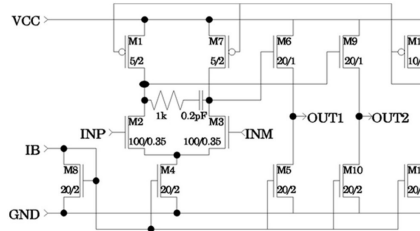


Task4: Common Source Amplifier- RF

- Finding C_{in} as the signal is not muted by more than 10% ($R = 1k$ and $f_{in} = 1MHz$, $I_b = 10uA$)
- Finding the range for R as its contribution on the output noise is <10%.
- What is the role of C_b ?
- Doubling the W_n , L_n , W_p , L_p
- Increasing the I_b
- Replacing CMOS with Bipolar transistors

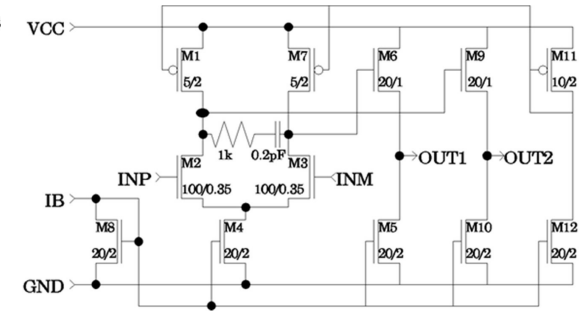


Task 5: CMOS Amplifier with Differential Input and Output



- Finding the gain for each input, and differential input, finding the output noise and equivalent input noise
- Look at the effect of noise on the power supply, VCC (.AC)
 - $M2$ and $M3$ are identical
 - $W_{M2} = W_{M3} + 0.1W_{M3}$
- Specify the power consumption variation

Task 5. CMOS amplifier with differential input and output



Use the same input forces and the same transistor models as in the previous task.

- Find the gain for each signal input, the differential gain, output noise and equivalent input noise with a $50\mu A$ current bias.
- Set up a simulation to find the effects of noise from the supply voltage VCC . Find impact on each of the outputs individually and on the difference between the outputs. Do the same simulation first where $M2$ and $M3$ are identical (as defined above) and then with the width of the $M2$ 1% greater than the width of $M3$. Put the results in a table and comment.
- Try to specify the variation in power consumption at VCC when the input signal is a 1MHz sine with amplitude 10mV.

Task 5: CMOS Amplifier with Differential Input and Output

- Simulation setup:
 - In all cases the DC's are: $INP \& INM = 1.65V$, $VCC=3.3V$
 - AC values as given below

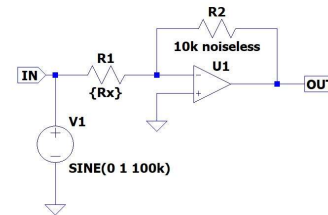
	INP AC	INM AC	VCC AC	sim. mode	Look for...
a) i)	1	0	0	.ac	OUT1, OUT2, OUT1-OUT2
a) ii)	0	-1	0	.ac	OUT1, OUT2, OUT1-OUT2
a) iii)	1	-1	0	.ac	OUT1, OUT2, OUT1-OUT2, OUT1+OUT2
a) iv)	1	0	0	.noise	inoise(INP) => onoise(OUT1), inoise(INP) => onoise(OUT2), gain for both cases above
a) v)	1	-1	0	.noise	Inoise(INP) => onoise(OUT1), gain,
b)	0	0	1	.ac	OUT1, OUT2, OUT1-OUT2
c)	0	0	1	.ac	OUT1, OUT2, OUT1-OUT2

Task 5: CMOS Amplifier with Differential Input and Output

- Note:
 - Output difference has to be calculated by the simulator.
 - Method: Select a signal among those available. Plot it in the result window. Click on the name and edit the name from say «V(out1)» to «V(out1)-V(out2)».

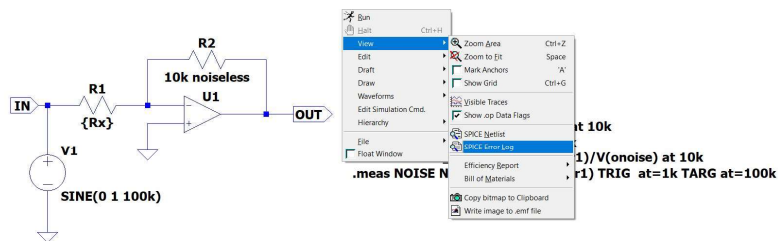
29

Example: How to plot .MEAS data

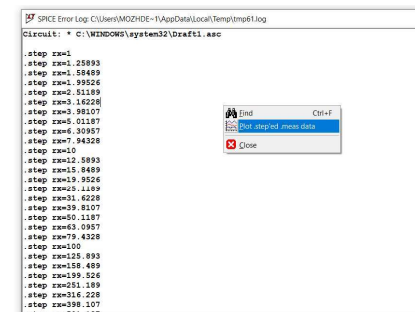


```
.inc opamp.sub
.noise V(OUT) V1 dec 200 1m 1G
.step dec param Rx 1 1000k 10
.MEAS noise NIitot FIND V(inoise) at 10k
.MEAS noise Nr1 FIND V(r1) at 10k
.MEAS noise N_r1_onoise FIND V(r1)/V(onoise) at 10k
.meas NOISE Nr1_INTEG INTEG V(r1) TRIG at=1k TARG at=100k
```

Example: How to plot .MEAS data

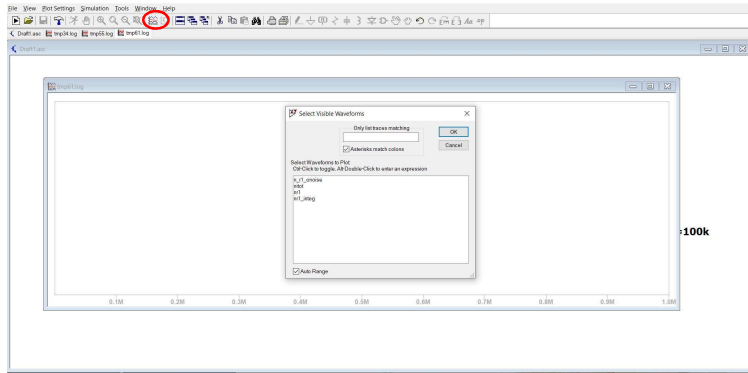


Example: How to plot .MEAS data

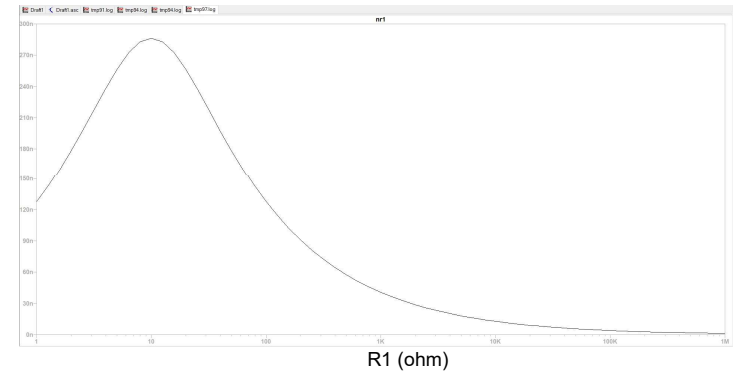


```
p.sub
OUT) V1 dec 200 1m 1G
param Rx 1 1000k 10
ise NIitot FIND V(inoise) at 10k
ise Nr1 FIND V(r1) at 10k
ise N_r1_onoise FIND V(r1)/V(onoise) at 10k
ISE Nr1_INTEG INTEG V(r1) TRIG at=1k TARG at=100k
```

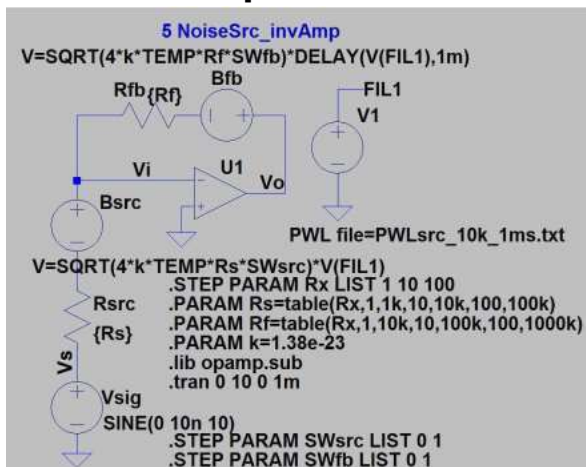
Example: How to plot .MEAS data



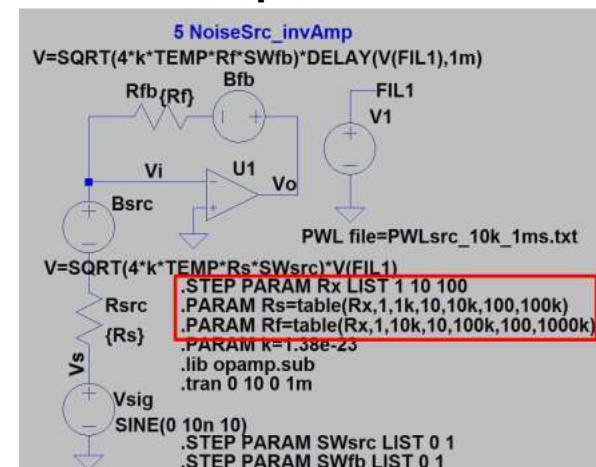
Example: How to plot .MEAS data



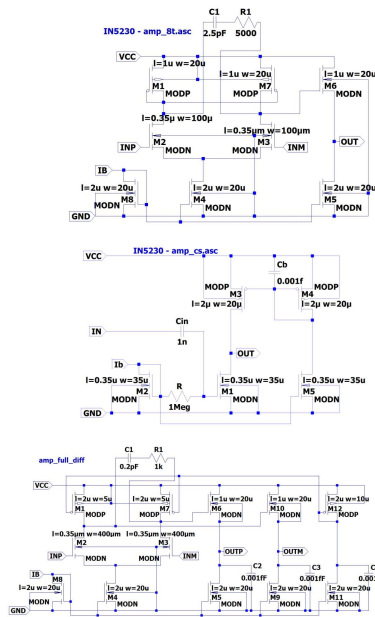
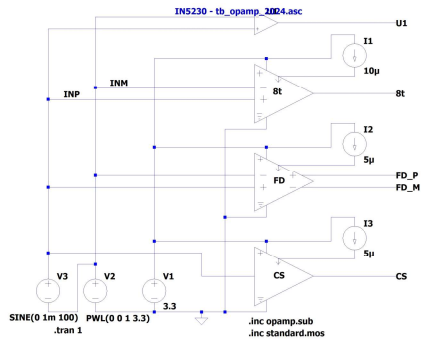
Transient component noise simulation



Transient component noise simulation



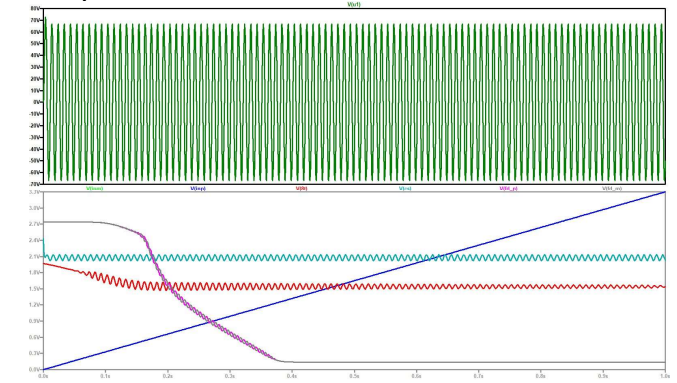
2024 - schematics



37

Testbench: tb_amp_2024.asc

- Input: Ramp with small sinus



38