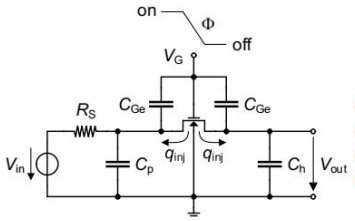


UiO : Department of Informatics
University of Oslo

IN5230
Electronic noise – estimates and countermeasures

Lecture 14
Flicker, Chopper and Switches

Non-ideal Effects in Switches



- clock feedthrough,
- channel charge injection
- sampled noise and
- leakage current.

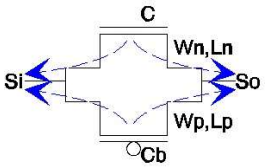
$$\Delta V = \alpha \cdot \frac{C_{Ge}}{C_{Ge}+C_h} \cdot V_{swing} + \frac{q_{inj}}{C_h} + \sqrt{\frac{kT}{C_h}} + \frac{I_{leak} \cdot T_h}{C_h}$$

- BSIM3 and BSIM4 does not model correct
- All contributions decrease if a larger hold capacitor is used, but cost power.

Techniques to Reduce Charge Injection

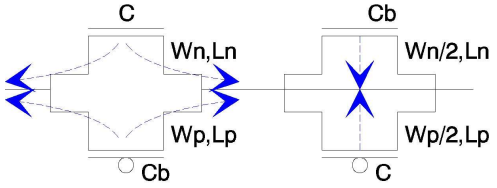
- The simplest technique uses **complementary switches** in such a way that the charges released by one switch are absorbed by the complementary device building its channel. This technique is rather inefficient, since the matching between the channel charges of the n-MOS and the p-MOS devices is poor and signal dependent. This charge mismatch is further degraded by phase jitter between the two complementary clocks
- Other more efficient strategies are described below
- It should be noted that **none of the techniques** described below offers a **perfect charge-injection cancellation**
- The efficiency of the **half-sized dummy transistor** technique depends on a proper layout in order to insure a good matching and a first-order insensitivity to doping gradient
- The technique which usually offers the best results is a **combination** of a fully **differential structure** and the **half-sized dummy transistor** technique

Charge injection countermeasures



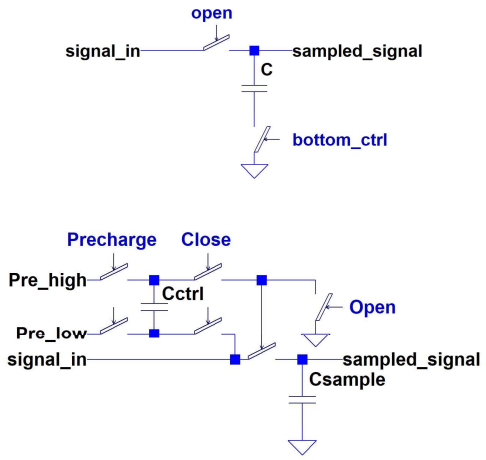
- Charge distributes according to the two terminal impedances. (Most charge to the lowest impedance)
- Possible countermeasures
  - Fast clock edges : Half charge to each terminal
  - Slow clock edges: Charge to low impedance
  - Dummy half-sized transistors on each side (next slide)
  - Bottom plate sampling: Make sampling capacitor have high impedance (second next slide)

Dummy half-sized switches



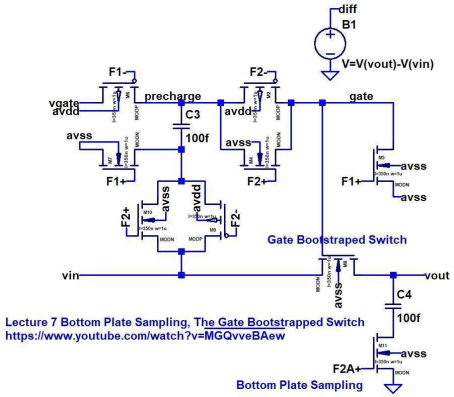
- A proposal is to add a pair of half-sized “opposite” dummy transistors. However, this solution requires impedance symmetry.

- Bottom plate switching
  - Makes capacitor high impedance when sampling switch opens
- Gate bootstrap
  - Fixed *gate-vin* control voltage reduces errors due to variable *gate-vin* difference



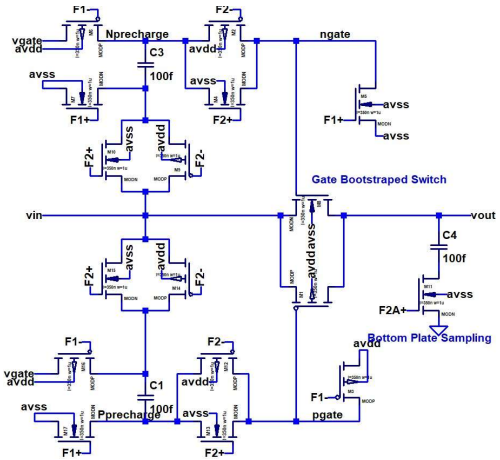
Gate bootstrapped switch with bottom plate sampling

- Bottom plate switch
  - Makes capacitor high impedance when sampling switch opens
- Gate bootstrap
  - Fixed *gate-vin* voltage reduces the errors steps *vin* dependence



Double gate bootstrapped switch with bottom plate sampling

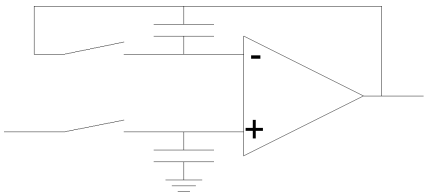
- Bootstrap on both NMOS and PMOS



Sampler with switch charge cancelation

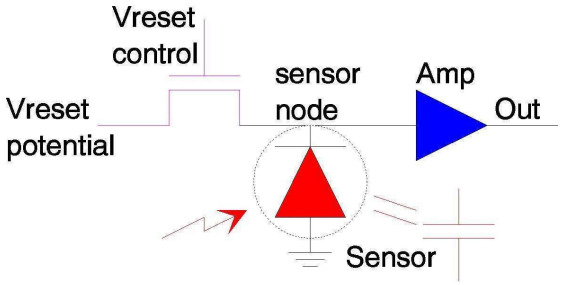
- A differential sampler with same sized switches on both inputs may almost eliminate the influence by the charge injection.
- At sampling both switches have the same potential and generates similar charge on both inputs.
- (Preferably output impedance of previous stage and present stage should be similar)

RED: Figure



Correlated double sampling: Background

- Photo diodes (CMOS pixel cells) consist of a reversed biased diode operating as a capacitor.



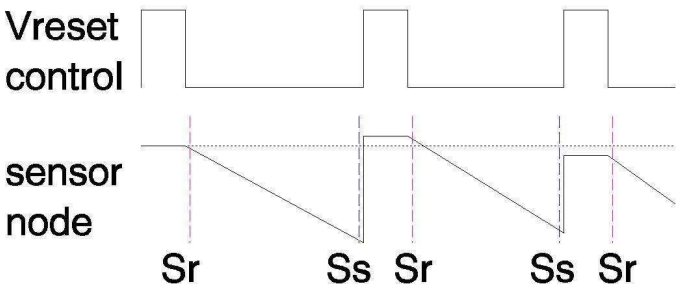
YELLOW: Figure

- A switched reset potential is placed on the sensor node. Accumulated electrons generated from light photons reduces the sensor node potential.

Correlated double sampling

YELLOW: Figure

Due to charge injection and thermal noise the sensor node will be resat to unpredictable levels.

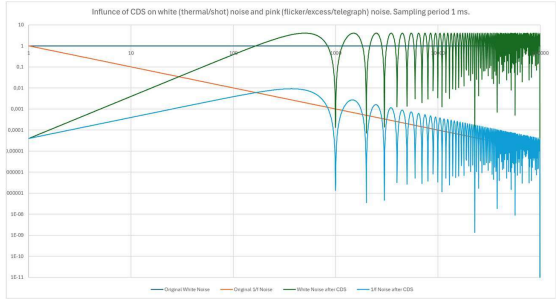


With correlated double sampling the value is measured both immediately after reset and before next reset. The difference is used.

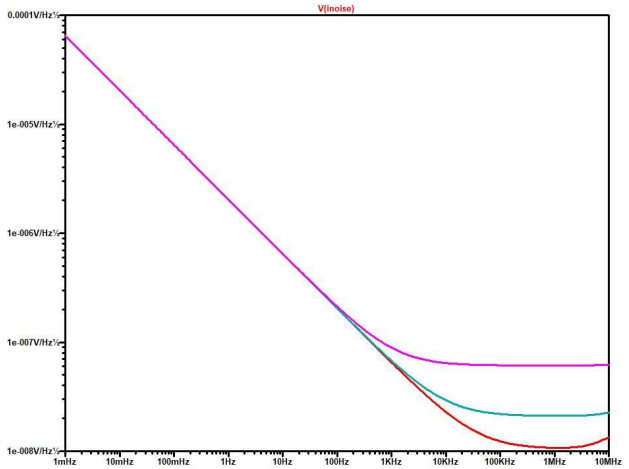
CDS influence on noise

- Correlated Double Sampling influence on white and pink noise.
- Sampling rate (i.e. time between reset and signal sample is 1 ms.)
- Note: Here is Fc=1kHz. In reality Fc is MHz.
- Minimum noise at f=n/T where n is natural numbers (including 0). (0 Hz, 1 kHz, 2 kHz, …)
- Maximum white noise at f=(n+1/2)/T, flicker at a somewhat lower frequency (500 Hz, 1500 Hz, 2500 Hz, …)

$$S_{\mathrm{CDS}}(f) \propto S(f) \times (1 - e^{-j2\pi fT})^2$$
$$S_{\mathrm{CDS}}(f) = S(f) \cdot |H_{\mathrm{CDS}}(f)|^2 = S(f) \cdot 2 \times (1 - \cos(2\pi fT))$$



- Figure: Equivalent input noise for 350nm OpAmp with 3 different feedback resistances
- Flicker noise corner frequency approach 100MHz for the smallest sizes



Flicker noise - sources

- Most dominant sources for CMOS
  - Surface grid phenomena in the interface between crystal and oxide.
    - Dominating in conservative technologies, less in newer with smaller transistor lengths.
    - Increase with current.
  - Traps inside the oxide.
    - Dominating in the newest, most scaled technologies
    - Occurs also when no current is passing

Flicker noise reduction methods

1. Sizing of transistors
2. Bias switching and Large-signal excitation (LSE)
3. Chopping/modulation
4. Correlated Double Sampling (CDS) and Auto-Zero (AZ) techniques (also described in F9-Razavi)

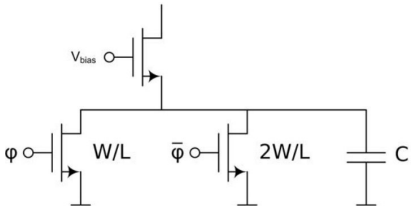
1. Sizing of transistors

- Common expression for flicker noise representation at the gate:

$$V_g^2 = \frac{K}{WLC_{ox}f}$$

- This expression is independent of current in the channel
- Noise decreases with the inverted square root of the transistor area.
  - Costly:
    - A reduction by 10 requires 100 times the area.
    - More area means more capacitance and lower frequency response.
    - Maintaining frequency response requires more power

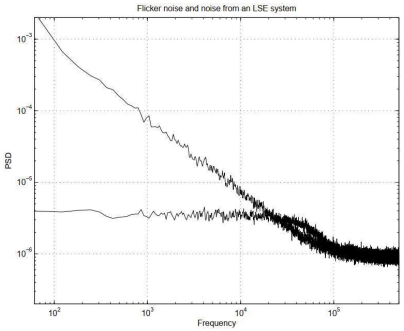
2 Bias switching and large-scale excitation (LSE)



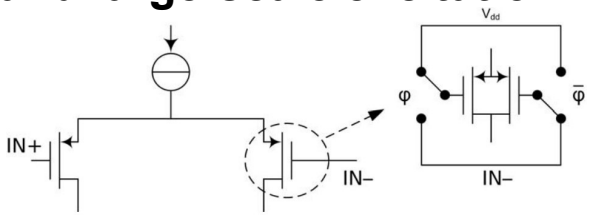
- Figure: Switched current source. Duty-cycle 0% - 100% spans a factor 2 in current tuning. Measured noise is less than simulated. Reason is switching a transistor off kicks some electrons out of their traps.

2 Bias switching and large-scale excitation (LSE)

- Figure: Matlab-simulation where the memory of the flicker noise is deleted (turned off) almost completely once every 10 μs (lower curve). Upper curve is reference (constant on). (No circuit simulator yet (in 2008) that takes flicker noise memory effects into account.)



2 Bias switching and large-scale excitation (LSE)



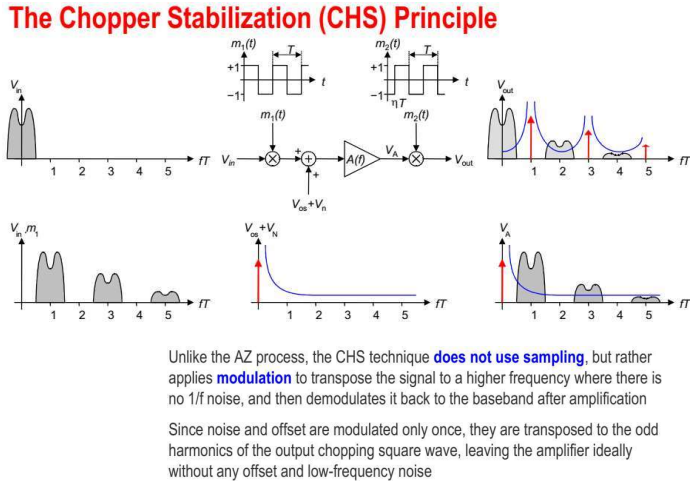
- Figure: Switched differential pair at op-amp input. The one turned off is in cut-off. Low-f noise was measured reduced by 5 dB.
- Reduces flicker noise but generates switch noise at switch frequencies and harmonics. (Trade-off)
- Another alternative could be to short-circuit source-drain while isolating from other functionality.

2 Bias switching and large-scale excitation (LSE)

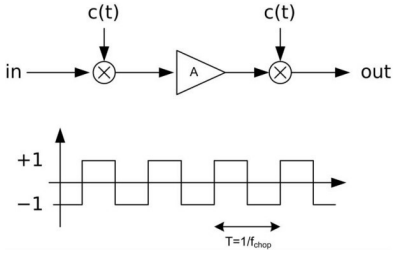
- Gives some reduction of flicker noise
- Seems to be more predictable at conservative technologies.
- Unpredictable in newer technologies and may give more noise
- Poorly modelled by simulation software
- The next two methods seems to be better

3 The Chopper Stabilization (CS) technique

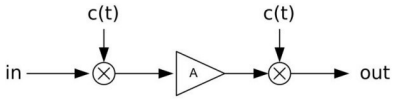
- CS requires two mixers
- It is only noise generated between the mixers that are reduced.



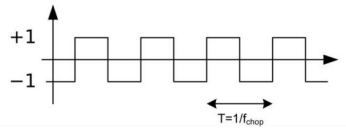
3 Chopping



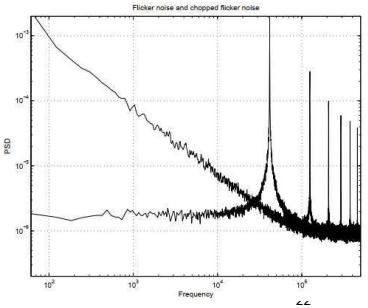
- Figure: The principle of chopping. The signal is modulated before and (back) after the flicker-noise contributing part (here: amplifier).
  - First mixer: signal modulated to f_chop, 3*f_chop, 5*f_chop, etc.
  - Last mixer: Signal is modulated back to baseband. Flicker and offset is modulated up to f_chop.
  - f_chop has to be significant above signal bandwidth
  - Below f_chop the noise is white and at the level of the amplifier output at frequency f_chop. A preferred f_chop is the 1/f-noise corner frequency.



3 Chopping

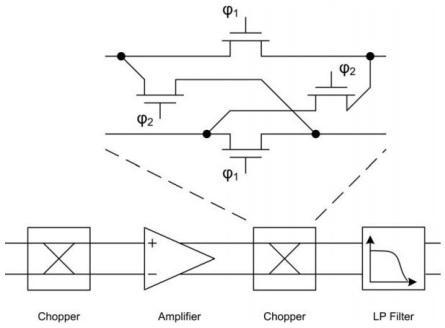


- Note that chopping does not remove the flicker and offset contributions. Thus, it is common to add a low-pass filter after the last mixer to remove these contributions.
- Flicker noise and chopped flicker noise. With chopping the low frequency noise level is equal to the noise at the chopping frequency without chopping. Thus f_chop should be f_corner or higher. Figure 12 and 13:



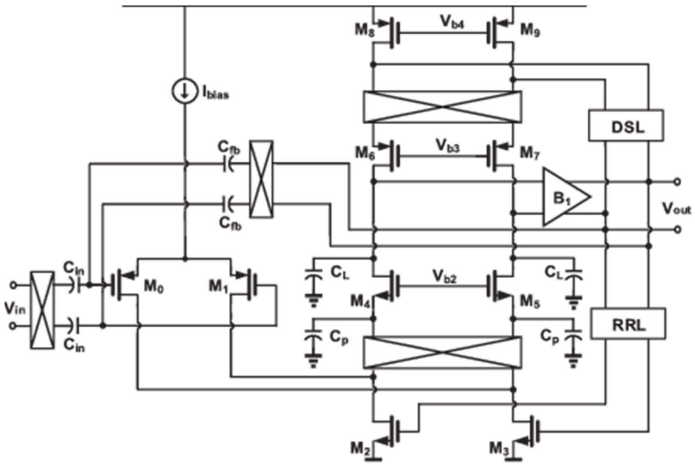
3 Conventional chopper amplifier

- Chopper amplifier Figure 14:
- Design guidelines:
  - f_chop > f_corner
  - f_chop > 2* f_sig_bw
  - Amp working band: f_chop ±f_sig
  - LP-filter pass up to f_sig (stop from below f_chop).
  - Switches with minimum charge injection.



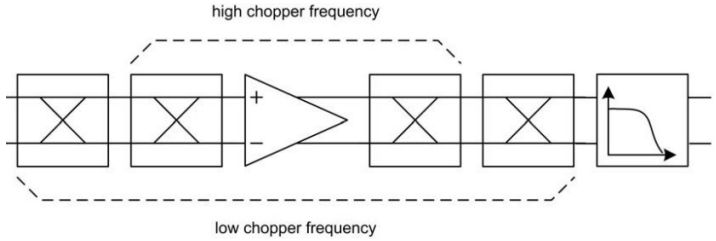
3 Chopper on Folded cascode

- Noisy and switched: M0, M1, M2, M3, M8, M9
- Less noisy and stable: M4, M5, M6 and M7



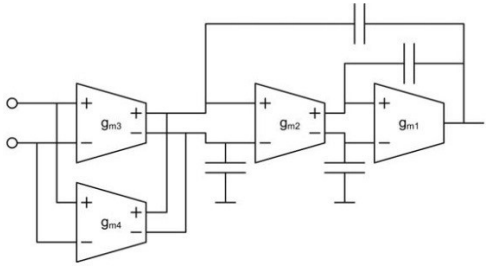
3 Conventional chopper amplifier

- Nested chopper amplifier. Reduces influence from charge injection. Fig 15:
- f_chop_high > f_corner, f_chop_low > 2* f_sig_bw
- Outer eliminates charge injection from inner. Outer remains but is less due to lower clock rate.
- Let inner edges be some time after outer edges so that error pulses from first chopper can die away.



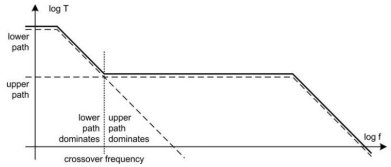
3 Multi-path chopper amplifiers

- All previous must fulfil f_chop > 2*f_sign_bw. May be avoided with multi-path chopper
- DC-gain larger and f_gbw lower in 4 compared with 3. Transfer function of 3 and 4 will cross in f_cross. Below f_cross 4 will dominate and above 3 will dominate. The lower can be replaced with a chopper.
- Example [17] has 1uV offset, f_chop = 4 kHz, f_sign_bw = 1.3MHz with 50pF load. Somewhat more residual offset than others but very much higher upper signal frequency.



- Fig 16: Multi-path amplifier.

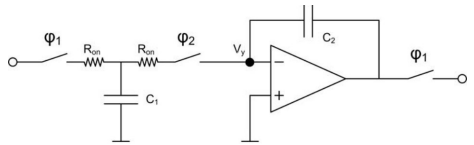
- Fig 17: Open-loop transfer function of the multi-path amplifier



4. Correlated Double Sampling (CDS) and Auto-Zero (AZ) techniques

- Example given in slide set F9-Razavi
- But first: Sampling in general

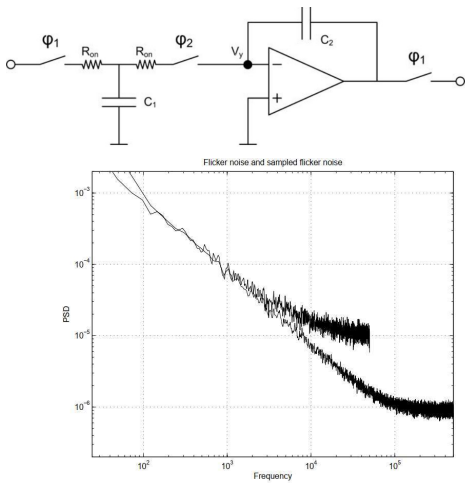
Sampled noise in SC (Switch Cap) circuits



- If the noise bandwidth (f_{nbw}) is larger than the sampling frequency (f_{clk}), the higher frequency noise will be “folded” into the lower frequency region. The total amount of noise will not be reduced.

Sampled noise in SC circuits

- Thus, sampling 10-MHz-wide white noise at 1 MHz gives 20 times higher noise power.
- Figure: PSD of white noise overlaid by flicker noise, sampled with 1MHz (over-sampled) and 100kHz (under-sampled).
  - Over-sampling gives same flicker noise but less white noise due to less aliasing

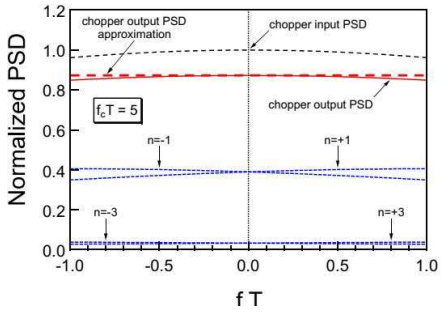


Flicker noise reduction (Ref: ChatGPT)

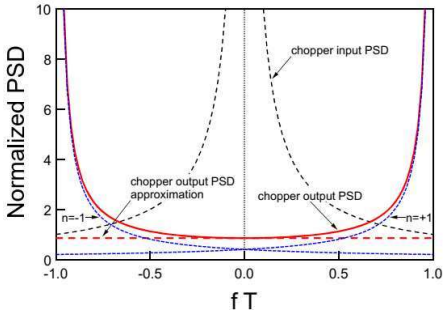
- Process-Level Improvements
  - High-Quality Oxide Layers
  - Thin Oxide Layers
  - Surface Passivation
- Circuit-Level Techniques
  - Correlated Double Sampling (CDS)
  - Chopper Stabilization (Modulation)
  - Auto-Zeroing Techniques
  - Use of Differential Circuits
- Device-Level Techniques
  - Larger Transistor Size (Increase Area)
  - Use of PMOS Transistors
  - Biasing Techniques
- Digital Calibration
  - Digital Signal Processing (DSP)
- Use of Low-Noise Technologies
  - SOI (Silicon-on-Insulator)
  - Buried Channel Transistors

The Chopper Stabilization (CS) technique

Effect of Chopping on the Amplifier White Noise

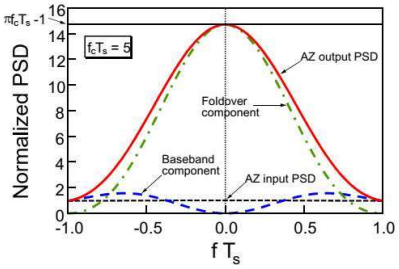


Effect of Chopping on the Amplifier 1/f Noise

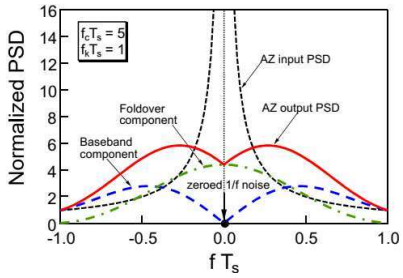


The Autozero (AZ) technique

Effect of AZ on amplifier white noise



Effect of AZ on amplifier 1/f Noise



The Chopper Stabilization (CS) technique

Conclusions

- Autozero and chopper stabilization are very effective techniques to reduce 1/f noise in low-frequency analog circuits
- They have been used extensively in the recent years to fight against the increased 1/f noise of nano-scale CMOS
- AZ is a **sampling technique** resulting in **noise aliasing**
- Thanks to the high-pass characteristic, the 1/f is canceled at the cost of an **increase of the white noise** coming from the foldover component
- Unlike AZ, CS **does not alias noise**
- 1/f noise is shifted to higher frequency **with almost no penalty on the residual white noise**