

UiO : Department of Informatics
University of Oslo

IN5230 Electronic noise – Estimates and countermeasures

10 credits

Thursdays in seminar room Postcript (<room number>)

09:15-11:00 Lectures

11:15-12:00 Optional hour for lab presentation etc.

Lecturer: Joar Martin Østby, joar at ifi.uio.no

Teaching assistant: Pål Gunnar Hogganvik, paalgh at ifi.uio.no

Time for lecture and lab presentation

- Alt1: Friday 09:15-11:00(-12:00)
- Alt2: Monday 09:15-11:00(-12:00)
- Alt3: Thursday 09:15-11:00(-12:00)

Electronic noise – estimates and counter measures

Electronic noise…

⇒Noise is a challenge in all electronic systems.

⇒ In sensor systems:

-Determine smallest measurable value

-Determine step resolution

(Eg RF: distance and data rate)

⇒ In digital systems: May result in wrong functionality in larger systems (wrong state in digital systems)

⇒ EMC (Electromagnetic Compatibility): Regulations

⇒ Future trends:

⇒ More dense structures on integrated circuits

⇒ Smaller and more compact packaging

⇒ Lower supply and threshold voltages

⇒ Lower noise thresholds

⇒ Higher frequencies/steeper edges

All lead to increased noise generation and noise sensitivity.

⇒Conclusion: Huge need for noise expertise now and rising demand in the future

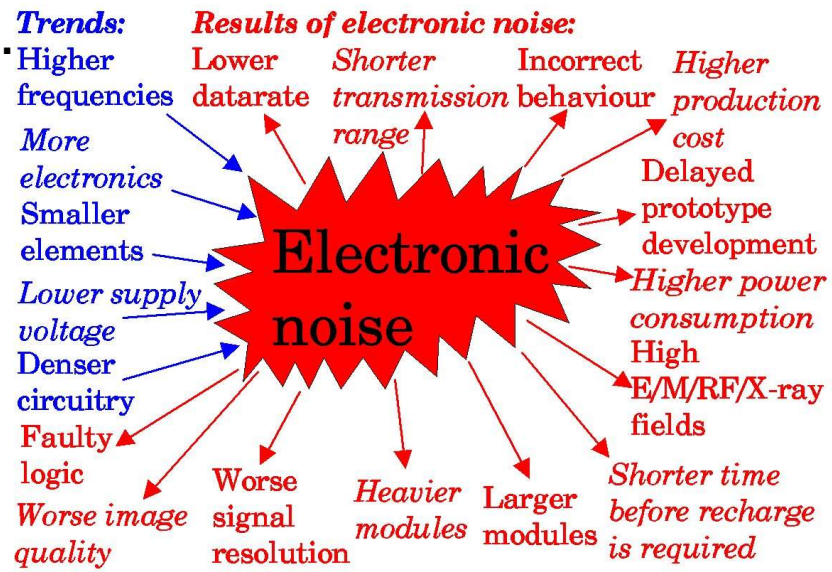
… Estimates and countermeasures

Design for acceptable noise levels implies a repetitive loop were

- The design is modified and
- The dominating noise sources is identified

until an acceptable noise level is achieved

This is done first theoretically/mathematically, then with simulation and eventually at the end by modifying the manufactured design.



Target students for the noise course

- The other master courses at Nanoelectronics are CMOS courses while this course target electronic designers in general. (I.e. also targeting those not doing CMOS design.)
- Both
  - Physic students doing electronic design in general and
  - Informatic students doing nano electronic (CMOS) design.
- Physic students will have a small taste of CMOS design but the course is not a “CMOS-design course”
- Nano electronic students will have a taste of EM-fields, packaging, PCB and system design
- Simulation tool: LTspice from Analog devices (and not Cadence)

Colour code for lecture slides

- Yellow: You should be able to explain and discuss the figure, equation etc when the figure/equation is given by the examiner
- Red: You should be able to draw the figure/give the equations without help and explain/discuss

What is noise?

- The term «noise» is borrowed from acoustics
- Acoustic noise:
  - Unwanted sound – (a subjective definition). (However it is uncomfortable to be in a room without any sound at all. Thus we name it noise even though it in some cases are wanted.).
  - Unpredictable - but not always. A completely smooth tone will be very predictable but still be considered as noise.
- Electronic noise:
  - Unwanted (subjective?).
    - Prevents us to perceive the weakest signals. Limits the resolution we may achieve.
    - May be desirable in random number generators and in some measuring systems.
  - Unpredictable/random (subjective?)
    - Unpredictability is emphasized more when it comes to electrical noise. While acoustic noise can be unpredictable, (real) electrical noise normally will be.
    - This does not imply we cannot say anything statistically about the noise amplitude and frequency characteristics. But we will not be able to predict an exact noise amplitude at some time into the future.
    - Further analysis may show that what seems to be unpredictable actually is not. Say, by synchronising with 50Hz main power lines the noise may be predictable. Also, fixed pattern noise (FPN) in image sensors is rather predictable.

Electronic noise – Acoustic/visual noise

- While the acoustic noise is limited to the frequency range perceived by the human ear (20Hz-20kHz) the electronic noise will be over the entire frequency range of electronics (1aHz-10THz).
- Electronic noise may be perceived as sensed noise when converted into sound or image, say if we amplify the noise and output it on a speaker or a TV-monitor.
- The “snowstorm" we are watching on (old analogue) TV receivers with a weak antenna signal, is the electronic noise in the preamplifier. If this noise did not exist, we could receive a TV signal infinitely far away with a very small amount of energy.

Noise in general

- Noise is "random" electronic charges that comes in addition to the predictable signal. With repeated measurements with the exact same setup/inputs the difference between each measured value and the average is the noise. Due to noise the measured signal will not be exactly as expected from simulation/calculation. (Nonlinearity in components is not considered as noise.)

YELLOW: Equations

$$V(i) = V_{SIM} + V_{DC} + V_{Noise}(i)$$

$$V_{AVG} = \frac{1}{n}\sum_{i=0}^{n} V(i) = V_{SIM} + V_{DC}$$

$$\sum_i V_{Noise}(i) = 0$$

V(i) is measurement i in a series of n identical measurements. The measured value is the simulated value, a stable DC-offset (due to model errors, production variations etc.) plus the noise.

- When we simulate voltage at a circuit output, the simulator will be able to find the results with many digits of accuracy. It will then look like the circuit can handle extremely small signals and signal changes. However, when we make the circuit and look at the output with an oscilloscope, we will see that the signal is not a sharp line. The signal is subject to noise.

SNR improvement

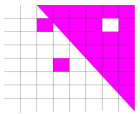
If we want to improve the accuracy of a measured signal (SNR: signal-to-noise-ratio) there are two major strategies we may follow:

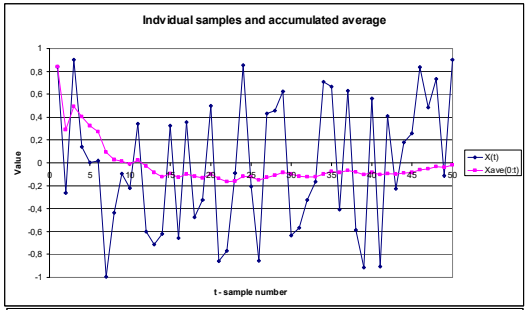
1: Single sample (SS) improvement. We improve the quality of each individual sample through improvement of sensor and front-end electronic design. This is important if the signal is "unpredictable", constantly changing and not repetitious.

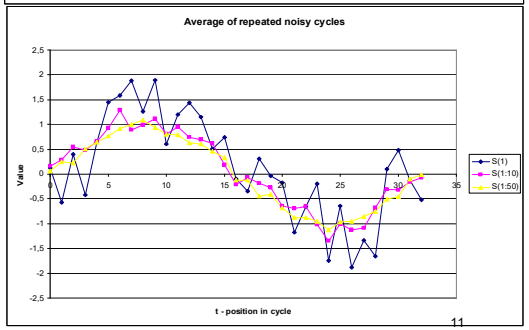
2: Multi sample (MS) improvement is achieved by combining data from several single samples. To do so we need both i) multiple samples, and ii) added information. The added information may be knowledge about possible shapes the signal may take and how the sampled values are related. Such information may be that the signal is a modulated communication signal and what possible states it may take. Another information may be that it is neighbour pixels in an image/video.

Examples of noise reduction through repeated sampling.

- Upper figure: DC-signal with random noise (dark blue). The average value of all previous values (pink) will approach the DC-value as the number of samples increases and the noise to signal ratio will be reduced.
- Bottom figure: The same can be done if the signal has another shape (here: sinus) and we know the possible shapes and frequency the signal may take.
- NB! If the noise is a periodic signal with a frequency equal to or an integral multiple of the signal frequency, the noise will not disappear.
- Image: Neighbouring pixels in space
- Video: Neighbours in space and time
- Identify moving structures

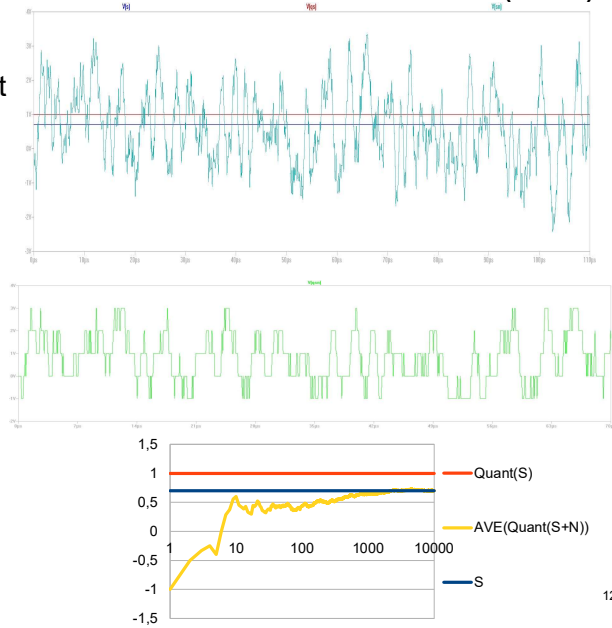






Noise may improve resolution in MS! (Dither)

- A noiseless signal of 0.7 lsb (least significant bit) will always give the same lsb and a resolution of 1 lsb
- MS with sufficient added noise will give a sequence of values. The average will have a resolution better than 1 lsb.
  - **S: Signal, N: Noise**
  - **Quant(isation): Nearest integer,**
  - **AVE: Average**



SNR, standard deviation and bits

- SNRimp (improvement)

$$SNRimp_{tot} = SNRimp_{SS} \cdot SNRimp_{MS}$$

YELLOW: Equation

- The noise standard deviation and SNR are inverse

$$SNR = \frac{1}{\sigma} k_A \Rightarrow \sigma = \frac{1}{SNR} k_A$$

- The SNR is proportional to 2 to the power of bits resolution

$$SNR = 2^n k_B \Rightarrow n = \frac{\log(SNR/k_B)}{\log 2} = \frac{\log SNR}{\log 2} + k_B^{'}$$

Energy for SS improvement

- Analog

$$V_{RMS} = \sigma \sim \frac{1}{\sqrt{I}} \Rightarrow$$

$$E_A \sim I \sim \frac{1}{\sigma^2} = \left(\frac{SNR}{k_A}\right)^2 = k_A^{'} \cdot SNR^2$$

$$E_A \sim SNR^2 \cdot E_{A1}$$

- Doubling (1 bit) of SNR improvement requires four times the energy

- Digital

$$E_D \sim n \cdot E_{D1} = \frac{\log SNR}{\log 2} \cdot E_{D1} + k_B^{''}$$

- Doubling (1 bit) of SNR improvement requires (n+1)/n times the energy

Energy for MS improvement

$$\sigma_m = \frac{1}{\sqrt{m}} \sigma \Rightarrow m = \left(\frac{\sigma}{\sigma_m}\right)^2 = \left(\frac{SNR_m}{SNR_1}\right)^2$$

- m: number of samples
- σ: Standard deviation for one sample
- σ_m: Standard deviation for *m* samples
- Making σ half requires four times *m*.

$$E_M \sim m \cdot E_{M0} = \left(\frac{SNR_m}{SNR_1}\right)^2 E_{M0}$$

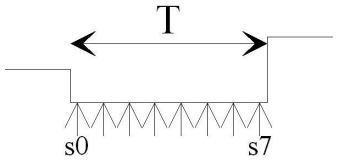
- Energy linear with *m*.

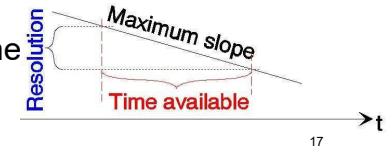
SS & MS energy summary

- To keep it very simple:
  - Doubling SNR for a single sample requires four times the energy
  - Doubling SNR through combining more samples requires four times the energy
- Warning! This is a simplification!

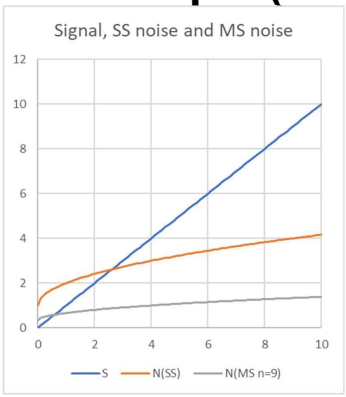
Improving SS SNR or MS SNR?

- Signal behaviour:
  - DC or long time repeatable? Free choice between SS and MS!
  - "Expensive" samples? (Say diagnostic X-ray on human beings). SS most important!
  - Stable for limited time? Trade-off between what we can achieve true SS and how much we can improve through MS.
  - Slowly changing signals? SS and MS possible. Multiple samples must be done within the available time. This time is depending on the maximum slope and the requested resolution.

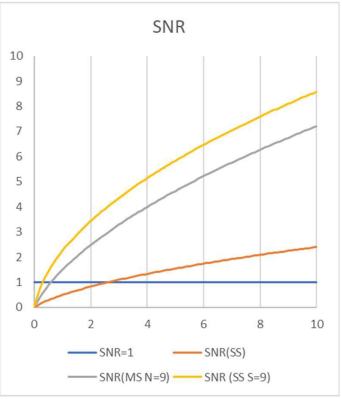




SNR for single sample (SS) and multi-sample (MS)



Typically noise increases with signal strength. However stronger signals has better SNR than weaker.



By combining samples we may measure below the SS noise floor.

Measurement noise sources and noise reduction

Possible noise sources

1. Physical phenomena to be measured
2. Sensor
3. Electronics

Noise reduction in electronics:

- Add "minimum" noise in the electronics (3)
- Select system architectures that minimize the noise from 1 and 2

Source noise example: Photon noise

- Example: Photon noise (light, x-rays etc.)
  - Signal: S
  - Noise: N = √S
  - SNR = S / N = S / √S = √S

  I.e. the SNR increases with the square root of the signal. If the signal increases by 100 the SNR increases by 10.

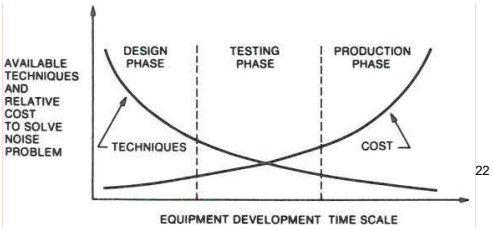
Photon noise (camera)

	ISO 100	ISO 200	ISO 400	ISO 800
A	A_{100}	2 A_{100}	4 A_{100}	8 A_{100}
#N	N_{100}	(1/2) N_{100}	(1/4) N_{100}	(1/8) N_{100}
Signal-strength/ pixel	S	2S	4S	8S
Noise/ pixel	$\sqrt{S}$	$\sqrt{2S}$	$\sqrt{4S}$	$\sqrt{8S}$
SNR	$\frac{S}{\sqrt{S}}$	$\sqrt{2}\frac{S}{\sqrt{S}} \approx 1.4\frac{S}{\sqrt{S}}$	$2\frac{S}{\sqrt{S}}$	$2\sqrt{2}\frac{S}{\sqrt{S}} \approx 2.8\frac{S}{\sqrt{S}}$
«Old» Film («analog») simplified.				
CMOS pixel matrix with "binning" (combining neigh-bours)				

When to implement noise reduction technologies

- The simulator can provide current and voltages with many digits of accuracy. Real inaccuracy due to noise must be estimated.
- Necessary modifications of "finished" systems are common and often due to noise problems. This gives production delays and significant additional costs. Thus, there is a need for expertise in noise.
- When designing systems that will measure small values of all types of sensors, knowledge of electrical noise is a "must".
- When creating consumer electronics, international regulations for "electromagnetic compatibility" (EMC) must be fulfilled. I.e. the system should not interfere with other electronics and should tolerate a certain amount of background noise itself.

Red: Figure



Two main classes of noise

Component noise and coupling noise.

Common for both: Both are undesirable and may degrade the measurement accuracy to below an acceptable level. Both must be reduced to an acceptable level.

"Component noise" and “coupling noise" are referred to in different books and different articles.

Regarding naming, there are several names in use within both classes:

"Component noise": "True noise", “inherent noise”, "real noise", "form specific noise", "netlist dependent noise" or "internal noise".

“Coupling noise": "Artificial noise", "layout specific" noise, “interference noise”, or "external noise".

Electronic noise hierarchy

- **Electronic noise**
  - **Coupling noise**
    - **Wired coupling**
      - **Signal lines**
      - **Power**
      - **Ground coupling/ground loops**
    - **Field coupling**
      - **Magnetic field/inductive coupling (near field)**
      - **Electric field/capacitive coupling (near field)**
      - **RF (Far field)**
  - **Component noise**
    - **Thermal noise**
    - **Flicker noise**
    - **Shot-noise**
    - **Generation-regeneration noise**
    - **Pop-corn noise**

Component noise (1/2)

Examples:
- Thermal noise
- Shot noise
- 1/f-noise or flicker noise,
- Pop-corn noise,
- R-G noise.

Input for analysis:
- Circuit schematic: elements and schematic (net list).
- Frequency information

Typical noise design target for electronic circuitry: Equal to the sensor noise level

When the component noise is simulated/estimated it will often be modelled as a voltage source or current source. In LTspice we use *.noise* analysis in the frequency domain and *.tran* with artificial sources in the time domain (or *.noisetran*).

Component noise will usually have a broad and "smooth" frequency spectre without spikes.

Examples of component noise (2/2)

⇒ Thermal noise

Noise related to the resistance in all conducting materials: Resistors, parasitic resistance in transistors, coils, capacitors etc.

In the case of impedance the thermal noise will be related to the real part of the impedance.

$$E = \sqrt{4kTR\Delta f}$$ **Red: Equation**

A function of
- temperature,
- resistance value and
- frequency bandwidth

⇒ Shot-Noise

$$I_{sh} = \sqrt{2qI_{DC}\Delta f}$$ **Red: Equation**

⇒ Flicker noise

$$I_f^2(f_l, f_h) = \frac{K_F I_{DS}^{AF}}{Cox \cdot L_{eff}^2} \int_{f_l}^{f_h} \frac{1}{f} = \frac{K_F I_{DS}^{AF}}{Cox \cdot L_{eff}^2} \ln \frac{f_h}{f_l}$$ **Yellow: Equation**

Coupling noise 1/2

Spreads by
- fields (E/M near field or RF far field) or
- common conductors.

Examples of dispersion media:
- common impedance,
- parasitic capacitance,
- parasitic inductance,
- parasitic resistance,
- capacitive coupling,
- inductive coupling (trafo),
- electromagnetic radiation.

Topics that affect this type of noise:
- screening,
- cabling,
- decoupling,
- voltage- and current supply,
- ground coupling,
- ground loops and
- substrate noise.

Coupling noise 2/2

Input for analysis:
- Layout of integrated circuit or PCB (Printed Circuit Board), types of cables, type of power supplies etc.
- Simulation results

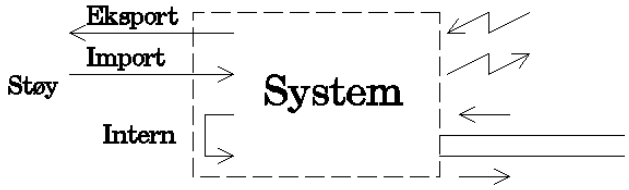
Coupling noise can almost be reduced to the level one would like ... (but it costs money, power, weight, volume etc.)
This can be achieved by additional screens, cables, decoupling, ground plane etc.

When coupling noise is simulated/estimated it will often be modelled as resistors, capacitors and coils but sometimes also as a signal generator. In LTspice we use voltage/current sources and capacitors, resistors, inductors and transformers.

The noise may have a wide frequency spectre but often some individual frequencies (“spikes”) being more dominant than others.

Noise and environment: EMC

Red:
Figure



EMC: Electro Magnetic Compatibility

Noise can be spread via cables and radiation

- Noise export: How much noise that can come out of a product and potentially disturb others. EMC rules restrict radiance.
- Noise import: External noise that may disturb the product. EMC regulations specify how much noise a product should be able to withstand.
- Internal noise: The system must be designed so that it can live with its own noise. No EMC regulations.

Temporary course plan

	Lectures (9-11)	Task/lab (11-12)	Deadlines etc.
34: 21/8	F1: Introduction		
35: 28/8	F1+: LTspice and Mandatory 1 presentation	Mandatory 1 presentation	
36: 4/9	F2: Cabling (Ott2)		
37: 11/9	F3: Cabling (Ott2)		
38: 18/9	F4: Grounding (Ott3)	Mandatory 2 presentation	18/9 08:00 Mandatory 1 deadline
39: 25/9	F5: Fundamental noise mechanisms (Mot1)		
40: 2/10	F6: Amplifier noise model (Mot2)		
41: 9/10	F7: Noise in feedback amplifiers (Mot 3)		
42: 16/10	F8: Noise in bipolar transistors (Mot 5)	Mandatory 3 presentation	16/10 08:00 Mandatory 2 deadline
43: 23/10	F9: Noise in field effect transistors (Mot 6)		23/10 08:00 Mand 3, amplifier
44: 30/10	F10: System noise modelling (Mot 7)		
45: 6/11	F11: Sensors (Mot 8)/NEMKO?		
46: 13/11	F12: Low noise design methodology (Mot 9)		13/11 08:00 Mandatory 3 deadline
47: 20/11	F13: Amplifier design (Mot 10)		
48: 27/11	Alternative day		
50:	Oral exam in week 49 or 50		

Literature

Syllabus

[1] C.D. Motchenbacher, *Low-Noise Electronic System Design,* John Wiley & Sons, 1993, ISBN 0-471-57742-1 (Component noise) (Chapter 1,2,3,5,6,7,8,9,10)

[2] Lectures and lecture notes

Additional literature:

[3] H.W. Ott, *Electromagentic Compatibility Engineering,* John Wiley & Sons, 2009, ISBN 978-0-470-18930-6. (Coupling noise)

For those especially interested

[A] Agnar Grødal, *Elektromagnetisk kompatiblitet for konstruktører,* Tapir forlag, 1997, ISBN 82-519-1271-7

[B] Z.Y.Chang etc, *Low-Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies*, Kluwer Academic Publishers, 1991, ISBN 0-7923-9096-2

[C] A.v.d. Ziel, *Noise in Solid State Devices and Circuits*, John Wiley & sons, 1986, ISBN 0-471-83234-0

[D] Behzad Razavi, *Design of Analog CMOS Integrated Circuits,* McGraw-Hill, 2015, ISBN 0-07-238032-2 (in particular chapter 7)

[E] Tim Williams, EMC for Product Designers, Elsevier Ltd, Oxford, GB, 2010, ISBN 978-0-75-068170-4.

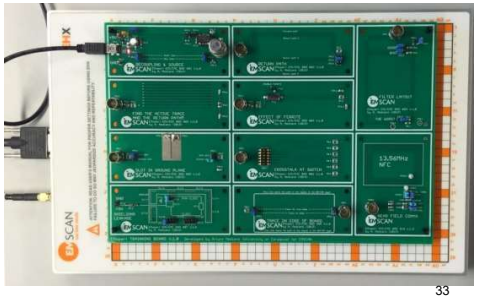
Mandatory assignments

- Assignment 1: Introduction to LTspice and Simulation of coupling noise (On any PC)
- Assignment 2: Measurement of EM-noise on PCB with EM-scanner (In lab)
- Assignment 3: Component noise (On any PC)

Measurement in lab

- EM-scanner (Electrical and Magnetic field) scanner
  - For PCBs, cables and ASICs
  - 150kHz-8GHz
  - 60µm-7.5mm
- IN5230: PCB with 10 sub circuits

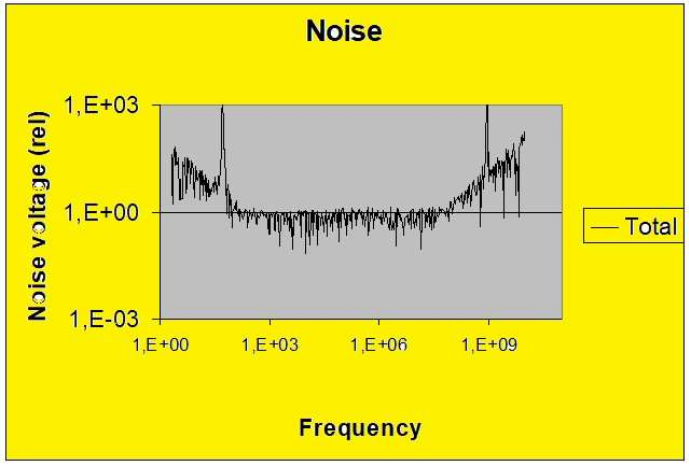




Mandatory assignments

- Three compulsory assignments (one on measuring and two on simulations). The last is larger than the preceding ones.
- The two simulation exercises are schematic drawing and simulations tasks performed using the LTspice simulator from Linear Technologies. This is a free simulator that you download yourself.
- The report should be submitted as a PDF file
- The reports have to contain complete schematics (with forces and inputs), simulation results and comments/reviews of these.
- NB! Submission deadlines and what should be submitted is strict. Ensure you are updated.

Noise example



Yellow: Figure

- The figure illustrates the noise from a mixture of physical and artificial noise sources

Power supplies

- Power supplies influence on noise
  - As noise sources
  - As noise attenuating elements
- Two main types of power supplies
  - Linear regulators
  - Switch-mode regulators

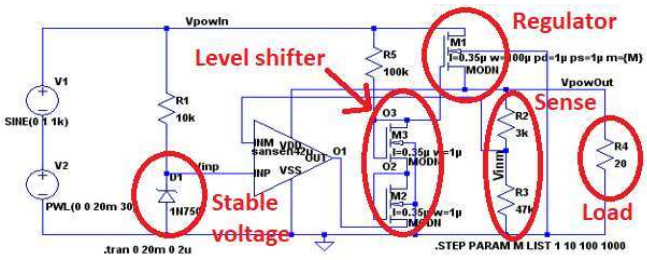
Linear voltage regulator

Advantages:

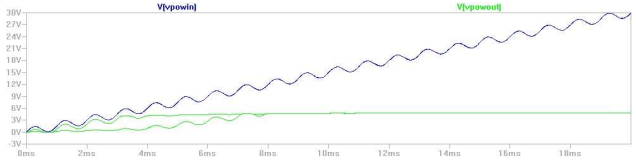
- Very stable output voltage (also without use of capacitance)
- Self supplied
- Works independently from start-up.

Disadvantage:

- Power dissipation in regulator is linear with load current



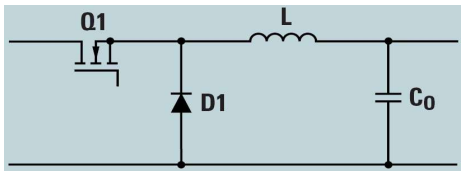
LinRegTsTvs

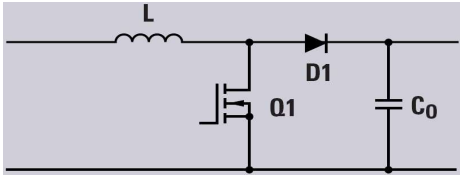


$$P_{tot} = P_{reg} + P_{last} = (V_i - V_o)I_o + V_o I_o$$

$$P_{reg} = \Delta V \cdot I_O = (V_i - V_o)V_o / R_L$$

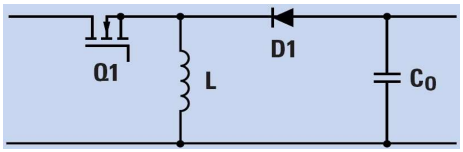
Switch-mode voltage supply: Buck, Boost and Buck&Boost





D (0:1] is the duty cycle of Q1

- Buck: Vo/Vi=D
- Boost: Vo/Vi=1/(1-D)
- Buck&Boost (inv): Vo/Vi=-D/(1-D)



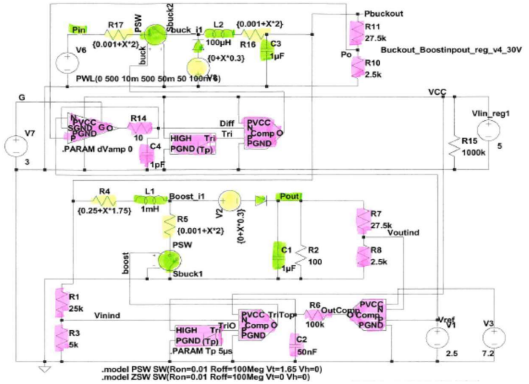
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University of Oslo

Switch-mode voltage supply

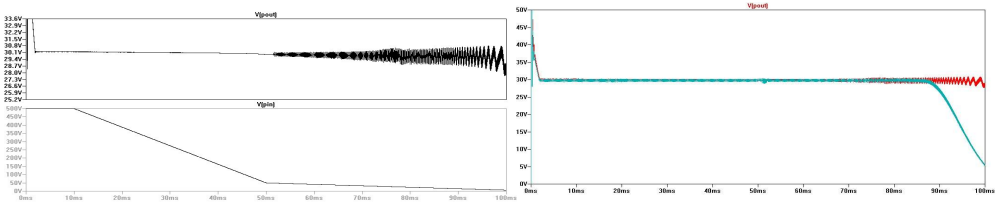
- Advantage:
  - Energy efficient: Ideally no energy loss
- Disadvantage:
  - More output noise than for the linear regulators
  - Needs start-up help
  - Large decoupling capacitors to remove ripple
  - Trade-off: fast start-up ⇔small ripple
  - Transistors: Challenge to design switch transistor gate drivers
- Some examples of classes:
  - Buck for voltage reduction,
  - Boost for voltage increase and
  - Buck & Boost-architectures when the input voltage can be both above and below the output voltage.

Serial buck and boost

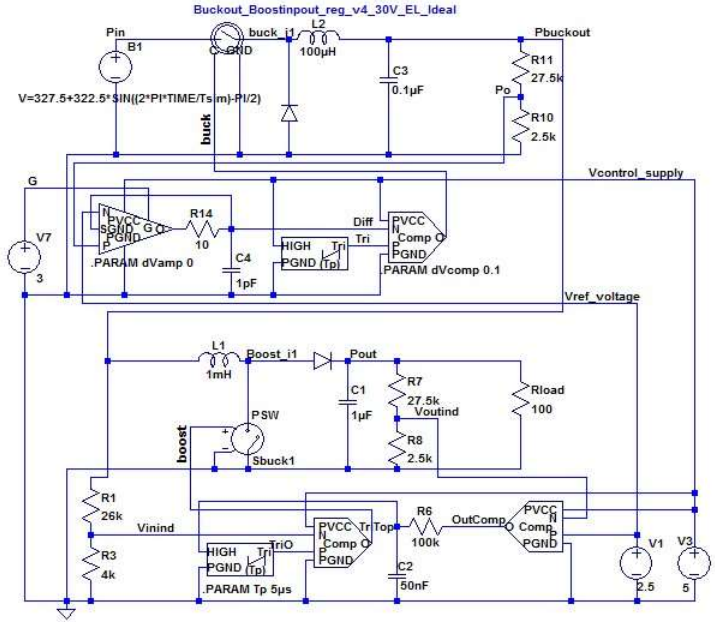
- Vin⇒Buck⇒Boost⇒Vout
- Colour code:
  - Green: main components,
  - Pink: regulators,
  - Beige: parasitic
- Figures
  - Under left: Output and input without parasitics
  - Under right: Output with and without parasitics
- Inputs with ramp shape



Buckout_Boostinpout_reg_v4_30V

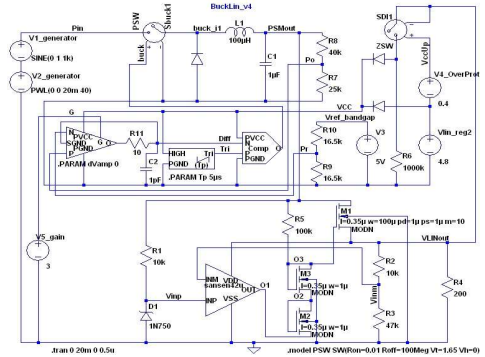


Serial bock and boost

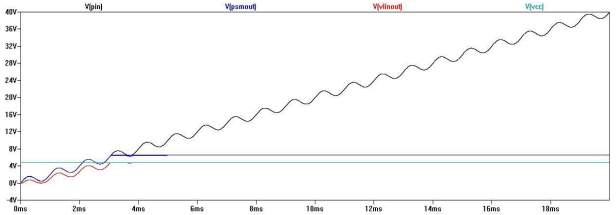


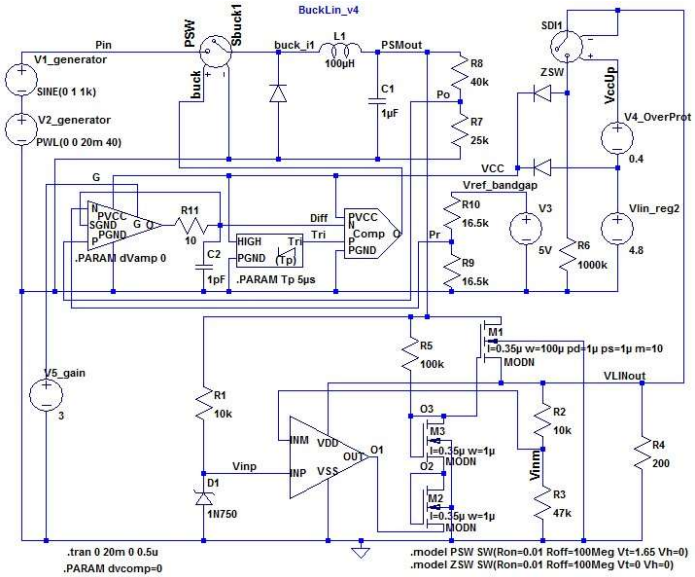
Combined buck-linear

- The buck ensures an energy effective voltage shift down to a level somewhat above the desired output voltage
- The linear regulator offers a more stable output voltage somewhat below the voltage offered by the switch regulator.
- No/little need for capacitance



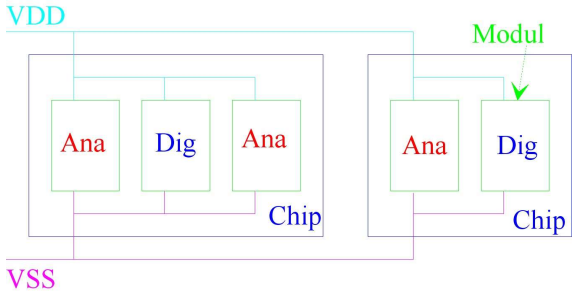
BuckLin_v4

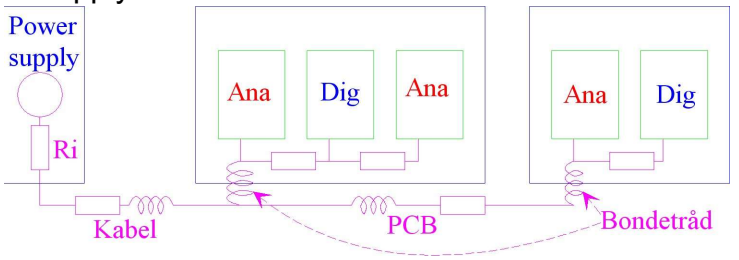




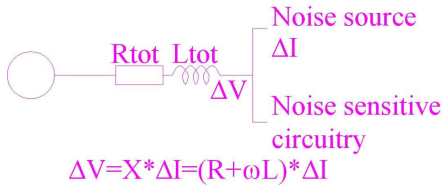
Noise on supply lines

- Upper figure: An ideal system of circuits and interconnects without unwanted parasitic elements.
- Lower figure: Parasitic resistance and inductance has been drawn for the VSS supply line.





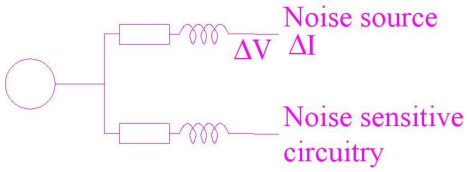
Noise on supply voltage



- Problem: Some elements draw power unevenly. It causes variation in the supply voltage/current level. (This also applies to ground.)

- Improvements with present network
  - Reduce ΔI? (Vsup, a more smooth current consuming logic family, asynchronous logic)
  - Reduce R?
  - Reduce L?
  - Reduce f?
- Improvements through modification of network
  1. Split in several branches
  2. Low impedance decoupling close to sensitive electronics

Several branches



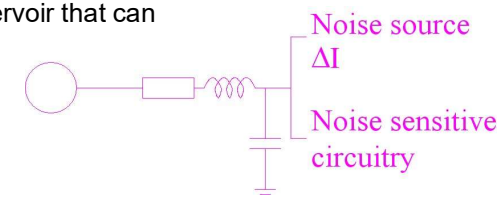
1. Split in several branches

- For example independent supplies for:
  - Preamplifiers
  - Other analogue circuitry
  - Digital circuitry

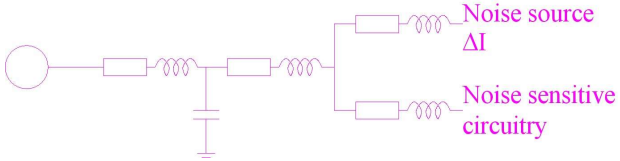
Decoupling

2. Low impedance decoupling close to sensitive circuitry

The decoupling capacitor is a charge reservoir that can compensate uneven charging due to ΔI



If there is no resistance and/or inductance between a huge capacitor and the circuitry, ripple can in theory be completely removed. However, as illustrated on the bottom figure, there will always be parasitic resistances and inductances. To reduce the effects of these it is important to position the decoupling capacitor as close as possible to the sensitive circuitry.



Signal edge spectrum

Yellow: Figure

- CMOS current noise: Triangular shape
- FFT
  - Low f: Period
  - Higher f: Edges
- Edges
  - Decrease with 40dB/decade above 1/(πtr)
  - Less than half of the energy below 1/(πtr)

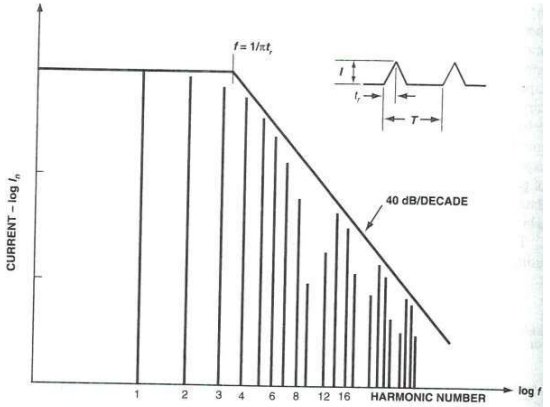
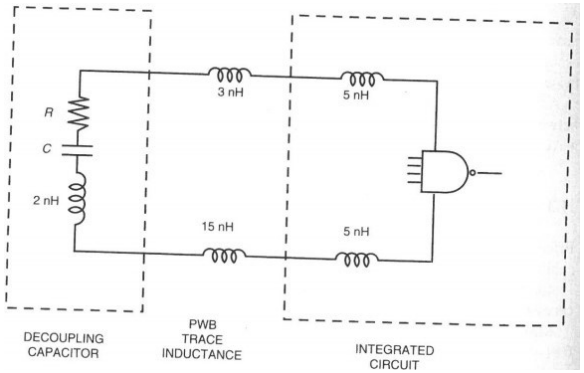


FIGURE 11-4. Envelope of Fourier spectrum of an isosceles triangular wave.

Decoupling - Typical inductances

Yellow: Figure

Standard has been for almost 50 years to add a 10nF or 100nF decoupling capacitor. For today's frequencies above 50 MHz this is not sufficient, due to parasitic inductances of 10-40nH. Now an added capacitance has to be considered as a LC-element.

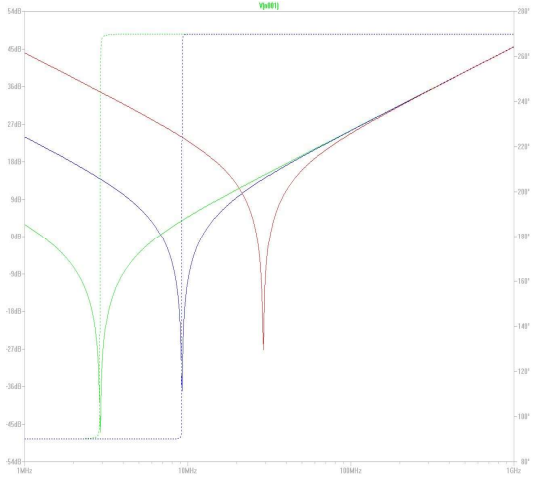


- **SMT (surface mounted): 1-2nH**
- **PCB trace: 5-20nH**
- **IC leadframe: 3-15nH**

Decoupling - Three different capacitors

Yellow: Figure

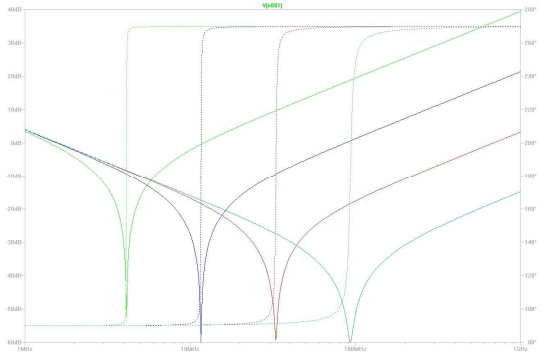
- 100nF&30nH⇒3MHz
- 10nF&30nH⇒9MHz
- 1nF&30nH⇒29MHz
- It is possible to tune the dip to a specific frequency below 50MHz
- Above 50MHz the 30nH dominates, independent of the capacitance value.
- Making 30nH half would only increase *f* by 1.41.
- Above 50MHz a single capacitor is not sufficient!
- (Dot'ed curves are phase)



100nF, 10nF,1nF

Decoupling - Equal parallel capacitors, 100nF

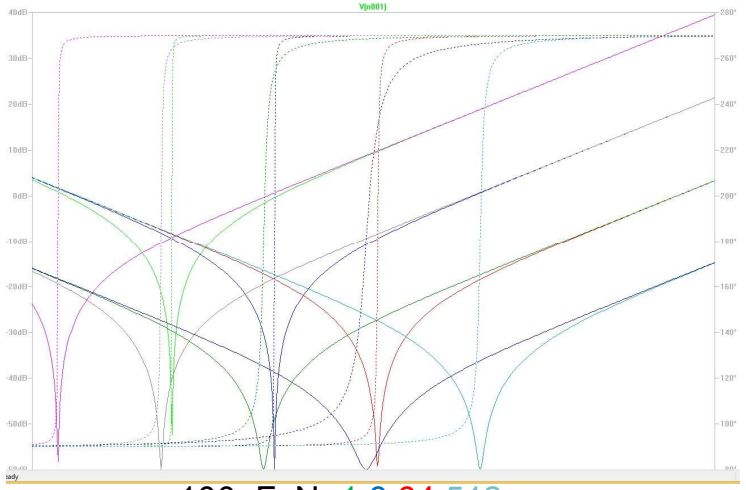
- Inductance
  - Difficult to reduce for one line
  - Reduction through multiple in parallel
- Example N capacitors in parallel
  - Total capacitance 100nF
  - Effective inductance 30nH/N



Yellow: Figure

- N=1,8,64,512

Decoupling - Equal parallel capacitors, 100nF&1µF

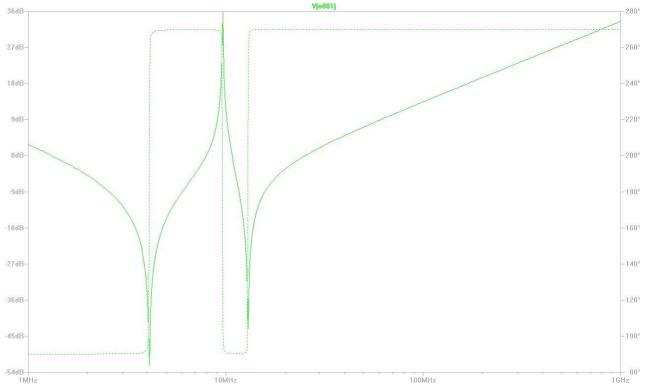


- 100nF, N=1,8,64,512
- 1µF, N=1,8,64, 512

Yellow: Figure

Decoupling - Two different capacitors

- Two capacitors
  - Both 15nH
  - One 100nF
  - One 10nF
- Three regions
  - Low: Both capacitive
  - High: Both inductive
  - Middle:
    - 100nF⇒Inductive
    - 10nF⇒Capacitive
    - ⇒Resonance spike



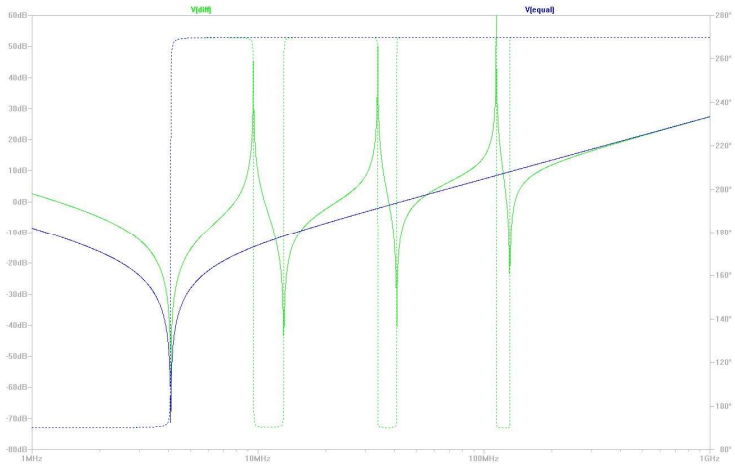
Yellow: Figure

- Resonance spike may pick up noise

Decoupling - Four different and four equal

Yellow: Figure

- 2x4 cap
- Each 15nH
- "Diff":
  - 100nF,
  - 10nF,
  - 1nF,
  - 100pF
- "Equal":
  - 4x100nF



⇒Equal capacitors are more predictable

Decoupling - Example 1/3

- Frequencies from:
  - Triangular edges decreases -40dB pr decade above corner frequency,
  - decap increases 20dB pr decade in inductive region.
- ⇒ Gives total decrease of -20dB/decade.
- Have to ensure low enough impedance until triangular frequency.

- Strategy: *N* equal capacitors.
- Example values:
  - Current spikes of 2.5A.
  - Voltage supply of 5V which shall be kept within 5% by the use of decoupling capacitors.
  - Current spike rise and fall time found to be 2ns.
  - Low frequency corner is 2MHz.

Decoupling - Example 2/3

$$Z_t = \frac{kdV}{dI} = \frac{2 \cdot 250mV}{2.5A} = \frac{500mV}{2500mA} = 0.2\Omega \text{ (Ott Eq 11.8)}$$

- Upper frequency decided by inductance i.e. number of capacitors:

$$n = \frac{2L}{Z_t t_r} = \frac{2 \cdot 10nH}{0.2\Omega \cdot 2ns} = 50 \text{ (Ott Eq 11.7)}$$

  - L: Inductance of each capacitor = 10nH
  - tr: Rise time/fall time=2 ns
  - Zt: Low frequency target impedance
  - K: 2

- Lower frequency decided by total capacitance:

$$\frac{1}{\omega C} \le Z_t$$

$$C = \frac{1}{Z_t \cdot 2 \cdot \pi \cdot 2MHz} = 400nF$$

$$C_u = 400nF/50 = 8nF \Rightarrow 10nF$$

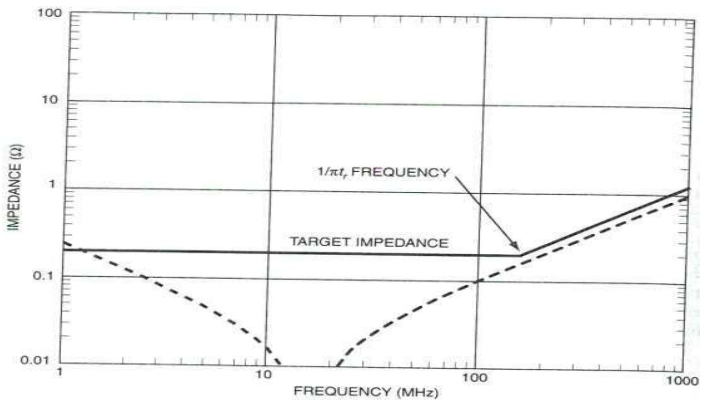
- Upper frequency corner

$$f = \frac{1}{\pi \cdot t_r} = \frac{1}{\pi \cdot 2ns} = 159MHz \text{ (Fig 11.4)}$$

Decoupling - Example 3/3: Resulting behaviour

Red: Figure

- 50x10nF



- Solid line: Requirement
- Dashed line: Expected capacitor behaviour

Typical parasitic values

Typical numbers:

Resistance on chip:

30mΩ/sq · (1cm+1cm)/30μm=2Ω

Inductances:

Bonding wire:10nH

IC leadframe: 3-15nH

Surface mounted cond.: 1-2nH

PCB trace: 5-20nH

Electrolyte cap.: 25nH

Disc cond.: 4-6nH

Coax 50Ω:

250nH/m, 100pF/m

Examples of generated noise:

1)

ΔI=100μA (Small!)

∑R=10Ω

⇒ ΔV=1mV over resistance

2)

ΔI=100μA

L=250nH

Tr=50ns ≈ f=10MHz

$\Delta V = X_L \cdot \Delta I = \omega L \cdot \Delta I = 2\pi F \cdot \Delta I = 1.6mV$

⇒ ΔV=1.6mV over inductance

Is 1mV or 1.6mV a problem?

In a sensitive sensor system: Yes

In a digital system: No

However careless digital design may result in: ΔI=10mA, R=50Ω ⇒ΔV=500mV. If the threshold is low this noise level may become a problem.

If the frequency is increased to 100MHz we will have ΔV=16mV.

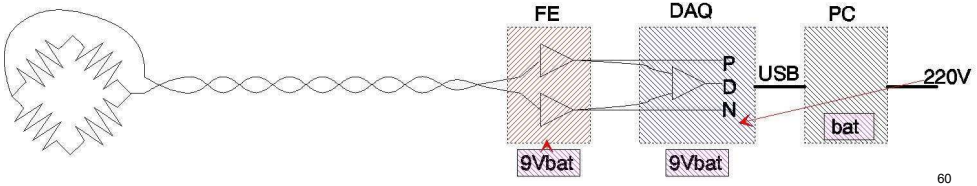
Frequency above 1GHz

REMEMBER: The wave length at 300MHz is 1 meter.

A 1m long coax may be considered as a capacitor and an inductance at frequencies below 300 MHz but as a 50Ω resistance at frequencies over 300MHz. (The last case assumes correct cable termination.)

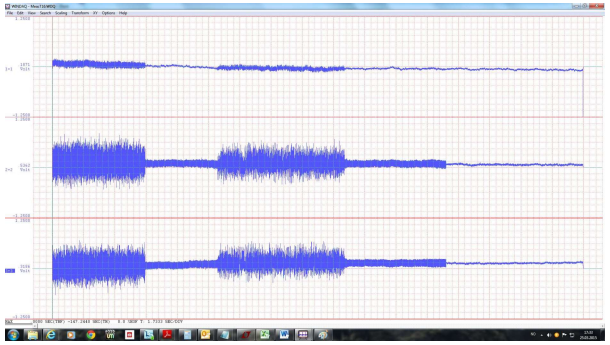
Example: Power noise in sensor system 1/7

- The system consists of
  - Wheatstone balanced bridge sensor
  - Long twisted-pair sensor wire
  - Gain Front End (FE) supplied by 9V battery
  - Commercial DAQ sampling and ADC module that may be supplied from: i) 220V through the PC usb-connection, ii) from the PC battery, iii) 220V from private adapter, iv) from a private 9V battery bank
  - PC, supplied from 220V or private battery
- P, N and their difference D are sampled sequentially.



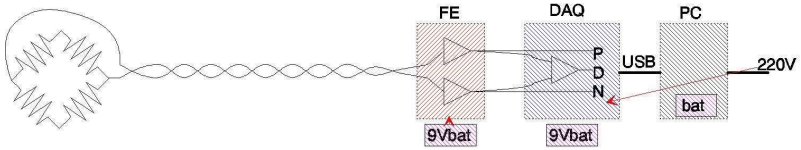
EX: Different DAQ power supplies 2/7

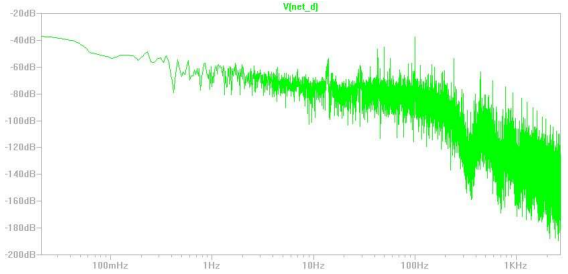
- Measurement
  - Signals from top: D, P and N
  - Five DAQ supply set-ups:
    - 1: From 220V (through PC and USB)
    - 2 & 4: From PC battery
    - 3: From 220V private adapter
    - 5: From 9V battery cluster



- Sampling of the differential signal gives less noise than P and N individually except for the last set-up. With a 9V cluster the noise is at a minimum.

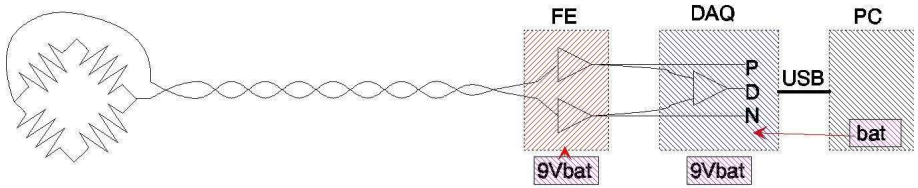
EX: 220V PC source 3/7

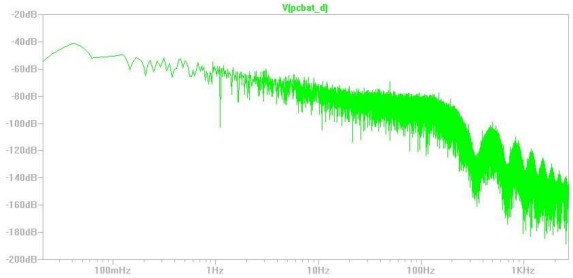




- DAQ powered from 220V through PC and USB.
- Several significant spikes like 50Hz and 100Hz.
- (-45dB@50Hz).

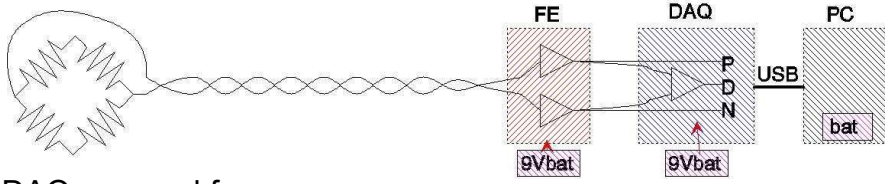
EX: PC battery source 4/7

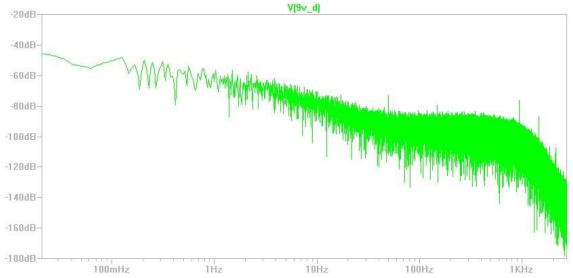




- DAQ powered through USB from PC battery
- Spikes reduced but «Wave» pattern remains.
- (-69dB@50Hz)

EX: Private battery 5/7

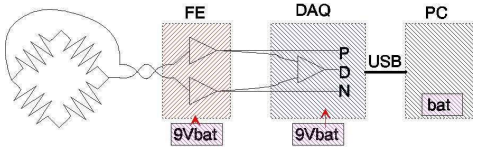


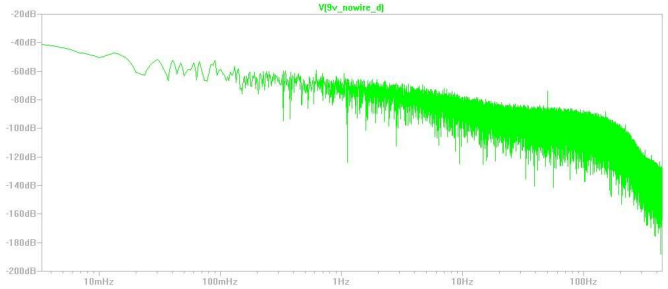


- DAQ powered from private 9V battery
- «Waves» are removed but a few spikes remain.
- 50Hz pick-up must have come through air.
- (-73dB@50Hz)

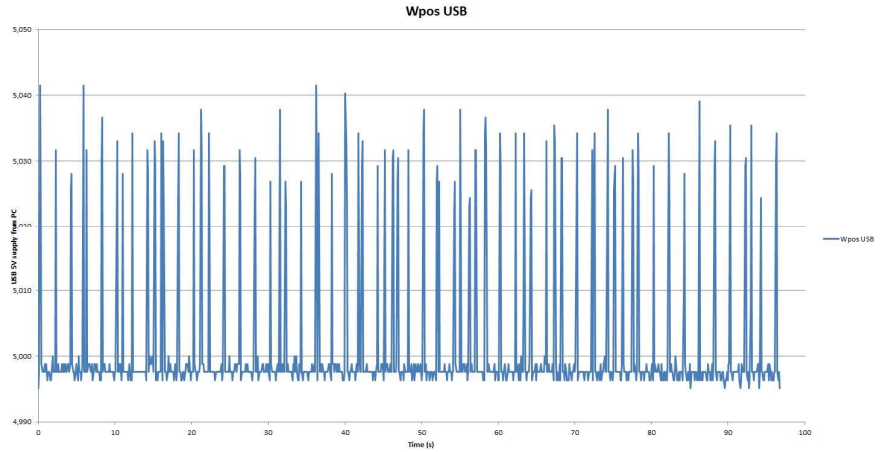
EX: All private batteries & short wire 6/7

- All private batteries
- Short sensor wire (to reduce pick-up)
- Some spikes reduced but some remain
- (-74dB@50Hz)





EX: 5V USB power noise 7/7



- Mostly 1-2mV spikes but also regular pulses above 20 mV.

Battery test

Batteries may be an alternative as a low noise power supply. Basic choices are between rechargeable and non-rechargeable batteries. There are also a choice between energy intensive or power intensive batteries. In the first case more of the volume are used for energy storing chemistry. In the latter case more of the volume are electrodes. This gives a smaller internal resistance supporting large decharge and charge currents.

In our test we have three batteries used to supply a front-end DAQ module.

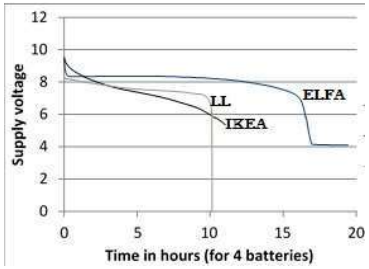
- "ELFA": A non-rechargeable Li-Ion battery from Ansmann. Energy density 24mAh/gr (=816mAh/34gr.). Price 100,- NOK per unit.
- "IKEA": An alkaline battery bought at IKEA for 9,- pr unit. Energy density 13mAh/gr (=598mAh/46gr.).
- "LL": A Li-Ion rechargeable from Litelong imported from China. Price approximately 50.- NOK per unit. Energy density 21mAh/gr (=525mAh/25gr.).

The measurement shows the battery voltage on the y-axis and the number of hours on the x-axis.

The low-end battery from IKEA and the LL rechargeable battery keeps the DAQ alive approximately 10 hours while the battery from Ansmann achieves 16 hours. For all cases with four batteries in parallel.

If low price is important the LL is preferred since it can be recharged many times. If recharging is a problem the IKEA has the lowest price. If low weight is important Ansmann has highest energy density followed by Litelong and with IKEA at last. For a short time the IKEA battery has the highest voltage but then falls under the others. The two Litium based batteries maintain the voltage for a longer time.

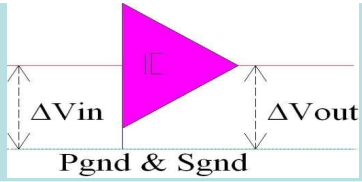




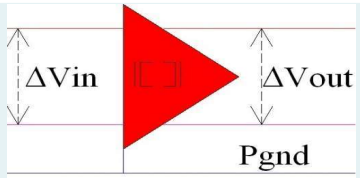
Signal reference

Yellow: All figures

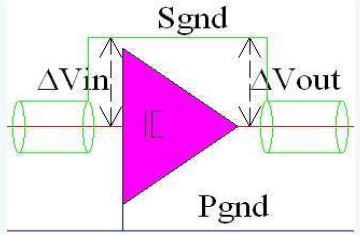
Low precision: Signal refers to shared power and signal ground. Noise on power influence on signal value.



Medium precision: Differential signalling with no signal ground. High immunity to common mode coupling noise. A more complex amplifier gives more internal noise.



High precision: Signal refers to private signal ground (Sgnd). Low internal noise contribution from amplifier. Trust heavily on proper shielding for protection towards coupling noise.



PSRR (Power Supply Rejection Ratio)

To determine the signal sensitivity to supply noise we must:

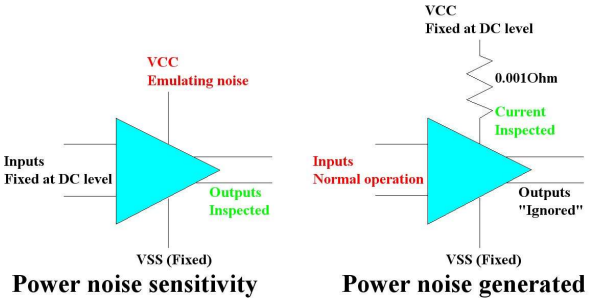
1. Find the noise sensitivity
2. Find the noise contribution from all modules connected to the supply

1. Noise sensitivity:
   - Linear and non-clocked circuitry: AC-analysis
   - Un-linear or clocked circuitry (say switch cap and mixers): The frequency characteristics are established through a number of transient analysis

2. Noise contribution:

   Simulate the variation in current consumption for all modules connected to the same power

Yellow: Figure



Conventional simulation modes 1/3

- DC-analysis
- AC-analysis (Frequency/small-signal analysis)
- Transient analysis (Timing analysis)

DC-analysis:
Voltage and currents are set by the initial value at 0 ns. Coils are short circuited (0 Ohm) and capacitors removed (∞ Ohm). All other simulation modes start with an DC-analysis.

AC-analysis (frequency mode):
The offset value (DC-value) of the input signal decides the simulation equations and parameters to be used. This mode gives the response of a infinitesimal small AC-signal. (Will not turn on/off switches, trigger latches etc.)

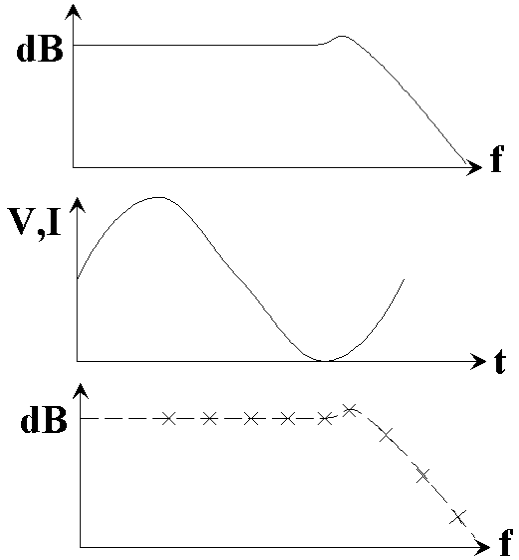
Transient analysis (time mode):
The simulation equations and parameters are chosen based on the actual voltage and current at every point of time.

Simulation modes 2/3

AC-simulation:
Simulation in the frequency domain.

Transient simulation:
Simulation in the time domain

Frequency behaviour based on multiple transient simulations



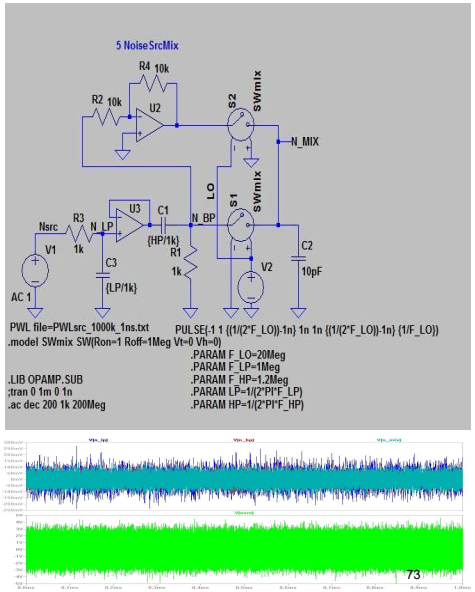
Exercise 3/3

Amplifier with a gain equal to 100. High supply is 5 Volt and low supply is 0 Volt. Input signal with offset 2.5 Volt and amplitude 1 Volt.

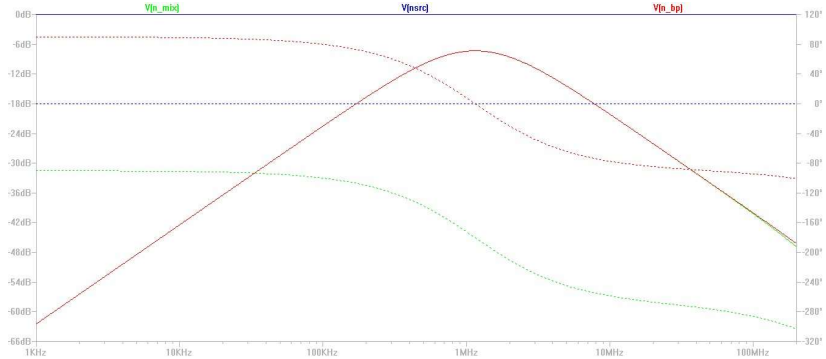
What will the output signal be if we do:
- an AC-analysis?
- an transient analysis?

Mixer: Noise example 1/3

- Mixer: ω1,ω2⇒(ω2-ω1), (ω2+ω1), {(3ω2-ω1), (3ω2+ω1)}… etc.
- Frequency mode simulation does not work well in clocked architectures like mixers. Instead we have to use timing analysis.
- Schematic:
  - Noise source (from file)
  - Band pass filter
  - Signal inverter
  - Two phase mixer

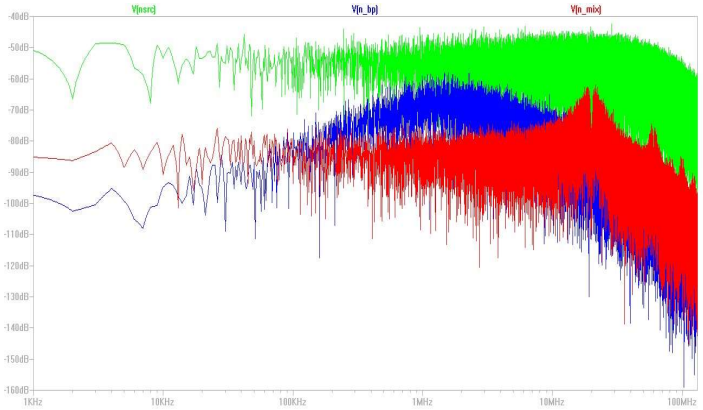


Mixer: Frequency analysis 2/3



- Frequency analysis does not “understand” the mixer. We will only see the effect of the bandpass filter. We will not see the frequency products generated by the mixer.

Mixer: Timing analysis 3/3



- Here we have done timing analysis. As a signal source we have used a wide band noise source.

  Green: FFT at the noise source (flat/white spectre)

  Blue: FFT after the band pass filter

  Red: FFT after the Mixer. We can see clearly the two (compressed) tops on each side of the mixer frequency.

2 Cabling (Ott)

2.1 Capacitive Coupling
2.2 Effects of shield on capacitive coupling
2.3 Inductive coupling
2.4 Mutual Inductance coupling
2.5 Effect of shield on Magnetic coupling
2.5.1 Magnetic coupling between shield and inner connector
2.5.2 Magnetic coupling – Open wire to shielded conductor
2.6 Shielding to prevent Magnetic radiation
2.7 Shielding an receptor against magnetic fields
2.8 Common impedance shield coupling
2.9 Experimental data
2.10 Example of selective shielding
2.11 Shield transfer impedance
2.12 Coaxial cable versus twisted pair
2.13 Braided shields
2.14 Spiral shields
2.15 Shield termination (pigtails)
2.16 Ribbon cable
2.17 Electrically long cables

2.1 CAPACITIVE COUPLING

Two conducting materials ⇒ capacitive coupling

Model for capacitive coupling : Capacitance

Capacitor:

$$C = \varepsilon \cdot \frac{A}{t} \qquad C = \frac{dQ}{dV}$$

2.1 Two-wire capacitive coupling

Red: Figure

- Wire 1 is a noise source while wire 2 is the noise receiver.
- V_1: Voltage on conductor 1 (Noise source)
- V_N: Voltage on conductor 2 from 1 (Received noise)

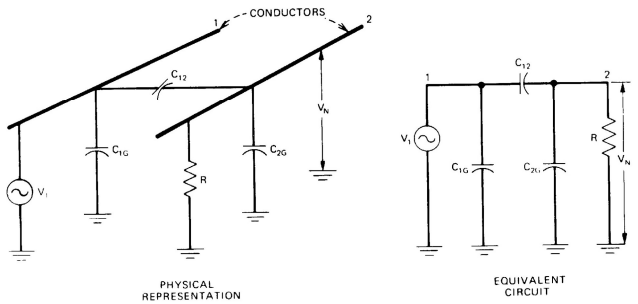


Figure 2-1. *Capacitive coupling between two conductors.*

$$V_N = \frac{X_{C_{2G}} \parallel R}{X_{C_{2G}} \parallel R + X_{C_{12}}} V_1$$

$$\frac{\frac{1}{j\omega C_{2G}} \cdot R \Big/ \left(\frac{1}{j\omega C_{2G}} + R\right)}{\frac{1}{j\omega C_{2G}} \cdot R \Big/ \left(\frac{1}{j\omega C_{2G}} + R\right) + \frac{1}{j\omega C_{12}}}$$

2.1 Split analysis in two cases

$$V_N = \frac{j\omega\left[C_{12} / \left(C_{12} + C_{2G}\right)\right]}{j\omega + 1/\left[R\left(C_{12} + C_{2G}\right)\right]} V_1$$

We will split our analysis in two cases depending on the denominator.

1. $1/[R(C_{12}+C_{2G})]$ (real) is larger than ω (imaginary)
2. The real part is smaller than the imaginary part

2.1x Case 1 (real denominator)

$$V_N = j\omega R C_{12} V_1 _ when _ R << \frac{1}{j\omega\left(C_{12} + C_{2G}\right)}$$

Red: Left part of equation

When is this the case for a CMOS ASIC?

Example:

Σ C = 250fF

f=1MHz

⇒R less than 600kΩ

Which R values can we have in a CMOS circuit?

CMOS input impedance: Very high

CMOS output impedance:

Conducting:	Some kΩ
Non-conducting:	Several MΩ

i.e. we are talking about a driven node!

NB! In the case of high frequencies or large total capacitance even an ordinary driven output will have too large resistance to be covered by this case.

2.1x Parasitic capacitances on an ASIC

(not included in the device models):

- Crossing metal and poly-conductors
- Parallel metal and poly-conductors
- Between wires and substrate

2.1x Some ASIC examples:

1) Power wire routed in parallel with a noisy wire in a length of 1 mm and with minimum separation distance. The noisy signal has a rise/fall time of 50 ns and toggle between 0V and 5V.

($f=10MHz$, $R=2k\Omega$, $C_{12}=100fF$, $V_1=5V$) (100fF*5V=500fC=10μA*50ns)

$\Rightarrow V_N=60mV$

2) Wide signal wire (50μm, i.e. low impedance), crossing equally wide (50μm) power wire. 20 mV noise on the power conductors with a dominating frequency of 40MHz.

($f=40MHz$, $R=2k$, $C_{12}=100fF$, $V_1=20mV$)

$\Rightarrow V_N=1mV$

(Is 1mV much?)

3) Signal wire in metal routed over a substrate with 1 mm length and 2 μm width. The substrate noise has an amplitude of 20 mV and a dominating frequency of 40 MHz.

($f=40MHz$, $R=2k$, $C_{12}=100fF$, $V_1=20mV$)

$\Rightarrow V_N=1mV$

NB ! This is a simplified model. The substrate will also have a resistor and thus a more complex filter performance!!

2.1 Case 2 (Imaginary denominator)

$$R >> \frac{1}{j\omega(C_{12}+C_{2G})}$$

When is this the case for a CMOS ASIC?

- When the node is not driven by a transistor, for example it is a dynamic memory element,
- When the frequency is high, or
- When the parasitic capacitance and/or other capacitance is large

What will the voltage be in node 2 in this case?

$$V_N = \left(\frac{C_{12}}{C_{12}+C_{2G}}\right)V_1$$

Red: Equation

The relation between the parasitic capacitance and the total capacitance in the inspected node will decide the ratio of the noise transferred.

We find from this that it is important that memory nodes have sufficient storage capacitance and little parasitic capacitance. Hence the distance from the driving source to the storage element and from the storage element to the reader should be short.

2.1 Capacitance: Width/distance

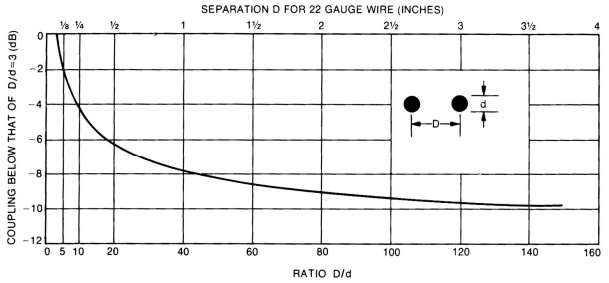


Figure 2-2. *Effect of conductor spacing on capacitive coupling. In the case of 22-gauge wire, most of the attenuation occurs in the first inch of separation.*

- The parasitic capacitance is proportional with the «area» divided by the «thickness». In the figure this is d/D. If the distance is increased the curve will have a 1/x-shape.

2.1 Two-wire capacitive coupling

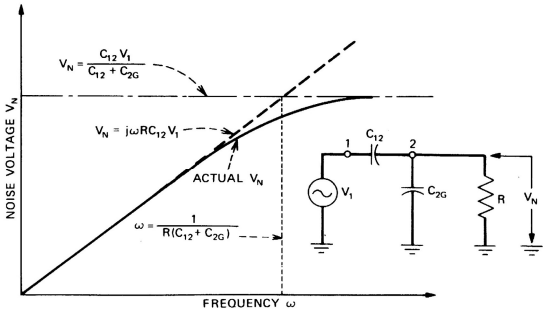


Figure 2-3. *Frequency response of capacitive coupled noise voltage.*

Red: Figure

$$\omega = \frac{1}{R(C_{12}+C_{2G})}$$

The curve shows the two cases we have analysed, the first case to the left and the second to the right.

Notice that the expression for case 2 is also an upper limit for case 1. Hence we can use case 2 as a «worst case» estimate. This may simplify the calculations if we do not know the frequency spectrum of the noise or if we do not know R.

2.2 EFFECT OF SHIELD ON CAPACITIVE COUPLING

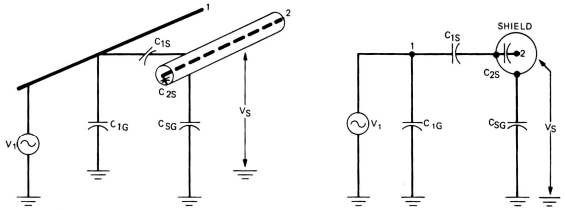


Figure 2-4. *Capacitive coupling with shield placed around receptor conductor.*

a) "Floating" screen

- Solid screen completely covering conductor 2.
- Screen (and conductor) has infinite resistance towards everything else.

$$V_S = \left(\frac{C_{1S}}{C_{1S}+C_{SG}}\right)V_1$$

Note that C_{2S} is not included.

V_S has the same potential as we found for conductor 2 earlier with infinite R resistance.

$$V_N = V_S$$

b) The screen is grounded

$$V_N = V_S = 0$$

2.2 Effect of shield on capacitive coupling

c) Screen does not cover all of the conductor

Screen grounded.

$$V_N = \frac{C_{12}}{C_{12}+C_{2G}+C_{2S}}V_1$$

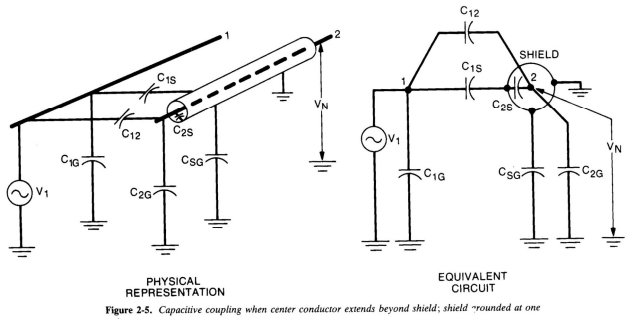


Figure 2-5. *Capacitive coupling when center conductor extends beyond shield; shield grounded at one point.*

Case 2 as discussed earlier but:

- C_{12} is reduced
- C_{2G} is increased with C_{2S}
- $\Rightarrow$ Reduced capacitive coupling

2.2 Effect of shield on capacitive coupling

d) Resistance between conductor 2 and ground

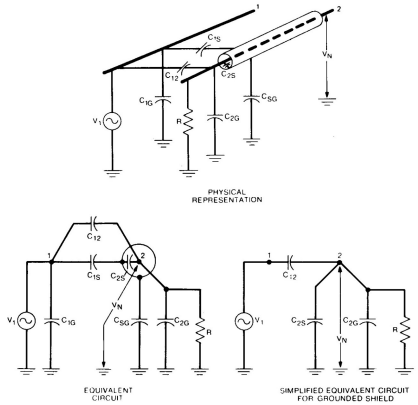


Figure 2-6. *Capacitive coupling when receptor conductor has resistance to ground.*

Like our original model but C_{2G} is extended with C_{2S}.

2.2 Case 1 and 2 with partial screen

Case 1:

$$R << \frac{1}{j\omega\left(C_{12} + C_{2G} + C_{2S}\right)}$$

The increase in capacitance C_{2S} is larger than the reduction in capacitance C_{12}. Thus the corner frequency between the two cases has decreased.

The induced noise is still:

$$V_N = j\omega R C_{12} V_1$$

But now with a much smaller C_{12}.

Case 2...

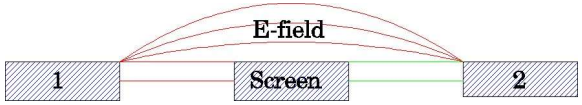
... will be as the previous case with infinite resistance.

2.2x How should the screen be…?

The main function of the screen is to reduce C_{12}. Assuming this should C_{2S} be small or large?, i.e. should the screen be close to the noise receiver or should the distance be large? Based on the previous expressions it may seem as C_{2S} should be a large as possible. However if a sensor generates a charge we want as much as possible of this to reach the preamplifier input capacitance (transistor gate). Thus it will not be desirable to have too much capacitance on the signal conductor. It may be desirable that the screen is at a certain distance from the signal conductor.

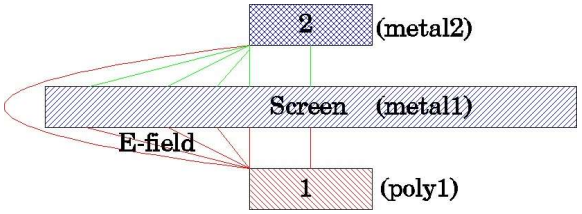
2.2x on ASICs

- Horizontal screen between conductors:



will increase the capacitance towards a stable potential C_{2G}. Limited influence on C_{12}.

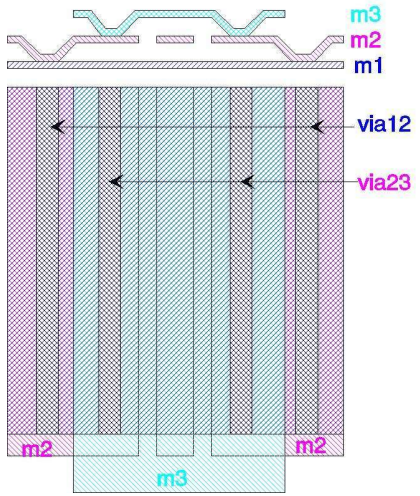
- Vertical screen between conductors:



reduces C_{12} and increases C_{2G} if the screen is wide enough.

2.2x Coax on ASIC

- It is possible to make a coax-like structure on an ASIC. To make it 100% dense on the sides long via-contacts have to be used. This violates standard design rules but the process house may allow it for this purpose.



2.2x Implementation

Crossing conductors:

If possible, put the noise sensitive wire in a higher metal layer, the noise source in a low layer and have a metal screen between.

Noise in substrate:

Estimate: Difficult. For ”worst case” estimates the substrate is considered conducting with zero resistance.

Counter measure: Wire to be protected in the highest metal layer. Screen in metal, poly or well. Well/substrate must be connected with many contacts to achieve as low resistance as possible to areas below the sensitive wire. (If possible the well should be connected to screen instead of VCC etc.)

2.2x Counter measures towards capacitive noise

1. Avoid crossing if possible
2. Minimize wire width when crossing
3. Increase distance
4. Use screen
5. Consider adding capacitance between ground and target
6. Chose isolation with lower ε_r between noise source and target
7. Reduce output impedance of line driver
8. Reduce frequency (avoid sharp edges)
9. Reduce the voltage range of the noise source
10. Generate opposite noise
11. Active shield

Red/yellow: Remember some, be able to describe all if given

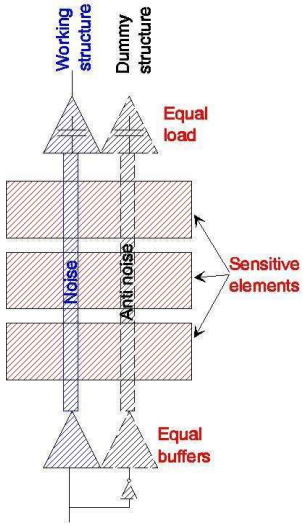
2.2x Generate opposite noise

Example:

Digital control signals have to cross an area with analogue dynamic memory elements. A voltage step of 5V on one of these lines will generate noise in the dynamic memory elements. To compensate for this we add a dummy line with the exact opposite signal. We make this as equal as possible with the same line driver and the same size of the (dummy) load.

- The voltage step and shape should be as equal as possible but in the opposite direction.
- The capacitive coupling to the sensitive cells should be as equal as possible.

Yellow: Figure



2.2x Active shield (driven guard/bootstrapping)

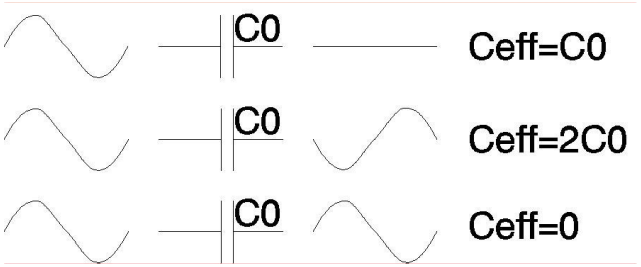
- It is very efficient for reduction of capacitive coupling and capacitive noise. It can also be used to implement a very high input impedance.
- It consists of a screen that is driven by a follow amplifier reading the signal to be protected.
- The screen is placed between the signal and other noise sources and capacitive loads. In this way they are hidden.
- When the screen has the same AC-signal as the sensed signal, the screen will effectively be invisible and the effective capacitance zero.

Active shield

- Names: Active shield/Driven guard/bootstrapping
- “Makes invisible”
- Purpose:
  - Achieve extremely high input impedance
  - Isolate from noise sources
  - Eliminate parasitic capacitive loads at input

2.2x Active shield - theory

- The effective capacitance experienced by a signal depends on the signal on the other side of the capacitor.
- If the other side is grounded the effective capacitance will be the original one. If it is in opposite phase it will be larger while it will be less if it is in phase. If the signal is equal the capacitance will disappear.



Red: Figure

Effective capacitance

Cu: Unity capacitance (when Vm=0)

Vs: (AC) signal voltage

Vm: (AC) voltage on opposite side of C

For simplicity we consider only in phase (0º) or in opposite phase (180º) with a gain |m|. $V_m = mV_s$ where $m \in R$

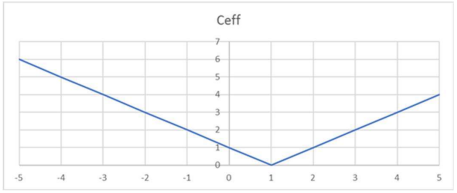
The change in charge on both capacitor plates are dQ.

$$dQ = C_u dV = C_u(V_m - V_s)$$

The S node experience this charge change over Vs which represents an effective capacitance Ceff.

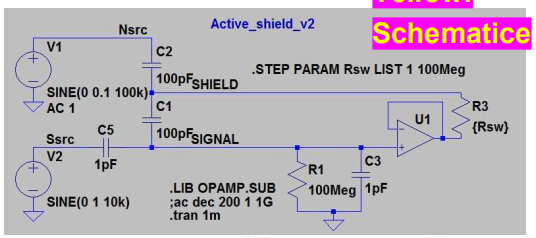
$$C_{eff} = \frac{dQ}{dV} = \frac{Q}{V_s} = \frac{V_m - V_s}{V_s} C_u = \frac{m-1}{1} C_u$$

$$C_{eff} = |m-1| C_u$$



2.2x Active shield example

Yellow: Schematice



The elements we want to see are:

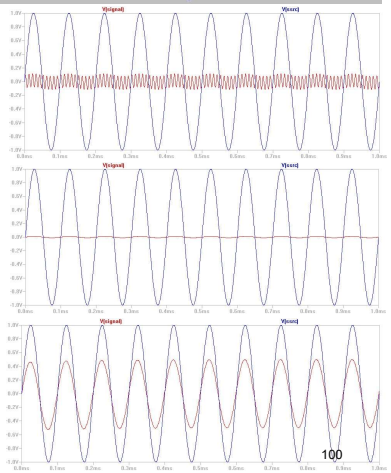
V(Ssrc): source signal

C5: Sensor capacitance

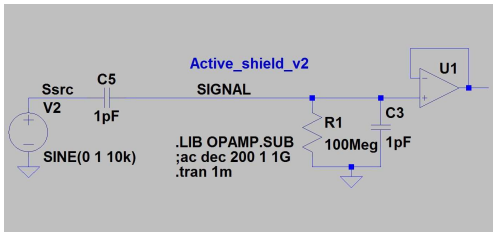
C3 & R1: Input impedance

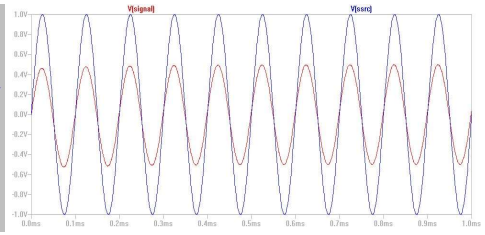
Since C5=C3 we will have V(SIGNAL)=V(Ssrc)/2 when we have managed to make all others invisible.

- With floating shield the noise Nsrc will dominate SIGNAL due to the large C1&C2.
- With grounded shield Nsrc will be stopped but Ssrc will be attenuated due to the large C1.
- With active shield Nsrc and C1 will be invisible.

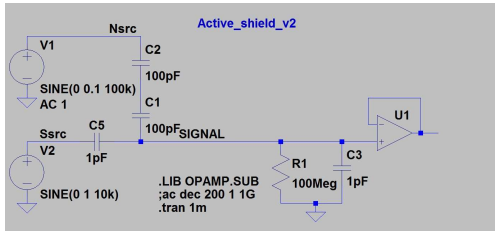


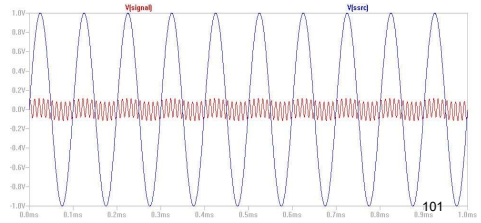
2.2x Active shield



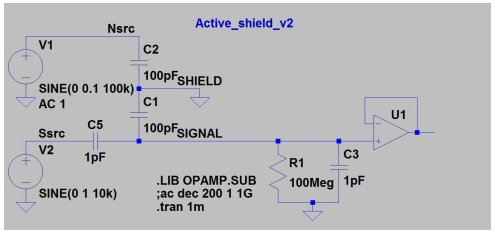


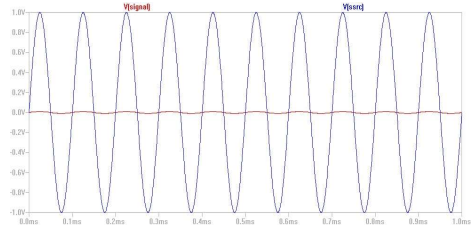
- Above: What we want
- Below: What we have



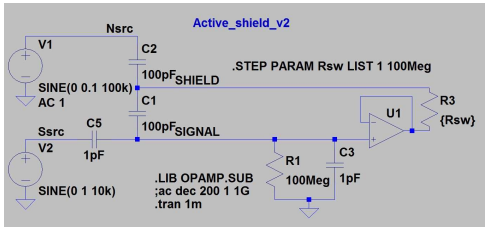


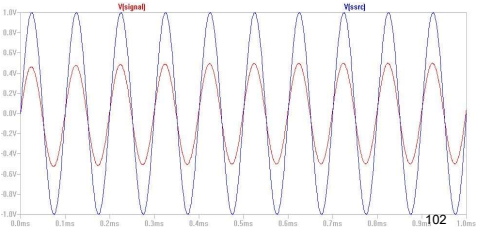
2.2x Active shield





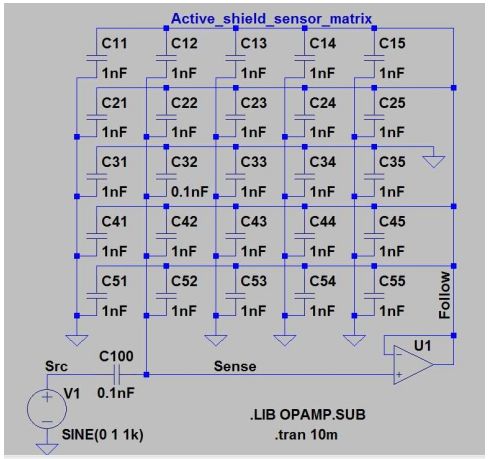
- Above: Grounded screen
- Below: Active screen

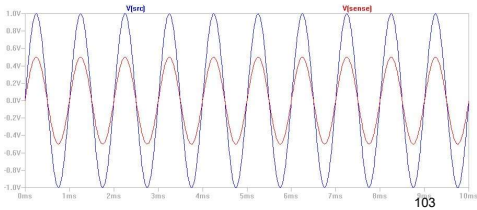




2.2x Active shield – Sensor matrix example

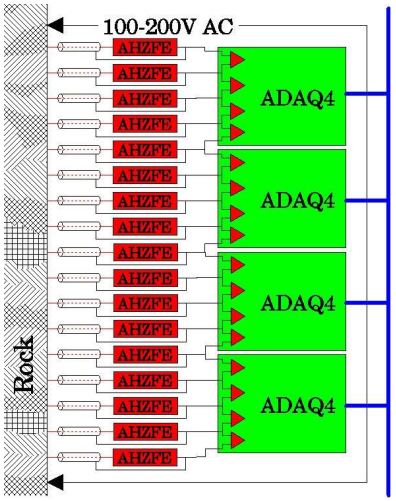
- Active shield can be used to select one capacitor in a sensor matrix.
- Our example target is C32
- Method: Ground the C32 row and connect all other rows to active shield.
- The other columns are grounded but may be connected to active shield to reduce power.
- Simulation shows V(Sense)=V(Src)/2! Thus only C100 and C32 influence and we have succeeded!





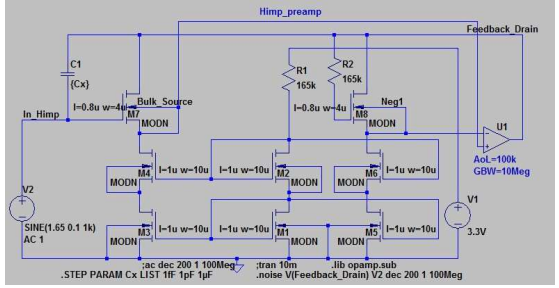
NCM-eye

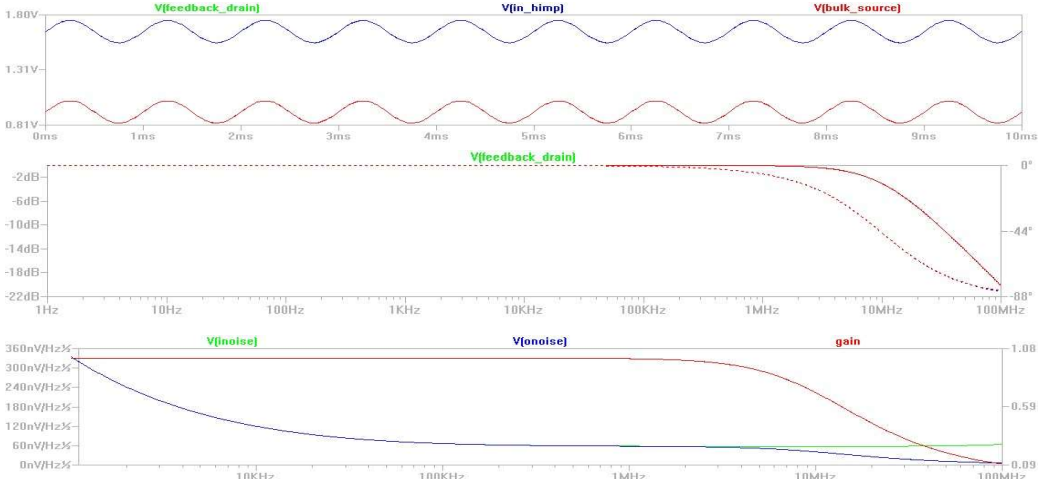
- Goal: Measure resistance in rock
- Two ASICs designed for 200° C operation temperature
- Measurement setup:
  - 100-200V AC is set up over the rock region to be inspected
  - Sensor front ends width very high input impedance (10-100GΩ) measure the local voltage level
  - Voltage differences between neighbour pairs are found
  - Resulting values are converted into a digital format and feed into common buses



Very high input impedance preamp

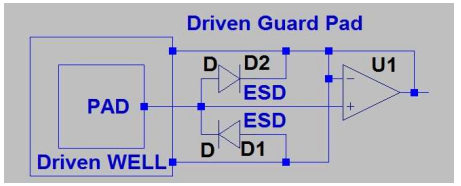
- GBW=10MHz
- Zin = 1-100GΩ

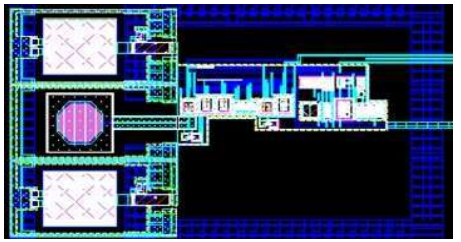




Driven guard pad

- Pad well connected to driven guard.
- ESD connected to buffer output. For this use the guard and signal have the same DC.
- Power (IO-ring) are not crossing signal path.
- Bottom figure: Driven guard pad surrounded by two standard pads.





2.3 INDUCTIVE COUPLING

$$\phi = LI \qquad L_1 = \frac{\varphi_1}{I_1}$$

L: inductance, I: current in closed circuit, ϕ: magnetic flux

L is a function of the geometry of the closed circuit and the materials within the magnetic field.

$$M_{12} = \frac{\phi_{12}}{I_1}$$

M_{12} mutal inductance between circuit 1 and circuit 2.

ϕ_{12} *flux in circuit 2 due to current in circuit 1.*

I_1 current in circuit 1.

Ignore colours

2.3 Inductive coupling

$$V_N = -\frac{d}{dt}\int_A B \cdot d\vec{A}$$

The voltage V_N is generated in a circuit loop around an area A with a flux density B. A and B are vectors. (A is a normal vector to the plane.)

Special condition example:

Conditions: A is constant, B varies with a *sin* function but with the same phase all over A. The angle θ is between A and B.

$$V_N = j\omega BA\cos\theta$$

Since $\phi_{12}=BA\cos\theta=M_{12}I_1$ in this case will have:

$$V_N = j\omega MI_1 = M\frac{di_1}{dt}$$

Red: Equation

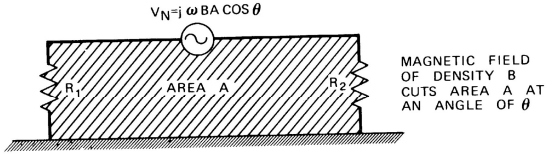


Figure 2-7. *Induced noise depends on the area enclosed by the disturbed circuit.*

2.3 Inductive coupling between two conductors

(Both are parts of their own closed loops.)

How to reduce undesired inductive coupling:

- Increase the distance between the loops
- Twin the noisy conductors (assuming the current returns through the opposite conductor and not through the ground plan.)
- Reduce the receiving area by putting the receiving circuit closer to the ground plan.
- Twin the receiving conductors.

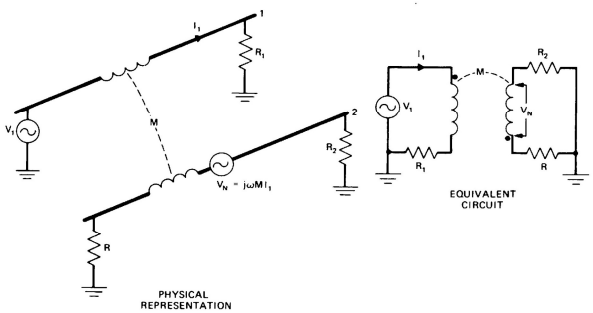


Figure 2-8. *Magnetic coupling between two circuits.*

- Orienting source and receiver perpendicular
- Use a screen

2.3 Identifying E and M field

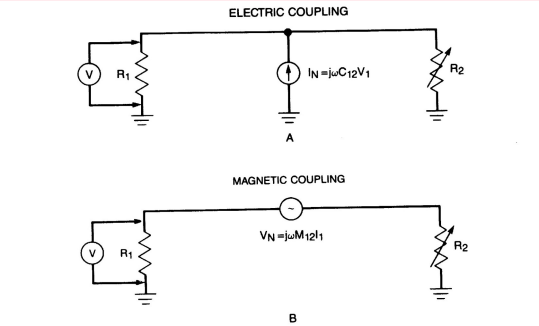


Figure 2-9. *(A) Equivalent circuit for electric field coupling; (B) equivalent circuit for magnetic field coupling.*

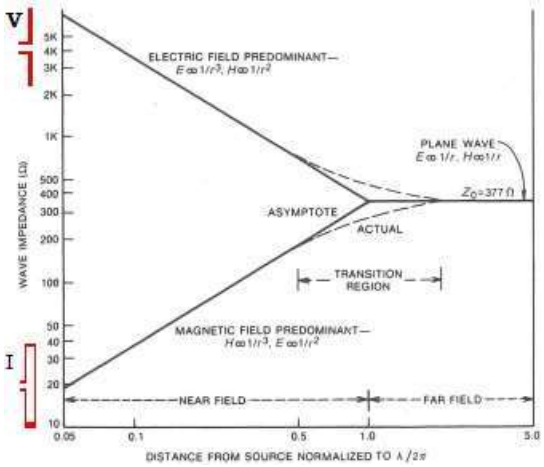
RED!!!: ALL

When R2 is reduced..... If the voltage measured over R1.....
increases is the coupling inductive while if it decreases the coupling is capacitive.

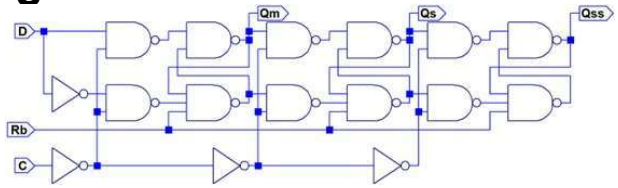
This example illustrates how we can know whether the noise is due to an E-field or an M-field. When we know this we can do further actions towards the type of noise we have identified.

Nearfield

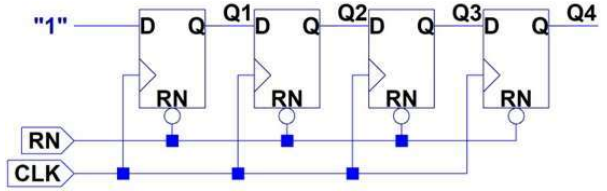
- E-field generated by voltage over open dipol
- M-field generated by current through closed dipol
- Approaches fixed ratio at λ/6



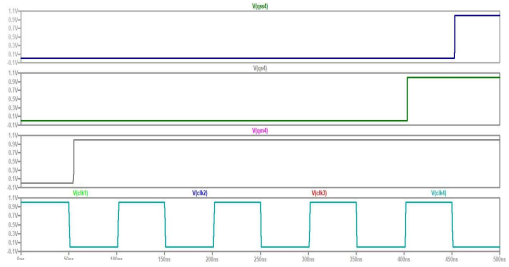
Multistage «latch» and clock variation

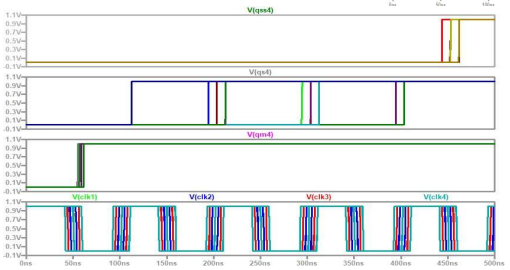


- 1-stage (latch), 2-stage (flip-flop) and 3-stage register cell
- 4-cell circuit. Initial reset to 0 followed by 4 clock pulses feeding in a «1» at the bottom.



- Q4-response with: 3-stages, 2-stages and 1-stage





- Same as above but with clock-edge variations