

UiO : Department of Informatics
University of Oslo

IN5230
Electronic noise –
Estimates and countermeasures

Lecture 12 (Mot 9)

Low noise design methods

From a system designers point of view is the challenge:

Given a sensor with a known signal, a familiar noise, and a known impedance and response characteristic:

How do we optimize the amplifier to achieve the lowest equivalent input noise?

The amplifier must be matched to the sensor. This matching is the essence of low noise design!

When we design an amplifier for a particular application, certain specifications are given. If these can not be satisfied we must make compromises: Examples of specifications are:

- amplification (gain)
- bandwidth,
- impedance levels,
- feedback,
- stability,
- dc supply,
- costs,
- PSRR (Power Supply Rejection Ratio),
- CMRR (Common Mode Rejection Ratio),
- area (for ASICs), and
- signal-to-noise requirements.

A common method of design is that we first focus on the bandwidth and gain and then look at noise. When noise is also important, noise should be considered already from the beginning!

To achieve optimum noise, it is necessary to:

1. Select the correct input and amplifier element: FET or BJT!
2. Then select operation point.
3. Further select a circuit configuration: Common emitter/source, collector/drain and base/gate.
4. Feedback and filtering are then selected accordingly to meet other design requirements.

9.2 Design Procedure

Let us assume that the source impedance Z (f) and preamplifier noise *En(f)* and *In(f)* is a function of the frequency *f*. Absolutely minimal equivalent input noise will be determined by these. If one operates on a frequency *f* with (infinitely) narrow bandwidth one should use a network that matches *R0=En(f)/In(f)* with *Z(f)*. The same will of course be the case if *Z(f), En(f)* and *In(f)* does not change significantly with *f*. Otherwise, when the signal has a certain bandwidth, an integration have to be done over the entire bandwidth. One can use programs (eg. LTspice) to carry out this integral. The resulting analysis may indicate that there is too much noise to meet the requirements or it may indicate that a different operation point is more favourable. If it is not possible to meet the noise requirements at this time it is no network around the transistor that can reduce the noise to an acceptable level.

The noise in the first stage must be small to achieve low total noise for the system. If the gain in the first stages(s) is large enough we may be able to ignore noise analysis for the subsequent stages. In high frequency stages this will often not be the case. The gain-bandwidth product overhead relative to the target frequency is too small so that the gain is not sufficient at the desired frequency. Multiple stages are needed and the noise contribution from subsequent steps must be taken into account.

After deciding on preamplifier a bias network and power supply has to be selected. The new total noise is estimated with the new elements. Then we can add feedback to get the correct impedance, gain and frequency response.

Will we when designing for a low noise application always design the amplifier for the lowest possible noise?
No, not necessarily if the NF is less than 2 to 3 dB. A NF of 3dB means that the amplifier contributes as much as the source and that the total noise is $\sqrt{2}$ times as large as each of the elements. If a huge effort is required to get a very low NF value, the total noise can only be reduced towards $1/\sqrt{2}$ of the total noise when NF=3dB. I.e. by going under 3dB the maximum reduction that can be achieved is 30% of the 3dB-noise level.

In, say a transmitter and a receiver, a 3dB reduction of noise will correspond to a doubling of the transmission power. This can be significant. It may mean for example higher data rate, better image quality or longer transmission range.

Another possibility is to construct a system so that it operates with a reactive source with only a small resistive resistance. An inductance and a small series resistance could provide virtually no thermal noise. However the term *In*Xs* will dominate at higher frequencies.

To achieve low noise, the designer should focus primarily on the lowest equivalent input noise and ignore NF.

9.3 Features of the active input item.

Options: BJT or FET, either as a discreet component or at the input of an IC. Important parameters when selecting the input element is source impedance and frequency range. Figure 9.1 from the book may give some indication.

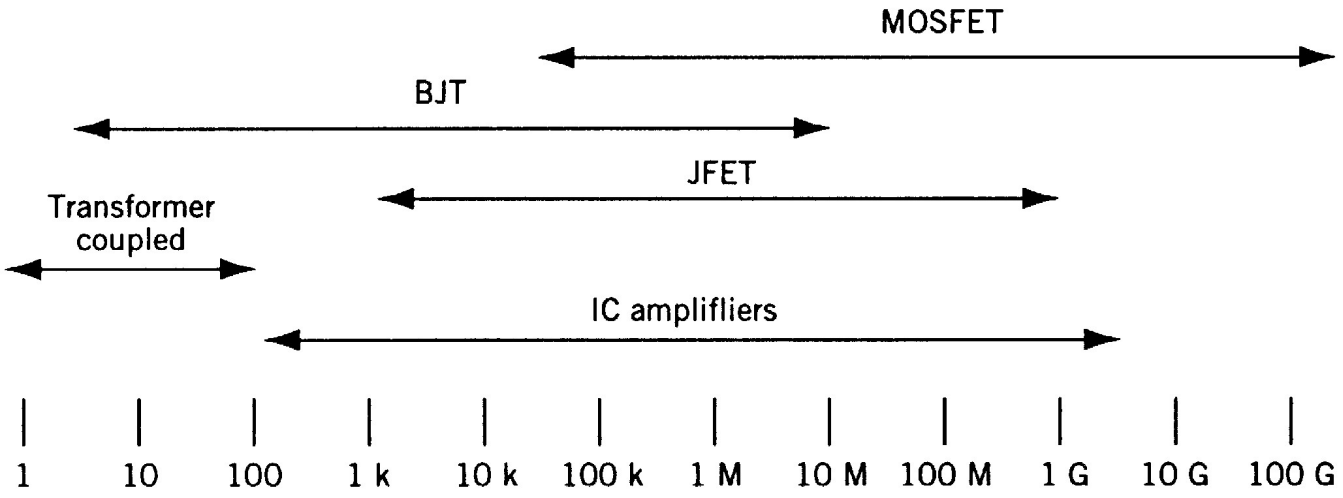


Figure 9-1 Guide for selection of active input devices.

At the lowest input resistances, it is often necessary to use a transformer to match the source resistance to the amplifier's R_0.

Bipolar transistors (discrete or at the input of an IC) is often beneficial when the source impedance is in the middle region. R_0 is regulated by say increasing the collector current for low resistances and vice versa. There is a small difference between *npn* and *pnp* transistors:

- *pnp* has a lower base resistance due to higher mobility in the n-base. Thus the base has a lower thermal noise voltage and can be used at lower source resistors.
- On the other hand, have the *npn*-transistors often higher β_0 and f_T. This will be beneficial for larger source resistors at higher frequencies.

In the case of larger source resistors FETs are more appropriate because of lower *In*.

When the source resistance can vary over a large area JFETs will often be preferred. A JFET has an *En* which is slightly higher than a BJT but an *In* which is significantly lower. This is particularly important when working with a reactive source over a wide frequency range since the source impedance is linearly related to the frequency. The FETs are also well suited as a voltage amplifier due to high input resistance and low input capacitance.

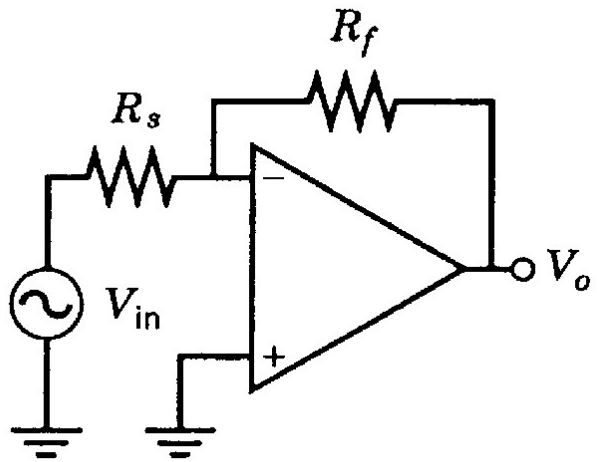
For the highest source resistances MOSFETs are preferable because of very low *In*. According to the textbook MOSFETs have flicker noise that is between 10 and 100 times as high as JFETs and BJTs. ~~It is expected that this will be improved as the processing technology is developed.~~ MOSFET (CMOS/BiCMOS) has other strong benefits (also non-noise-related) that results in that the MOSFET can be more attractive: Low cost, low power, compact digital logic, high integration level of analogue and digital circuitry on the same dice. The latter also means that one can have advanced analogue and digital noise reduction architectures/algorithms implemented on the same dice. The integration ratio has both negative and positive effects with regard to coupling noise. On one hand, wires are shorter and coils smaller and will therefore not pick up the noise so easy, while on the other hand, distances are smaller, so that coupling noise, for example via the substrate becomes a larger challenge.

In the case of small source impedance, bipolar input stages may be preferable, while at high input impedances *In* becomes more important and the low *In* of MOSFETs will make it best suited.

Feedback

Having decided the type of input transistor, operation point, and amplifier architecture, we select the feedback to obtain the desired input impedance, gain and frequency response. As shown in Chapter 3 the feedback does not change the equivalent input noise (except for any additions due to for example, thermal noise in the feedback resistance). However, the output signal and output noise will be affected.

If the goal is low input impedance, we can use an architecture like this:



Low input impedance is important when it comes to measuring current. The input impedance is reduced proportionally with the relationship between the open-loop and the closed-loop gain. This method to reduce the input impedance is effective if one wants to reduce the frequency responses dependency on the input capacitance.

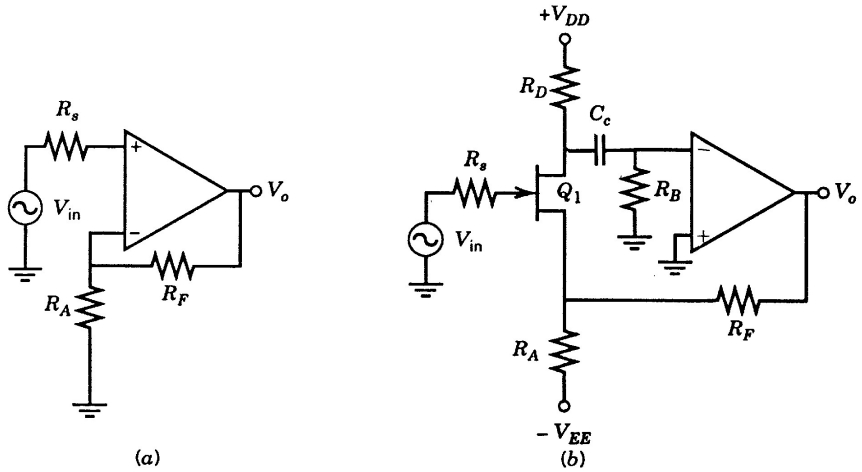


Figure 9-3 High-input-impedance amplifiers: (*a*) Noninverting amplifier and (*b*) CS stage added for higher input resistance.

The circuit to the left has high input impedance and reduced input capacitance. High input impedance is necessary when there is a voltage signal from a high impedance source to be measured. The figure on the right has an extra transistor in the input to increase the input impedance.

(Also highly relevant is the high input impedance schematic shown in the lecture related to active shield.)

Bandwidth and source requirements

The bandwidth of the input amplifiers should not be larger than strictly necessary to pass the signal. Unnecessary extra bandwidth allows more noise.

General noise characteristics of BJT indicates that the noise is constant and at the lowest level at the medium frequencies. In general, an increase of the collector current will increase the 1/f-noise and reduce high frequency noise (i.e. internal coupling noise). The current must be adapted to the individual setup and application and the noise must be found by integrating over the appropriate frequency range.

Inductive source provides the largest source impedance for high frequencies. Low *En* is important at low frequencies, while low *In* is important at high frequencies. The solution may be a BJT with low collector current or a FET with a low *En* at low frequencies.

A source with capacitive shunts means that *En* will be most critical. The solution may be a bipolar transistor with high collector current to minimize *En*. If the source resistance is large it may be necessary to use a FET with a low *En* at high frequencies.

When it comes to sensors that are both inductive and capacitive very much will depend on where the resonance frequency is in relation to the frequency band to the desired signal. At the resonance the noise may be minimal while the conditions for the desired signal can be difficult. Over and under the resonance, the conditions may be quite different and vary greatly. A FET that has both low *En* and low *In* will probably be the best alternative. The best solution is often to place the resonance at the upper frequency limit of the desired frequency range.

High frequency and high source impedance requires low *In* at the relevant frequency range. In addition, low input capacitance is required to ensure adequate frequency response. This can be achieved with a FET that operates as a voltage follower or an emitter follower with small collector current. The input capacitance can be further reduced by using negative feedback.

Equivalent input noise

The expression for the equivalent input noise can be written:

$$E_{ni}^2 = E_t^2 + E_n^2 + I_n^2 \left| Z_s \right|^2$$

Z_S is the total source impedance. *Et* is the source noise. If the noise is purely thermal, *Et* will be the noise due to the real part of the source impedance.

In the following we will look at the equivalent input noise for two amplifiers. Such curves can describe a single frequency or represent integrals over a frequency band.

We must remember here that the curve for *Et* is with resistance on the x-axis while the curve for *In*|*Zn*| is with impedance on the x-axis. The dotted curve for the total noise is thus only appropriate when the source impedance is purely resistive and does not have inductive/capacitive elements.

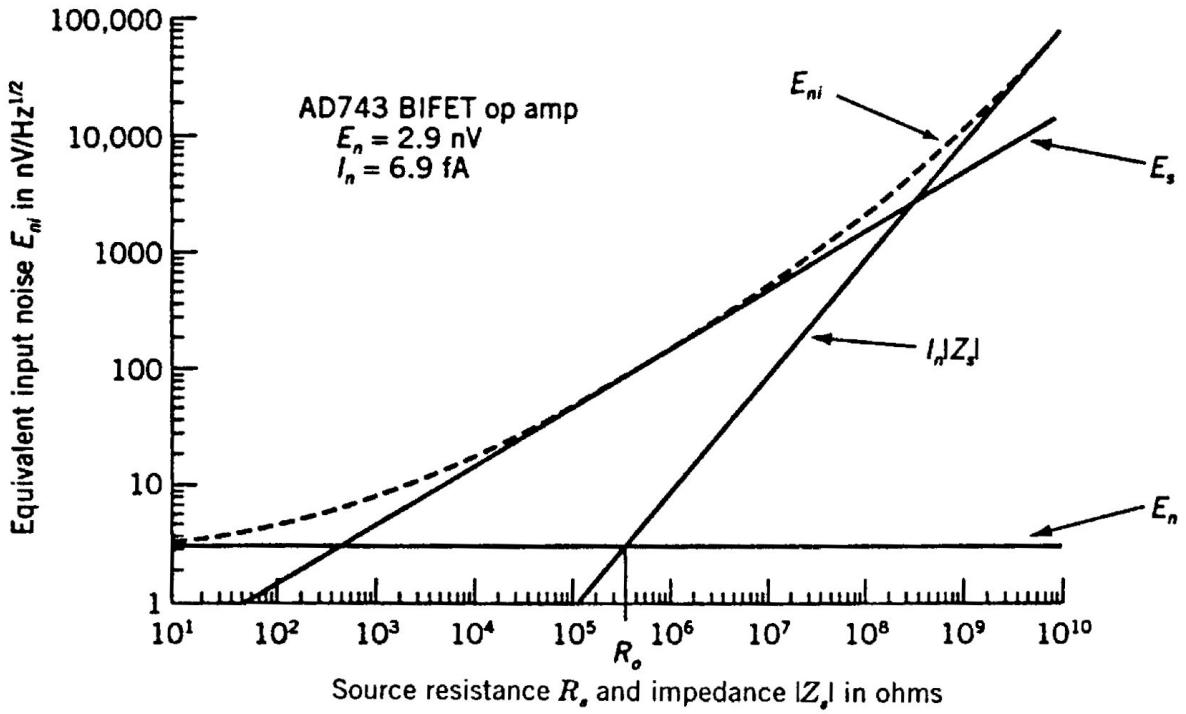


Figure 9-4 Plot of total equivalent input noise versus source resistance for an AD743 BIFET op amp.

We see that the FET amplifier AD743 has optimum source resistance at 420kΩ and that a relatively good adaption can be achieved in the entire region from 600Ω to 300MΩ.

The bipolar amplifier OP27 has optimum source resistance at 6.7kΩ and has relatively good adaptation in the range from 200Ω to 200kΩ.

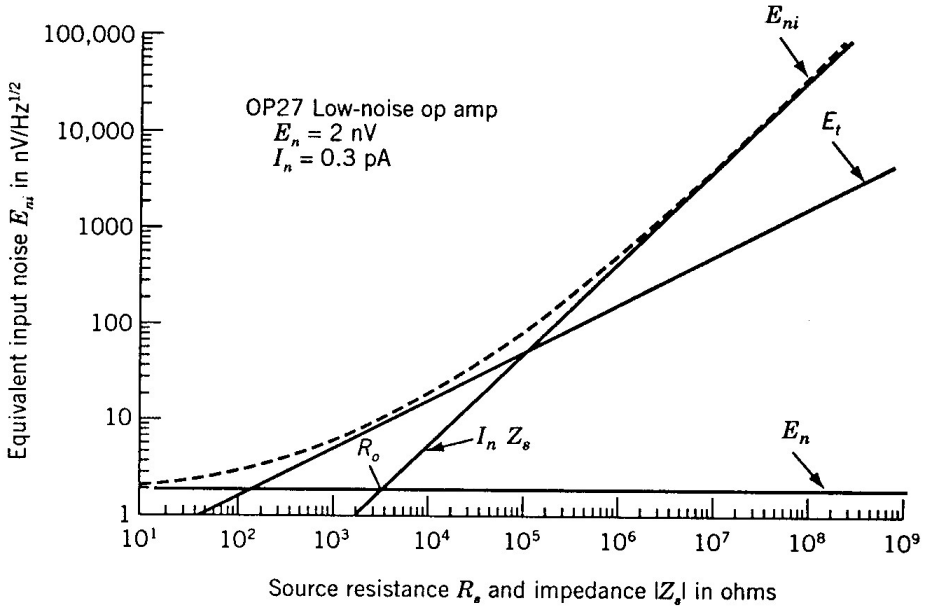


Figure 9-5 Equivalent input noise for an OP-27 low-noise bipolar op amp.

When the sensor/source is not given, a sensor is selected with high S/N-level and impedance as close as possible to what is optimal for the amplifier. If the source resistance is less than optimal, adding more resistance in series does not reduce the equivalent input noise but increase it. Increasing the source resistance is worthwhile only when the signal is increased accordingly.

When the sensor/source is given, *En* and *InZs* is selected through the choice of the input transistor, connection, etc. so that *Eni* is as small as possible. For example, if the source resistance is 100Ω, the bipolar amplifier OP27 will have the lowest noise figure while if the source impedance 1MΩ the AD743 amplifier will have the lowest noise.

Transformer coupling

When the sensor impedance is very different from the optimum source resistance of the amplifier a transformer could be the solution. This applies, for example, at very low source resistances.

Figure 5-6 indicates that for very small source resistors the lowest equivalent input noise is achieved in this figure for currents around 10mA.

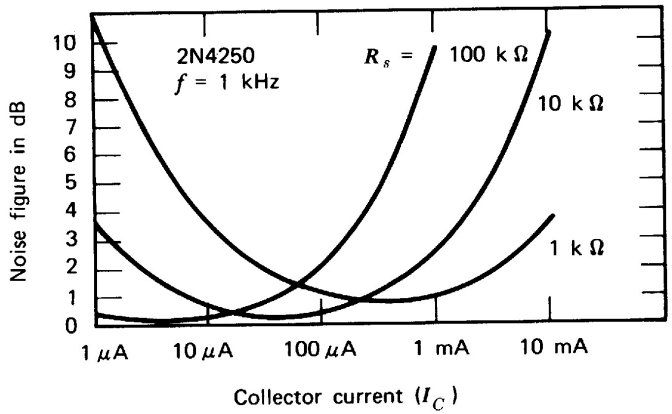


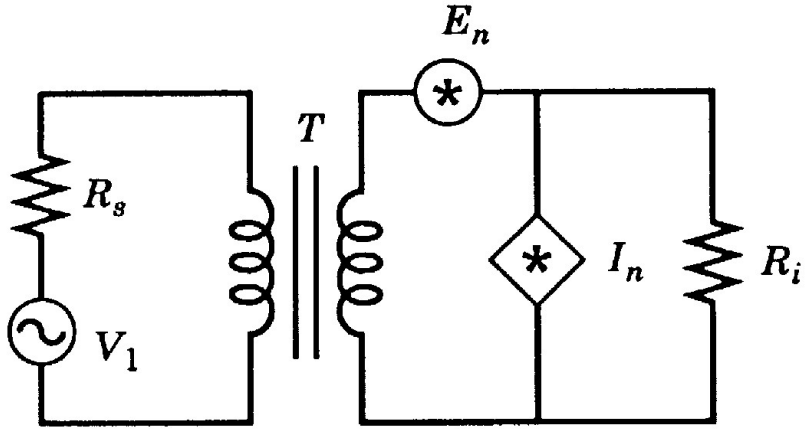
Figure 5-6 Effect of collector current and source resistance on noise figure.

However, this high current provides poor optimal noise factor. If one uses a transformer coupling, a lower *Ic* can be used and the noise reduced.

The goal is to make the transformed source resistance equal to the amplifier's optimum source resistance.

Transformed to the source side the equivalent noise voltage becomes:

$$E'_n = \frac{E_n}{T}$$



And the equivalent noise current is:

$$I'_n = TI_n$$

The amplifier's transformed optimal source resistance can be expressed:

$$R'_o = \frac{E'_n}{I'_n} = \frac{E_n}{T^2 I_n} = \frac{R_o}{T^2}$$

So we choose *T* so that *R'o* is equal to *Rs* (or more precise: *Zs*). Now the amplifier "sees" a source resistance equal to the optimum.

Design example #1

Goal:

- Evaluate different input possibilities given an operating frequency of 10kHz and a source resistance of 100kΩ.

Options:

- Standard OPAMP circuit with bipolar input
- Standard OPAMP circuit with FET input
- Discreet bipolar transistor
- Discreet JFET
- Discreet NMOS
- Discreet PMOS
- ASIC with npn input
- ASIC with pnp input
- ASIC with NMOS input
- ASIC with PMOS input

In the first 6 options, we will choose between the available standard components that are offered us by the suppliers. Components can be characterized with the values and curves that describe these. We will only be able to choose between the components that are available and not be able to choose freely, for example transistor size, input capacitance etc. In the case of the ASIC options we will be able to choose exactly the sizes of the physical and electrical parameters that we want. But we will be limited by the technology we have selected. It means that we can not choose a JFET transistor in a standard BiCMOS process. We will describe electrical quantities such as noise and gain as mathematical expressions of the widths and lengths of transistors, etc. We will thus be able to optimize these sizes so that we get exactly the figures and transistor size that are optimal.

Example MOSFET:

$$En^2 = \frac{8kTg_m/3}{g_m^2} + \frac{\left(K_F I_{DQ}{}^{AF}\right)/\left(fC_{ox}L_{eff}^2\right)}{g_m^2}$$

$$In^2 = 2qI_{gs} + 4kT \cdot \frac{\omega^2 g_m R_L^2 C_{gd} C_L}{1+\omega^2 R_L^2 C_L^2}$$

Example Bipolar:

$$En^2 = 4kTr_x + 2qI_C r_e^2 + \frac{2qf_L I_B^{\gamma} r'^2_x}{f} + 2qI_C r_x^2 \left(\frac{f}{f_T}\right)^2$$

$$In^2 = 2qI_B + \frac{2qf_L I_B^{\gamma}}{f} + 2qI_C \left(\frac{f}{f_T}\right)^2$$

The textbook describes only the first four options and it is only those we want to discuss further.

Integrated amplifiers

First, we consider integrated amplifiers. Appendix A shows the characteristics of a variety of amplifiers, and we want to choose between these. We swipes *En* and *In* at 10kHz and generate the following table): (The µA741 value is different from what found in the textbook).

Integrated preamplifiers			
	En (nV/√Hz)	In (fA/√Hz)	Eni (nV/√Hz)
OP27/OP37 Bipolar	3,5	850,0	85,1
TL061 JFET	45,0	90,0	45,9
TL071 JFET	20,0	55,0	20,7
OP97 super beta Bipolar	18,0	7,0	18,0
µA741 Bipolar	10,0	650,0	65,8
AD745 BiFET	3,0	50,0	5,8
TLE2027/2037 Bipolar	2,5	600,0	60,1
Lin CMOS	10,0	45,0	11,0

Eni at the far right is $\sqrt{(En^2 + In^2 * 100k\Omega^2)}$. We see that there are different amplifiers that have the lowest *En*, *In* and *Eni*.

If the source resistance of 100kΩ is purely resistive, it will contribute with a noise equal to $40nV^2/\sqrt{Hz}$. Used together with the AD745 the total noise becomes 40.4 $nV^2/\sqrt{Hz}$ of which the source noise will be dominant.

Discrete JFETs

Appendix B shows the graphical representation of the characteristics of multiple JFET transistors. The table below shows the values of *En* and *In* read at 10kHz.

	JFET		
	En (nV/√Hz)	In (fA/√Hz)	Eni (nV/√Hz)
2N2609 n-channel JFET	3,0	40,0	5,0
2N3460 n-channel JFET	4,0	10,0	4,1
2N3684 n-channel JFET	4,0	8,0	4,1
2N3821 n-channel JFET	2,5	5,0	2,5
2N4221A n-channel JFET	5,5	7,0	5,5
2N4416 n-channel JFET	2,0	13,0	2,4
2N5116 p-channel JFET	5,0	33,0	6,0

Eni at the far right is $\sqrt{(En^2 + In^2 * 100k\Omega^2)}$
In the case of the least noisy transistor (2N4416) the total noise including the thermal noise of the 100kΩ resistance is equal to $40{,}1nV^2/\sqrt{Hz}$. I.e. the source noise is strongly dominant.

Discrete bipolar

In appendix C it is given some graphical characteristics for some discrete bipolar transistors. The table below show some values read out from three of the transistor figures. For each of the transistors five collector currents are read.

	Bipolar		
	En (nV/√Hz)	In (fA/√Hz)	Eni (nV/√Hz)
	2N930 npn		
1µA	15,0	74,0	16,7
10µA	5,4	200,0	20,7
100µA	3,4	630,0	63,1
1mA	3,4	2300,0	230,0
10mA	5,4	13000,0	1300,0
	2N4124 npn		
1µA	15,0	86,0	17,3
10µA	4,3	17,0	4,6
100µA	1,8	400,0	40,0
1mA	1,3	1300,0	130,0
10mA	1,3	4000,0	400,0
	2N4250 and 2N3964 pnp		
1µA	15,0	80,0	17,0
10µA	4,6	100,0	11,0
100µA	1,8	290,0	29,1
1mA	1,6	860,0	86,0
10mA	1,6	2700,0	270,0

We see that the high current reduces *En* but increases *In*. What is optimal will be highly dependent on the source impedance. Anyway for all cases there will be a specific current that makes minimal noise. Of the three reviewed transistors, it is the 2N4124 with $IC=10\mu A$ that has least noise = $4.6nV^2/\sqrt{Hz}$. Including the source resistance the total noise becomes $=40.3nV^2/\sqrt{Hz}$.

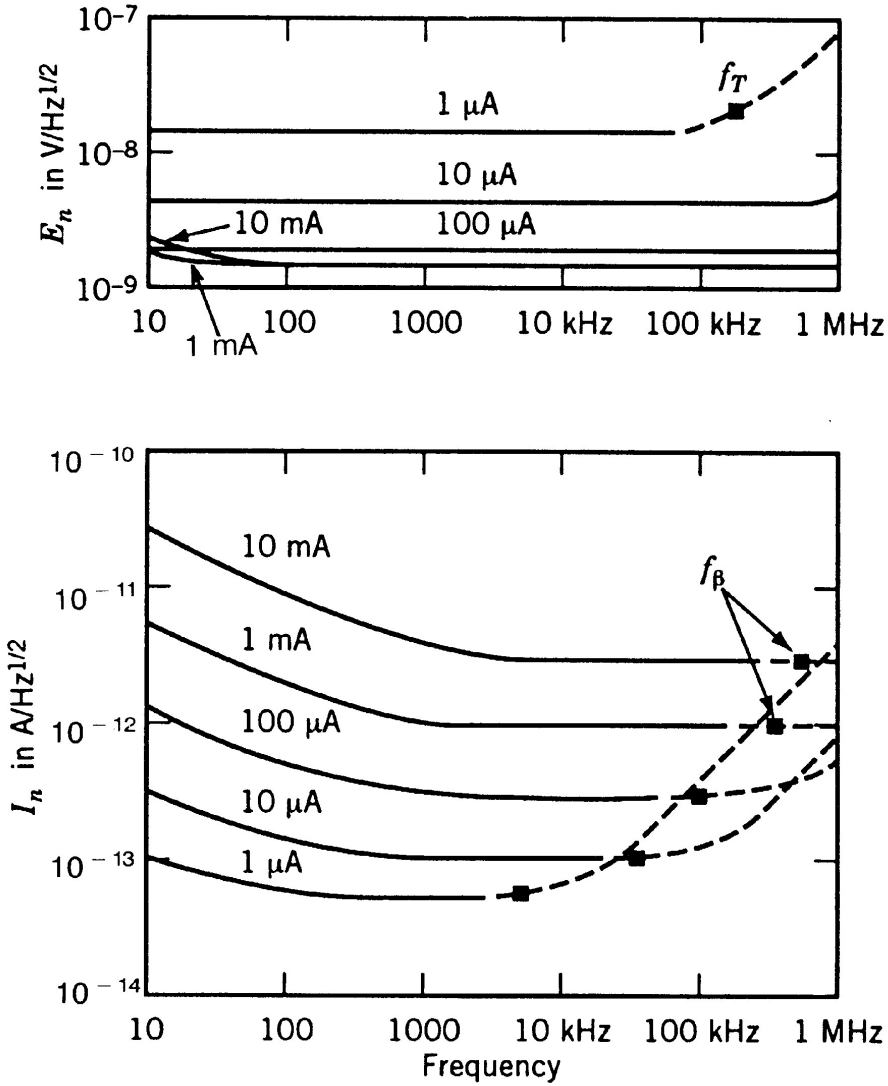


Figure 5-9 E_n and I_n performance of a 2N4250 transistor.

Design example #2:

Goal:

Frequency of 100Hz and source resistance varying between 5 and 500Ω.

Solution:

By studying the graphs in appendix C, we see that 100kΩ is a favourable input impedance. We will match the source resistance to this with the help of a transformer. We start our calculation with a source resistance that is geometric in the middle: 50Ω.

$$T^2 = \frac{R_{opt}}{R_S} = \frac{10k\Omega}{50\Omega} = 200 \qquad T = \sqrt{200} = 14.14$$

When R_S is 5Ω the transferred resistance on the secondary side is 1kΩ whereas when R_S is 500Ω it is 100kΩ on the secondary side equal. The DC-resistance in the coil must be significantly smaller than the transferred resistors found above. I.e. on the primary side the parasitic/routing resistance must be substantially below 5Ω. The parasitic resistance R_C (see fig 8-17 p. 201) must be significantly larger than largest resistance, i.e. on the primary side significantly larger than 500Ω say 10kΩ.

We choose a bipolar transistor based on the graphic characteristics given in appendix C. We will find the transistor with minimum noise at 100Hz for a source resistance from 1kΩ to 100kΩ.

2N4250 Example:

In the 100Hz figure, we see that the 1dB NF area covers a region from approx. 1kΩ&100μA towards 100kΩ&1μA. At 10kΩ it seems as the centre of the 1dB region is at about 30μA.

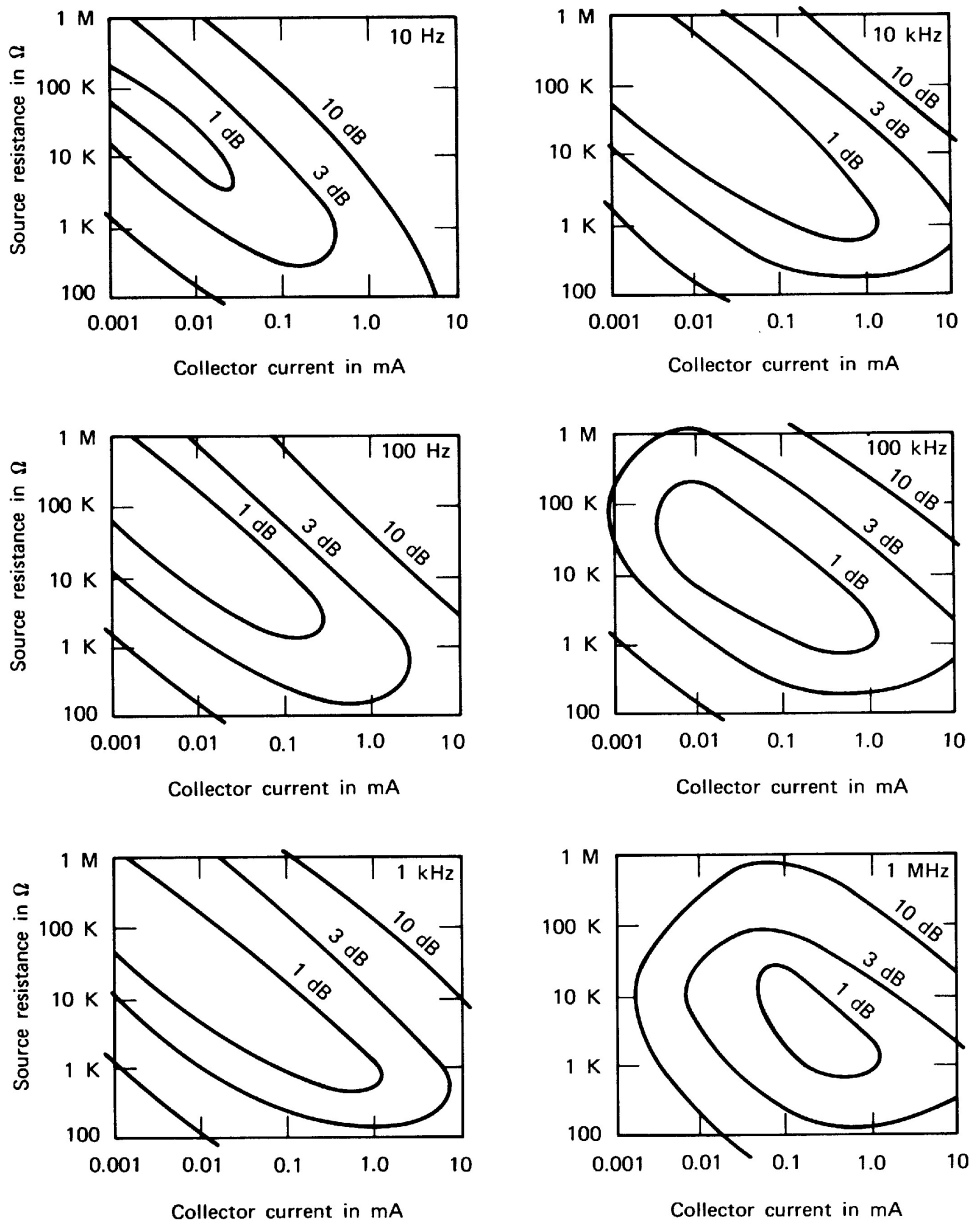


Figure 5-8 Contours of constant narrowband noise figure.

By studying all the figures in appendix C we can set up the following table for 100Hz:

Transistor	Characteristics of 100Hz
2N930	Small 3-dB contour
2N4124	Large 3-dB contour
2N4125	Small 1-dB contour
2N4250	Large 1-dB contour for large and medium Rs
2N4403	Large 3-dB contour
2N5138	Large 3-dB contour
MPS-A18	Medium 1-dB contour for high-Rs

From the table we see that the same transistor as in our previous evaluation is still the best.

We find that the *En* and *In* for 2N4250 at 30μA are $En=3nV/\sqrt{Hz}$ and $In=0.3pA/\sqrt{Hz}$. Not surprisingly this gives a $Ropt=En/In=10k\Omega$. These values are valid for the secondary side. In order to convert the value to the primary side we divide *En* by the turn ratio and multiply *In* by the same ratio.

We put up in a table the properties of the lower limit, the upper limit and the geometric mean of the source resistance.

Rs	5Ω	50Ω	500Ω
R_2	1kΩ	10kΩ	100kΩ
E_t	0.284nV/√Hz	0.89nV/√Hz	2.82nV/√Hz
E_{ni}	0.355nV/√Hz	0.946nV/√Hz	3.55nV/√Hz
NF	1.94dB	0.460dB	1.96dB