INF 5230 Electronic Noise – calculation and countermeasures

Mandatory lab 3 - 2026.

Send report by email to farnazsa@ifi.uio.no.
Deadlines: 11th of November, 08:00 am.
Assessment: Approved / Not approved.

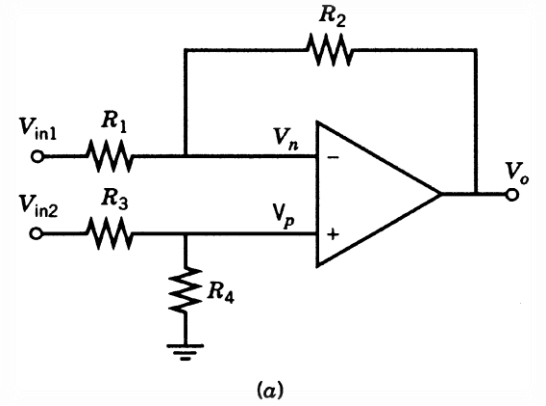
- Reports are submitted on an individual basis.
- The reports shall consist of schematics that are used, simulation results, text EXPLAINING what has been done as well as an ANALYSIS of the results.
- Put up a summary table and comment at the end of each task when relevant!
- USE WHITE/LIGHT BACKGROUND for the plots!
- Avoid yellow curves.

2024 modifications

Since some students seems to struggle unreasonable much with drawing the amplifier transistor schematics, the schematics will this year be given to the students. There are four amplifiers that will used in this assignment: An ideal amplifier from standard library (opamp), a simple 8 transistors differential amplifier (amp_8t), a common source amplifier (amp_cs) and a fully differential amplifier. The last amplifier (the fully differential) used in subtask 5 will be made available later. A test bench (tb_opamp_2024) contains a simple setup for the first three amplifiers. The students can use this as a basis for developing the test benches for the different subtasks in this assignment. (The test bench shows how the amplifiers response on a small sinus on top of a ramp).

1. Ideal amplifier

We will first look at an ideal amplifier in an ideal differential amplifier configuration. You can copy the amplifier symbol from the "opamp" circuit in the LTspice "Educational" area (2024: Or from tb_opamp_2024.zip). *Let the opamp Aol be 100k and the GBW be 10Meg.* Be sure to get the "include" statement. Build a resistive network around as indicated in Figure 3-4 "Differential amplifier using one op amp" page 56 (figure in Motchenbacher and repeated below). For all cases the relation between the resistors will be R1=R3=Rx and R2=R4=10Rx.



a) Let Rx be 1kΩ, 10kΩ and 100kΩ. Is the gain different in the three cases?

Run **.NOISE** simulations and find the output noise and equivalent input noise for the three cases at 10 kHz.

Find the total equivalent input noise both at the positive and the negative input by simulation (in the region where the gain is larger than one). What type of noise is present here?

b) Calculate manually the spot noise (at 1kHz) for each of the resistor elements (don't merge R3 and R4 into Rp!) **i)** locally (at their position), **ii)** their value at the output and **iii)** their equivalent value at the iii) input. Use the table below.

Which of these three (i), (ii) or (iii) can you find in the simulation results? Which of the resistors has the largest contribution at the output and at the input?
You may modify and manipulate the following expression to calculate the gain from the local positions to the output.

$$V_O = \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right)V_{in2} - \left(\frac{R_2}{R_1}\right)V_{in1}$$

Example table:

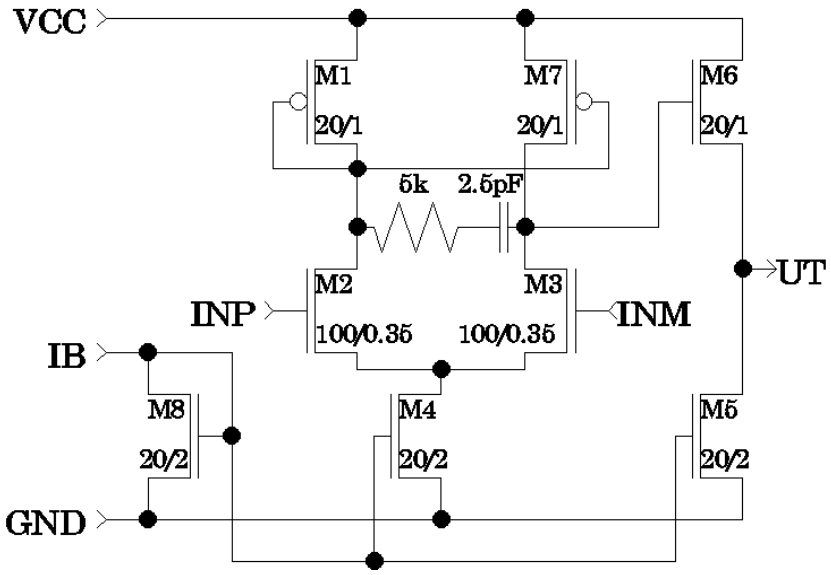
	Local noise (nV/√Hz)	Gain to output	Noise at output (nV/√Hz)	Equivalent noise at input(nV/√Hz)
R1				
R2				
R3				
R4				
Total				

Make similar tables for Rx = 1kOhm, Rx=10kOhm and Rx=100kOhm.

2. Simple CMOS amplifier

The ideal amplifier provides unrealistic behaviour at higher frequencies. We will now replace the amplifier with a simple 8 transistor CMOS amplifier.

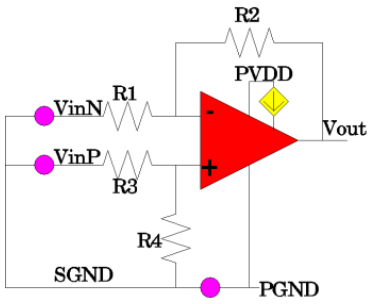
Before we can draw the amplifier, we must install model files and symbols. Download standard.mos and replace the original model file located at <programfiles>/LTC/LTspiceIV/lib/cmp/ with it. Download the symbols for pmos and nmos (pmos4.asy and nmos4.asy) and put these symbols in the directory where you have your schematics. (Links are also provided in the lecture plan.). Then draw the following schematic (2024: Use the schematic made available for you):



Change model designations respectively to MODP and MODN. Let bias reference current IB be 50µA. Remember to connect MODN substrate to low potential (GND) and correspondingly MODP substrate/well to high potential (VCC). The transistor sizes are given as width/length in the figure. Widths and lengths must be specified with µ or u after the size in LTspice! *The supply voltage VCC is 3.3V.*

Make a symbol with the same name as the schematic. (When the simulator finds a symbol, it looks for a schematic with the same name.)

Note that in this case the signal ground must be different from the power ground. Add a voltage source with DC=1.65V between the global ground (power ground at 0V) and the signal ground. Let R4 and the input signals refer to the signal ground and not to the power ground! (Pink circles are voltage sources.)



a) Perform AC analysis for the amplifier without feedback (i.e. open-loop). Let the common mode voltage (i.e. DC voltage of input signal) be 1.65V.
Do AC analysis with a signal on the **i)** positive input (ACpos=1, ACneg=0), on the **ii)** negative input (ACpos=0, ACneg=-1) and **iii)** with differential signals on both inputs (ACpos=1, ACneg=-1).

b) Replace the ideal amplifier in the feedback network in task "1 Ideal amplifier" with our new amplifier. Let Rx = 1kΩ. Inspect the simulation results on the positive input and the output. What is the frequency range at which the flicker noise is dominant?

c) We would like to know the (spot) noise at some frequencies and the integrated noise over some frequency ranges. Find the gain, the (non-inverting) input noise and the output noise at 1Hz, 1kHz, 1MHz and 1GHz. Then find the noise for the frequency ranges 1Hz-1kHz, 1kHz-1MHz and 1Hz-1MHz. (Use the .MEAS statement). If we consider the noise in 1Hz-1kHz uncorrelated with the noise in 1kHz-1MHz, how can we manually calculate the noise in the range 1Hz-1MHz from the two subareas we found through simulation?

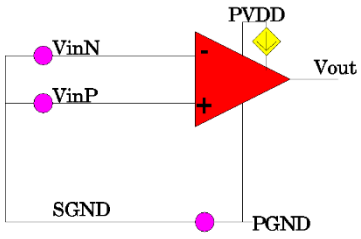
d) Perform the same NOISE simulation as in task 1 with Rx = 1kΩ, Rx = 10kΩ and Rx = 100kΩ. Simulate with a capacitive load of 1pF. List the six largest sources of noise at 10kHz for all three cases. The noise should be identified on resistor and transistor level. Consider all the noise from a transistor together without splitting up into thermal noise, flicker noise etc. Comment on the result.

	Rx=1kΩ	Rx=10kΩ	Rx=100kΩ
1.	<Strongest noise source>	<Strongest noise source>	<Strongest noise source>
2.	<2nd strongest noise source>	<2nd strongest noise source>	<2nd strongest noise source>
3.	<3th strongest noise source>	<3th strongest noise source>	<3th strongest noise source>
4.	<4th strongest noise source>	<4th strongest noise source>	<4th strongest noise source>
5.	<5th strongest noise source>	<5th strongest noise source>	<5th strongest noise source>
6.	<6th strongest noise source>	<6th strongest noise source>	<6th strongest noise source>

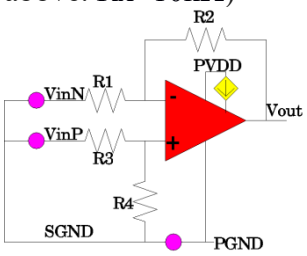
3. Open loop, 10x gain and follower.

In this task, you shall find the gain and spot noise at 1MHz and the integrated noise from 1 Hz to 1 MHz at output and the non-inverted equivalent input noise. Find this for open loop, for 10x (with the network over) as well as a follower. Present your results in a table.

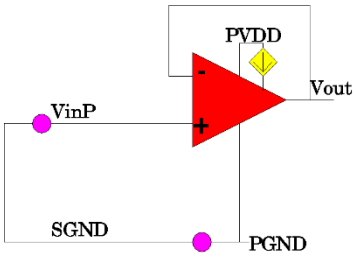
i) open loop,



ii) with a gain of 10 (with the network discussed above. Rx=10kΩ)



iii) a follower

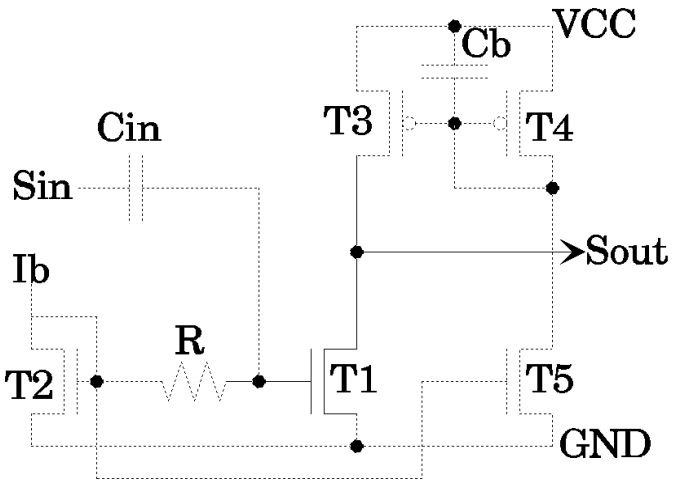


The small pink circles are voltage sources. The voltage sources between SGND and PGND is a 1.65V DC source.

	Spot noise	**Integrated noise**
	1 MHz (nV/√Hz)	**1Hz – 1 MHz (µV)**
Open loop		
Equivalent input noise		
Gain		
Output noise		
10x gain		
Equivalent input noise		
Gain		
Output noise		
Follower		
Equivalent input noise		
Gain		
Output noise		

4. Common source input stage

We will in this subtask look at a Common-Source architecture popular in RF-input stages. CS-amplifiers have worse common-mode behavior than the previous amplifier. However, since we will filter away the DC-component (with an input capacitor) and RF-amplitudes are typically only tens of microvolts, the bad common mode performance can be ignored.



The central element is the transistor T1. The other components are used to provide correct bias. The T1 source is connected to ground (common), while the input signal on the gate will be amplified to the T1 drain.

We wish only to amplify a narrow frequency bandwidth and ignore the DC-value of the input signal. We leverage this to provide the T1 gate the DC value that provides optimal performance. We place a capacitor (Cin) between Sin (signal input) and the T1 gate to achieve DC isolation. The value of the capacitor must be chosen so that the frequency we want to amplify is not reduced too much by the capacitor. The R and C form a high-pass filter for the frequency signal from the signal source and a low-pass filter for the DC value from T2.

The T1 working current is decided by an external current source at the input Ib. The circuit is based on multiple current mirrors. The current is reflected from T2 to T1 and T5, and the current through T4 is reflected to T3. In the current mirrors, the gate length of T2, T1 and T5 should be equal and the gate length of T4 and T3 should be equal. To simplify we choose to let all NMOS transistors to have the same width and length, and similarly the PMOS transistors to have the same width and length. Then all the local currents will be equal to the reference current Ib. (In an actual realization, we want currents through T2, T4 and T5 to be minimal in order to save power. Proper current in T1 and T3, will be achieved through the choice of the width ratio of the current mirrors.)

Parameters:
We will focus on the amplification of a signal at 1MHz. During noise analysis, we calculate the noise level between 0.8MHz and 1.2MHz. Let the input signal have an amplitude of 100uV. (During .ac and .noise we set the amplitude to 1V).

Initially we let the NMOS transistor lengths be 0.35µm and the PMOS transistor length to be 2µm. The NMOS transistors may have a width of 35µm and the PMOS transistors 20µm width. We use the transistor models MODN and MODP and let VCC be 3.3V. Start by giving Cb a low value. R can be set to 10kΩ. We start with a bias current Ib = 10µA.

a) (.ac) How large must Cin be to not mute the output signal more than about 10% of the maximum (for a huge capacitor)? Generate a logarithmic figure with Cin on the x-axis and signal strength on the Y-axis. Simulate with Cin values from 100fF to 10nF. Find a value for Cin and use it for the following subtasks.

b) (.noise) How large must R be to not contribute significantly (<10%) of the total noise? Use ".MEAS NOISE N_r1_onoise FIND V(r1)/V(onoise) AT 1Meg" to find the relation between R1 noise and total noise. Let the resistance vary between 0.1Ohm and 1GOhm. Generate a logarithmic figure with r1 on the x-axis. You will get a bell-shaped curve with minimum at low and high resistor values. One of these regions is not usable. Check the gain (and inoise) and explain why. Find the usable resistance where V(r1)/V(onoise) = 0.1. The R and C form a high-pass filter for our signal with corner frequency fc=1/(2*pi*R*C). Calculate the corner frequency for the C and R you selected and confirm that fc is below our signal frequency of 1MHz. Decide on a value for R and use it in the following subtasks.

c) (.noise) What does the Cb do? By increasing the value of Cb you can significantly reduce the noise while the signal gain is almost unchanged. Show this by simulating the input noise, output noise and the gain for values of Cb from 1fF to 1uF. Make plots of these with Cb on the x-axis. How much noise reduction can we achieve with large Cb and how large must Cb be to achieve this? Decide on a value for Cb and use it in the following subtasks.

$$V_{in}^2 = 4kT\gamma\left(\frac{1}{g_{m1}} + \frac{g_{m3}}{g_{m1}^2}\right)$$

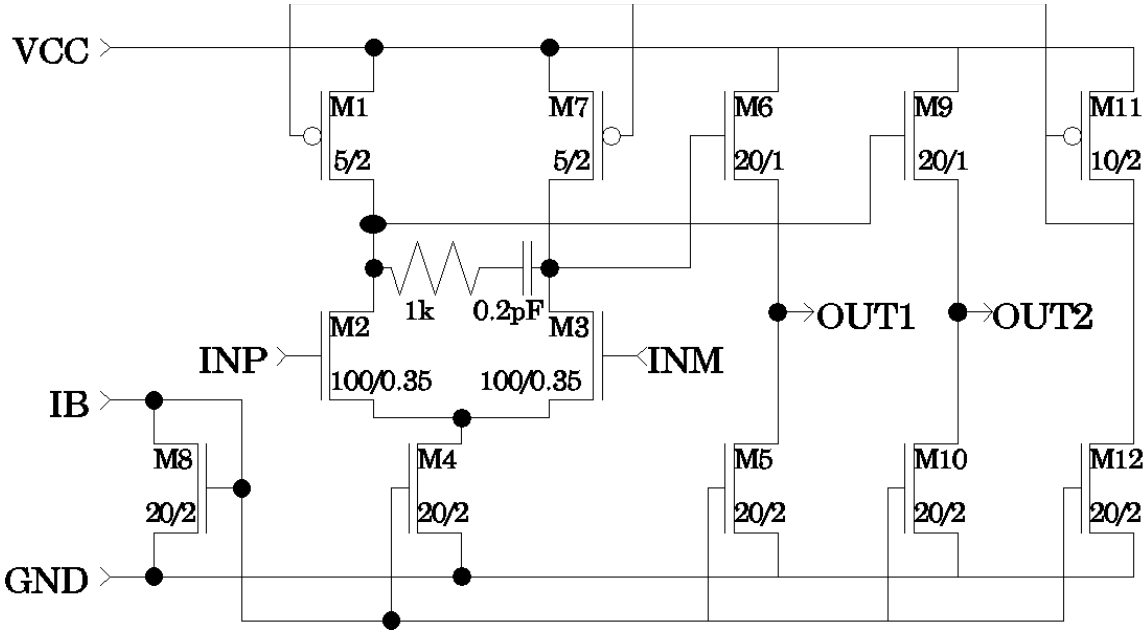
d) (.noise) According to theory (equation above) the equivalent input noise can be reduced by increasing the *gm* of T1 and/or reducing the *gm* of T3. (Will be discussed in FET-lecture.) Show this through simulation by **i)** doubling the width of the NMOS transistors, **ii)** the length of the NMOS transistors, **iii)** the PMOS transistor width and iv) length of the PMOS transistor. Find the output noise, equivalent input noise as well as the gain for these 5 setups (reference + 4 variations) at 1MHz and put them up in a table. A table example is given below.

e) (.noise) Increase the power Ib in steps of 10µA from 10µA to 100µA, and find the output noise, equivalent input noise and gain at 1MHz. Plot the gain, output noise and equivalent input noise as a function of current. Here, the increased current gives a lower gain. Still it gives an advantage when it comes to noise. Explain why based on your simulation results.

Example table for subtask d): Spot values at 1 MHz			
	Output noise	Equivalent input noise	Gain
Ref			
i) 2 WN			
ii) 2 LN			
iii) 2 WP			
iv) 2 WN			

5. CMOS amplifier with differential input and output

In this task, we modify the amplifier from task two so that we have differential output.



Use the amplifier in open loop i.e. as it is above without external feedback resistors etc.

a) Find the gain for i) INP (.ac analysis) to OUT1 and OUT2, ii) for INM to OUT1 and OUT2, iii) the differential gain (.ac analysis) , iv) output noise (.noise analysis) with

source on INP, output noise with source on INM and v) equivalent input noise (.noise analysis). In all cases have a 50µA current bias.

b) Set up a simulation to find the effects of noise from the supply voltage VCC. (Note: This is a noise coupling simulation. Hence you should run an .ac simulation and not a .noise simulation.) Find impact on each of the outputs individually and on the difference between the outputs (Note! Subtract in the simulator). Do the same simulation first where M2 and M3 are identical (as defined above).

In the testbench you have been given, the common mode voltage of the inputs has a ramp behaviour. When you inspect the outputs, you will see that the gain is larger for some input common mode voltages than others. Choose a common mode input voltage some place in the range where the gains are at the largest.
In all cases you have that INP_DC = INM_DC = to the value you found above.

Let VCC_DC = 3.3V. Table for the AC setups for subtask a), b) and c).

	INP_AC	INM_AC	VCC_AC	sim. mode	Look for…
a) i)	1	0	0	.ac	OUT1, OUT2, OUT1-OUT2
a) ii)	0	-1	0	.ac	OUT1, OUT2, OUT1-OUT2
a) iii)	1	-1	0	.ac	OUT1, OUT2, OUT1-OUT2, OUT1+OUT2
a) iv)	1	0	0	.noise	inoise(INP) => onoise(OUT1), inoise(INP) => onoise(OUT2), gain for both cases above
a) v)	1	-1	0	.noise	Inoise(INP) => onoise(OUT1), gain,
b)	0	0	1	.ac	OUT1, OUT2, OUT1-OUT2
c)	0	0	1	.ac	OUT1, OUT2, OUT1-OUT2

c) Repeat b) but with the width of the M2 1% greater than the width of M3. Put the results in a table and comment.
Hint: In case b) the difference should be zero while the actual result is a very low value given by the least significant bits of the number representations.

d) Try to specify the variation in power consumption at VCC when the input signal is a 1MHz sine with amplitude 10mV. Use a transient simulation.