

INF4420

A Brief Summary of Prerequisite Analog Design

Jørgen Andreas Michaelsen and Dag T. Wisland
Spring 2019



Introduction (I)

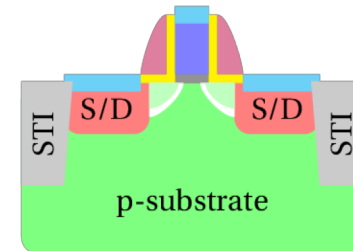
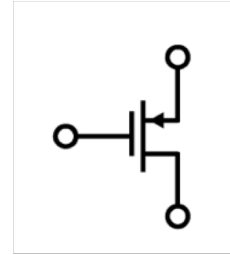
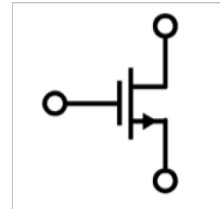
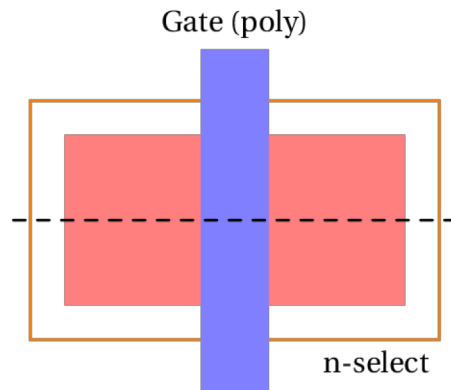
- Why recap previous curriculum?
- INF4420 builds on previous courses
 - Mainly INF3410 (Analog Microelectronics)
 - INF3400 (Digital Microelectronics)
 - These courses again build on previous courses (IN1080, etc.)
- We'll try to keep a practical and hands-on approach in this run through

Introduction (II)

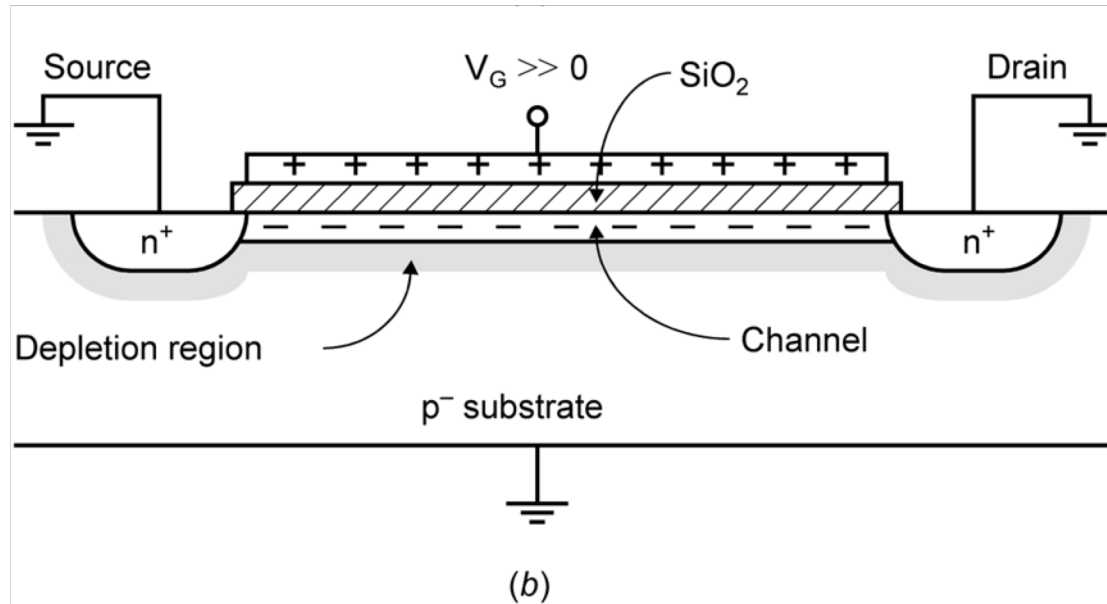
- There will be some new concepts towards the end of the lecture
 - This is added to help your understanding of the course material (not part of the curriculum)

MOSFETs (I)

- MOSFET—metal oxide semiconductor field effect transistor
- CMOS—complementary metal oxide semiconductor



MOSFETs (II)



Digital CMOS (I)

- The transistor is used as a switch to build logic functions
- Somewhat simplified:
 - When the gate voltage is a logic high (we will denote this as '1') the switch conducts (i.e. the channel from source to drain has low resistance)
 - When the gate voltage is a logic low (we will denote this as '0') the switch does not conduct (i.e. the channel from source to drain has high resistance)
- We know how to use this to build basic logic functions such as AND, OR, NOT, NAND, NOR, etc.

Digital CMOS (II)

- Even digital systems are never purely digital
 - We need input and output (I/O)
 - Which absolute voltage levels counts as a '1' and which counts as a '0'
 - Schmitt triggering
 - As speed of the digital I/O increase, this becomes *very* complex
 - Power management
 - Typically the requirement is $\pm 10\%$ supply voltage even with large transient currents
 - Clock management and generating clocks
 - For digital timing is key (how long is the clock period?)
 - May want to dynamically change clock speed on the fly (also supply voltage)

Analog CMOS (I)

- The somewhat simplified view of analog CMOS design
 - We use the transistor as an amplifier, which in turn can be used to build more complex amplifiers
- Amplifiers in this context can mean different things
 - We may have an input *voltage* which we want to gain up to a larger *voltage* (this is a very common scenario)
 - In some cases we do not need gain, but we want to drive a low impedance
 - In general inputs may be voltage or current, and outputs may be voltage or current

Analog CMOS (II)

- If the digital transistor is a switch, what is a useful model of the analog transistor (amplifier)?
 - Voltage controlled resistor (triode), similar to the digital switch, but we care about the channel resistance (rather than very low resistance or very high resistance). This is usually not the desired operating region for analog amplifiers.
 - **Voltage controlled current source, we control the current flowing from drain to source by means of the gate voltage. A *transconductance amplifier*.**

Voltage controlled current source (VCCS)

- Ideal current source
 - Ohm's law: $V = R \times I$
 - The ideal current source makes sure I is constant, irrespective of voltage or loading conditions
- Real current sources have finite output impedance
 - Approximate the current source as an ideal current source with a resistor in parallel
 - We now have a *useful* model of the “analog” transistor at DC

Small signal model (I)

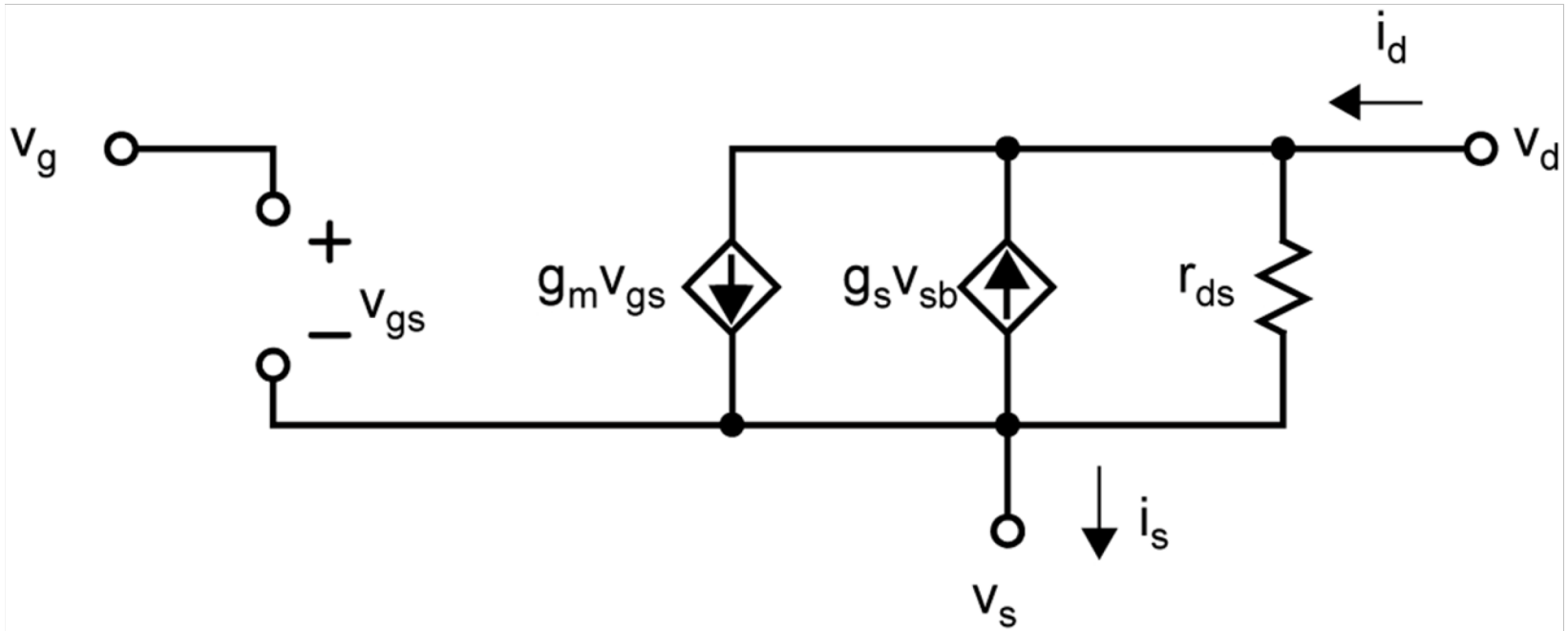
- Supposing we have voltages on the terminals of the transistor to properly bias it as a VCCS (we will come back to biasing in a few slides), we can use a small signal model to analyze the circuit as an amplifier
- If we are not careful with correct biasing, the transistor will behave more as a resistor than a current source, and the model we present here cannot be used

Small signal model (II)

- Meaning, we are only interested in the derivative of the voltages and currents, i.e. we analyze how the output *changes* as a function of the *change* in input
- Note: we need to be careful, because if the signals are large enough, the biasing also changes (but, it works even for practical design, and is *very* useful)
- This is what an AC simulation does

Small signal model (III)

- Fig. 1.17

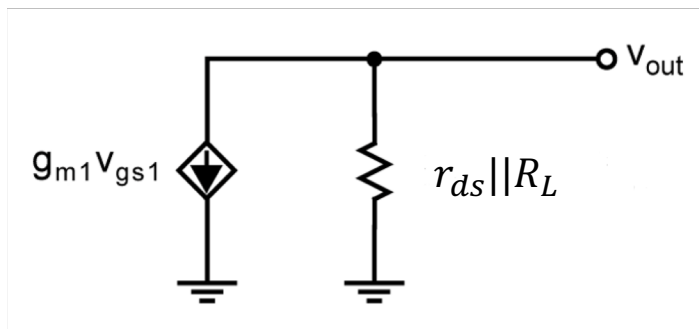


Transistor amplifiers

- The transistor itself is already a transconductance amplifier (voltage input, current output)
- If we want a voltage input and voltage output amplifier, we need a load to convert the output current to a voltage, i.e. a resistance (or more generally an impedance)
 - The transistor open circuit does have a finite output impedance, so the output voltage will change, but this is not useful in a practical circuit. This is called the self gain of the transistor, and is an upper limit to the achievable gain, $g_m \times r_{ds}$
 - Resistor load or transistor (active) load

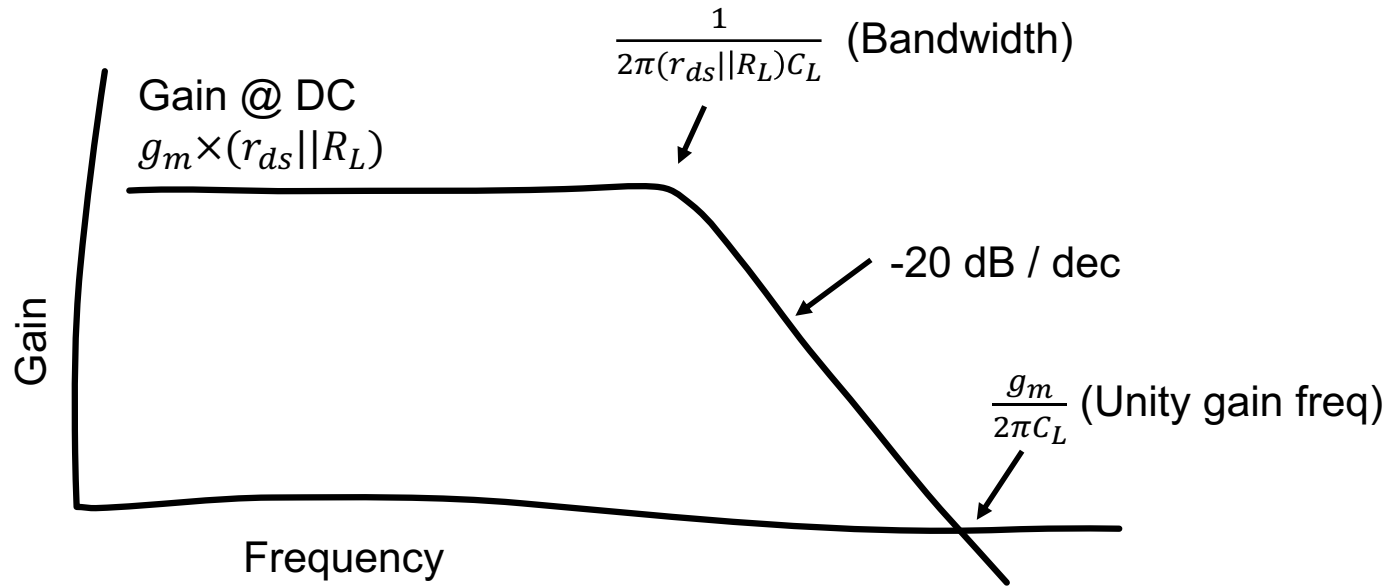
Common source (CS) amplifier (I)

- The transistor with the output and load at the drain is called a common source (CS) amplifier, because in the small signal, the source voltage is constant (its derivative is 0)



- Gain is $g_m \times (r_{ds} || R_L)$
- Capacitive loading (typically), C_L
 - $(r_{ds} || R_L)$ and C_L forms a pole

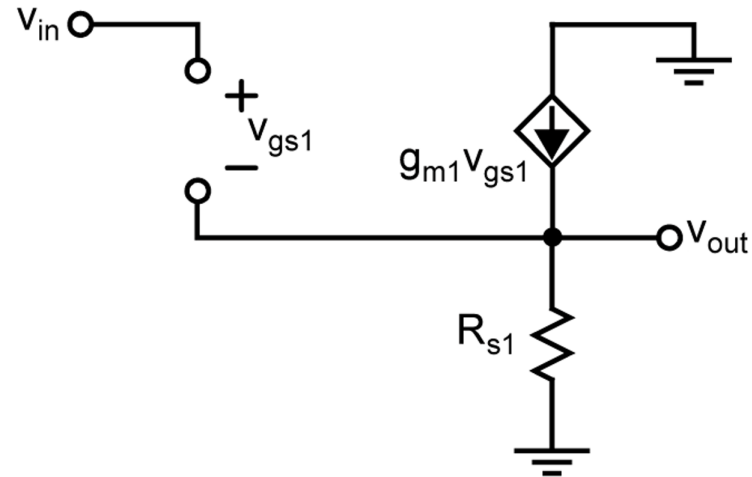
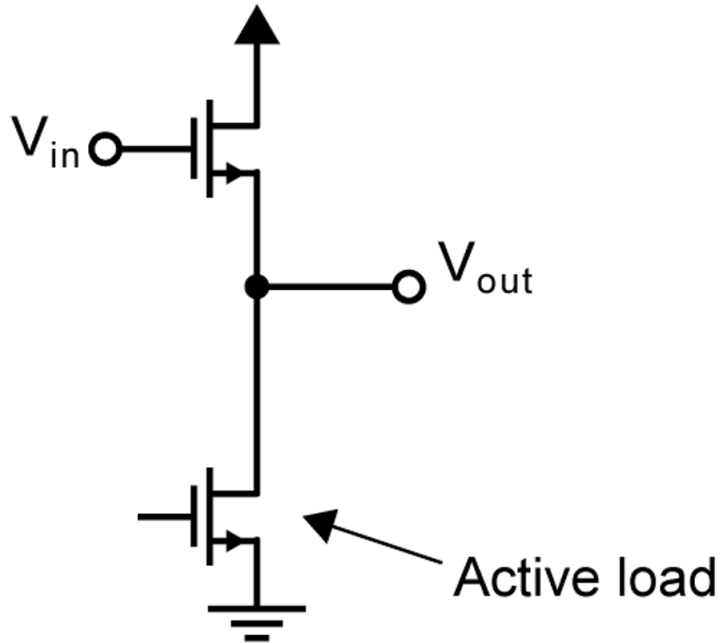
Common source (CS) amplifier (II)



Common drain (or source follower) amplifier (I)

- The source follower (SF) amplifier is typically used for voltage buffering
 - The gain is always less than one (ideally unity gain)
 - i.e. for driving low impedance
 - A CS amplifier is not suitable for driving low impedance because its gain is proportional to the load impedance

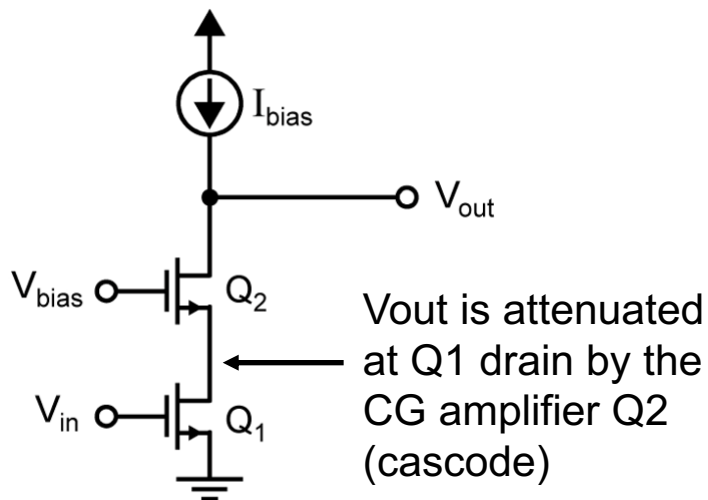
Common drain (or source follower) amplifier (II)



Cascoding (or common gate)

- There are three basic single transistor amplifiers.
So far: CS, CD (or SF)
- Common gate (CG). For analog design, almost always used with a CS amplifier to improve its output resistance:
Cascode

Cascoding (II)



The common gate, or cascode, attenuates the signal swing at the drain of the CS. Effectively improving the output resistance of the CS by the gain of the CG ($g_m r_{ds}$), so the output resistance becomes $g_m r_{ds}^2$

Designing an amplifier (I)

- Specifications
 - $UGF = 5 \text{ GHz}$
 - Load = 100 fF
 - Gain @ DC = 4 V / V
- Choose the topology (SF, CS, CG) and the load
- Calculate the required parameters (for biasing, W, L)

Designing an amplifier (II)

- Resistively loaded CS
 - Gain requirement is low, so a cascode is not needed and we can use a resistive load rather than an active load
 - We also need to consider the output common mode voltage, which is set by the resistive load (R_L) and the bias current (I_D)
- Hand-calculations
 - $g_m = \text{UGF} \times 2\pi \times C_L = 5 \text{ GHz} \times 2\pi \times 100 \text{ fF} \approx 3.14 \text{ mS}$
 - $R_O = \frac{\text{GAIN}}{g_m} = 4 / 3.14 \text{ mS} \approx 1273.88 \Omega$

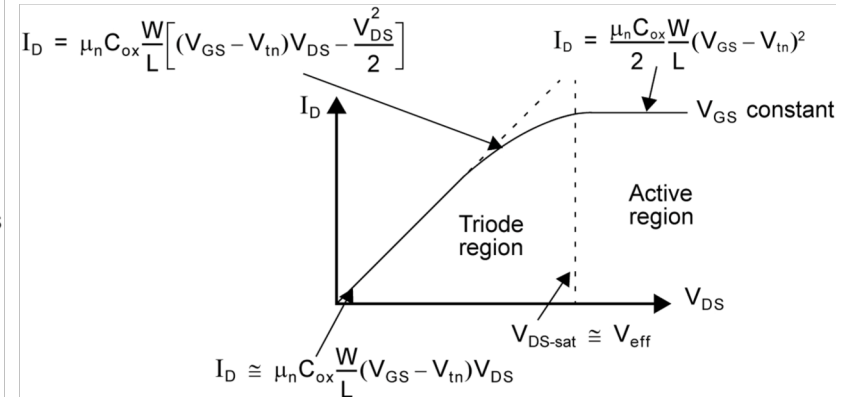
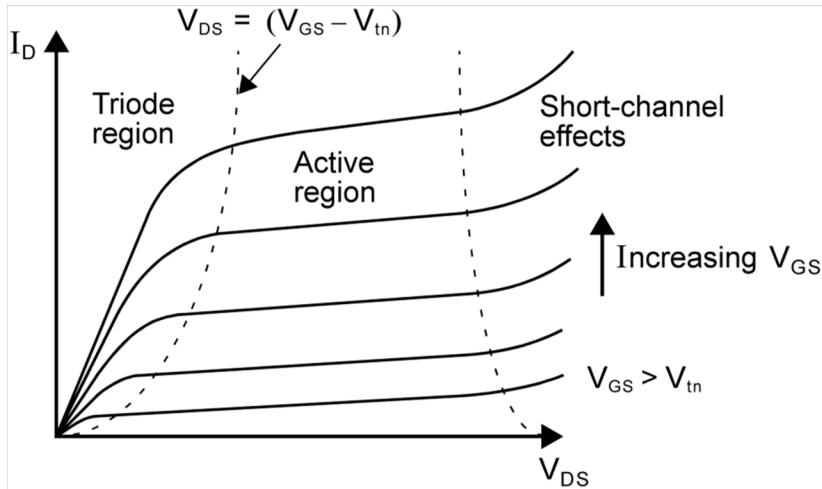
Designing an amplifier (III)

- We now need to
 - Pick the physical parameters of the transistor (W / L)
 - Choose the correct biasing (indirectly the gate voltage, but we bias using a bias current to derive the gate voltage)
- There are several methods to do this, we will design based on the overdrive voltage (V_{ov}), which is V_{eff} in the textbook
 - For a “square law device”: $V_{ov} = V_{gs} - V_{th} = \frac{2I_D}{g_m}$ (See eqn. 1.78)
 - This is referred to as the $\frac{g_m}{I_D}$ methodology

Biasing (I)

- We have analyzed CS, CD, and CG with some assumptions to make it more manageable and help our understanding
 - Small signal (we only care about the changes, derivative, gain)
 - We assume that the relevant small signal parameters (such as g_m) are constant
 - We assume that the transistors are biased such that it behaves as a voltage controlled current source
- We need to know when these assumptions are correct for our circuits to function as we intended

Biasing (II)



Design based on g_m/I_D (I)

- Square law equations are only useful for building intuition about how transistors work. *Do not use* for hand calculating the biasing of the transistor
 - The equations do not capture the complex (non-linear) device behavior
 - Required parameters (such as V_{th}) are not a single number nor constant
 - See BSIM4 model equations for details

Design based on g_m/I_D (II)

- Why?
 - We can design based on relevant parameters for the design
 - $\frac{2I_D}{g_m}$ (or informally, the overdrive voltage) is the key parameter for design
- Easy to estimate the required current for a given specification
 - I.e. the system level specification dictates a circuit level specification for gain and bandwidth, and we can quickly estimate the power consumption

Transistor speed, f_T

- Until now, we have considered the transistor at DC
- f_T is commonly used as the metric for the intrinsic speed of the transistor
- Defined as $f_T = \frac{g_m}{2\pi C_{gs}}$
- Choosing a low $\frac{2I_D}{g_m}$ for good efficiency (less current) implies a larger transistor ($\uparrow W$)
 - More device parasitics. C_{gs} increases and f_T decreases

Design based on g_m/I_D (III)

- Choosing a low $\frac{2I_D}{g_m}$ implies good efficiency, because we are using a low bias current and getting a (relatively) large change in current
- Choosing a high $\frac{2I_D}{g_m}$ results in a higher f_T . I.e. there is a trade-off between current efficiency and speed
- A common figure of merit (FoM) is $\frac{g_m}{I_D} \times f_T$

Design based on g_m/I_D (IV)

- Choose an appropriate device length
 - Do we need high gain ($\uparrow L$) or high f_T ($\downarrow L$)
- Choose $\frac{2I_D}{g_m}$ based on a speed vs efficiency trade-off
 - Also impacts available signal swing and noise
 - This gives the bias current, I_D (we already know g_m)
- To determine W (the final step), we need to generate a lookup table (using the simulator) plotting I_D vs $\frac{2I_D}{g_m}$ for a “unit” size transistor (we only do this once per device and L)

Designing an amplifier (IV)

- We can now complete the amplifier design
- We have to choose an appropriate $\frac{2I_D}{g_m}$ based on the speed / efficiency trade-off
- Choosing $\frac{2I_D}{g_m} = 200 \text{ mV}$ gives
 - $I_D = 314 \text{ }\mu\text{A}$
- Use the charts (or the simulator directly) to find W for 314 μA and 200 mV

Square law vs g_m/I_D

- g_m/I_D is not covered in previous courses and is not required for this course either.
- Transistor behavior requires an extensive set of equations, and parameters with no direct physical connection (obtained from fitting observed device behavior). See BSIM4 manual.
- The simplistic square law equations are good for building intuition as to how the transistor behaves.
- Key idea is that we can capture complex device behavior from one lookup table (generated by simulation). We can use this for hand calculating the transistor biasing and size.

Hand calculations

- What do we mean by hand calculations?
- Less useful hand calculations
 - Exact V_{gs} to get a given I_D or g_m
- Useful hand calculations
 - Required g_m for a given UGF and C_L specification
 - See the amplifier design example