# INF2270, exercise in combinational logic two's complement arithmetic: example solution 

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## Task 1

Figure 1 shows a cascade of half adders that increment a 9 -bit signed integer by 1. The bus notation ' $\mathrm{C}(7: 0), 1$ ' lables the bus cables from the MSB to the LSB, with a constant input 1 for the LSB and recursive connections for the carry out of the first 8 bits to the next higher bit. The XOR and AND gate represent 9 gates in parallel. The first half adder receives a constant 1 as carry in bit and thus, 1 is added to the the input $\mathrm{a}(8: 0)$ and the result S is equal to $\mathrm{a}+1$.

## Task 2

$$
\begin{array}{rlrr}
11011 & = & 27-32 & = \\
1110111 & = & -5 \\
1010101 & = & 85-128 & = \\
-9 \\
100000001 & = & -437-512 & = \\
111111111 & = & -255 \\
111-512 & = & -1
\end{array}
$$

What is the corresponding 8 bit two's complement number for:

$$
\begin{aligned}
& -31 \hat{=} \quad-31+256=225=11100001 \\
& -32 \hat{=} \quad-32+256=224=11100000 \\
& -127 \hat{=}-127+256=129=10000001 \\
& -128 \hat{=}-128+256=128=10000000 \\
& -77 \hat{=} \quad-77+256=179=10110011 \\
& 22 \hat{=} \quad 22 \quad=00001010
\end{aligned}
$$



Figure 1: A circuit that increments a 9-bit integer by 1

