

INF2270, another exercise in combinational logic

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Abstract

In this exercise you will get acquainted with diglog, have a look at a part of the mandatory exercise in task 1 and another combinational logic circuit in task 2.

Task 1

Use the diglog simulator to write and read content to the included memory cell SRAM8K “manually”. Get a ‘feel’ for the control signals. Use 8 toggle switches (cell SWITCH) to provide input (bottom, LSB on the right), 13 for the address lines (left, LSB on top), and three more for the control signals (top). Use 8 LED cells to check the input/output lines from the memory. You will also need to use a tristate buffer (cell 74244), to separate your SWITCH input from the I/O lines of the memory, for when the memory content should drive those lines (i.e. \overline{OE} is low). To check if your storing actions have the right effect you may also go into the configuration menu of the SRAM8K and look at individual memory cells there by writing an address into field ‘Address (DEC)’ or ‘Address (hex)’. Try to store at least two different values at two different addresses and check if you can make them reappear on the memory I/O lines thereafter.

The control signals of SRAM8K are equivalent to the ones discussed in the lecture SRAM:

- The pin with the triangle is actually not a clock but a active low chip select (\overline{CS} in the lecture/compendium).
- The pin labeled ‘R’ is actually active low and equivalent to the \overline{WE} in the lecture/compendium.
- OE is also active low and equivalent to \overline{OE} in the lecture/compendium.

There are two active low ‘enable’ signals (the tristate buffer is driving the output if the control signal is low) for the tristate buffer 74244 to let you control the 4 LSBs (i.e. bits 3:0, LSB 0 on the very top) and the four MSBs (i.e. bits 7:4, MSB 7 on the very bottom). Note that you actually do not need to worry about the numbering of the pins here, as long as you connect the correct input

to the correct output and know that the top 4 I/Os are controlled by the enable signal on top, and the bottom four by the enable signal at the bottom.

Note that if you do a mistake with the control signals of the tristate buffer 74244 and the memory SRAM8K you may try to drive the memory I/O lines to two different potentials. If such a conflict occurs you'll get a red bar at the bottom left of the simulation window and the corresponding line will get coloured dark red. Try to do this on purpose to see the effect!

Task 2

Design and simulate a comparator for two 4 bit two's complement input numbers a and b. There three output bits. One should be high if $a > b$ another if $a = b$ and the last if $a < b$.

Hint:

1. Do not optimize this for specifically 4 bits. Instead compose your solution of 4 identical cells (possibly with the exception of the most significant bit (MSB) for two's complement numbers), such that you can easily extend your solution to an arbitrary number of bits.
2. Try to do this for unsigned binaries first and then think what you will have to change concerning the first 'sign' bit for two's complement.

In order to test your circuit you may design it with the diglog simulator.