INF2270, example solution: more detailed pipelining speed-up and a counter with synchronous load

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Pipelined Processor Absolute Speed-Up

Part 1:

1. $\frac{1\text{GHz}}{4\text{CPI}} = 250\text{MIPS}$

2. $\frac{900\text{MHz}}{1.2\text{CPI}} = 750\text{MIPS}$

Part 2:

1. 1/259ps=3.86GHz
   3.86GIPS
   $\frac{3.86\text{GIPS}}{250\text{MIPS}} = 15.44$ times faster

2. $\frac{3.86\text{GHz}}{1.2\text{CPI}} = 3.22\text{GIPS}$
   $\frac{3.22\text{GIPS}}{250\text{MIPS}} = 12.88$ times faster

3. $\frac{3980\text{ps}}{16} + 20\text{ps} = 269\text{ps}$
   $\frac{1}{269\text{ps}} = 3.72\text{GHz}$
   $\frac{3.72\text{GHz}}{1.2\text{CPI}} = 3.10\text{GIPS}$

Synchronous Counter with load

Figure 1 shows one possible solution. Remember that a JK flipflop works like a T-flipflop if J and K are shortened. This is the case if LD=0 since the same signal is routed to both J and K through the multiplexers and the circuit becomes equivalent to the synchronous counter without a LD control signal.

When LD=1, on the other hand, K receives the inverted J signal and J is shorted to the input. Thus, on the next clock edge, the value I is loaded into the counter.
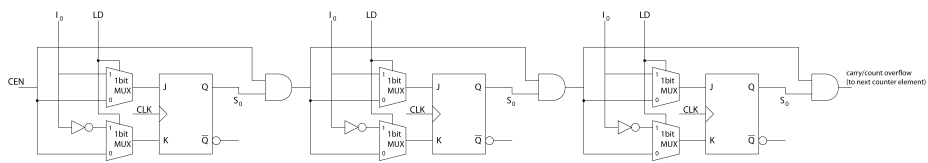
Figure 1: A counter with LD and CE control signals