Introduksjon til effektforbruk

Effektforbruk:

$$P(t) = i_{DD}(t) \cdot V_{DD}$$

Effektforbruk over en tidsperiode T:

$$E = \int_0^T i_{DD}(t) \cdot V_{DD}\, dt$$

Gjennomsnittelig effektforbruk over en tidsperioden:

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t) \cdot V_{DD}\, dt$$

Statisk effektforbruk:

1. AV strøm.
2. Tunnellering.
3. Pn-overganger.
4. Lekkasje i transistorer som overstyres.

Dynamisk effektforbruk:

1. Opp- og utladning av kapasitanser.
2. Kortslutningsstrøm.

Svak inversjon

Når gate source spenningen er lavere enn terskelspenningen:

$$I_{ds} = I_{ds0} e^{\frac{V_{gs}-V_t}{nU_t}} \left(1 - e^{-\frac{V_{ds}}{U_t}} \right)$$

der:

$$I_{ds0} = \beta U_T^2 e^{1.8}$$

$$n = \text{slope factor}$$

Korte kanaler og kraftig elektrisk felt gir "drain induced barrier lowering" (DIBL):

$$V_t' = V_t - \eta V_{ds}$$

Oppgave 2.11

Finn strømlekkasje i svak inversjon i en inverter ved romtemperatur når inngangen er 0. Anta at $\beta n = 2\beta p = 1 mA/V^2$, $n = 1.4$ og $|Vtp| = Vtn = 0.4V$. Anta at bodyeffekt og DIBL koeffisient $\gamma = \eta = 0$.

$$I_{ds} = I_{ds0} e^{\frac{V_{gs}-V_t}{nU_t}} \left(1 - e^{-\frac{V_{ds}}{U_t}} \right)$$

$$= \beta U_T^2 e^{1.8} e^{\frac{-V_t}{nU_t}} \left(1 - e^{-\frac{V_{ds}}{U_t}} \right)$$

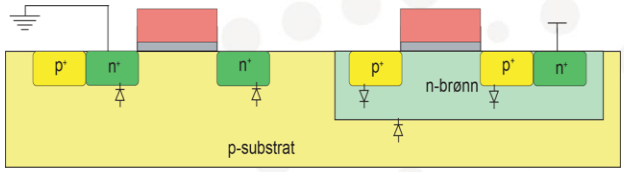
$$\approx 4.1 \cdot 10^{-6} e^{\frac{-0.4}{1.4 \cdot 0.026}}$$

$$\approx 4.1 \cdot 10^{-6} \cdot 1.69 \cdot 10^{-5} A$$

$$\approx 6.9 \cdot 10^{-11} A$$

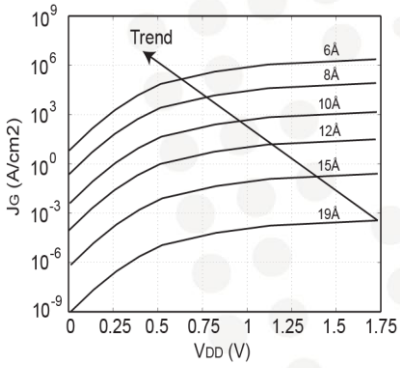
$$= 69\ pA$$

Lekkasje i pn-overganger



$$I_D = I_S \left(e^{\frac{V_D}{U_T}} - 1 \right)$$

Tunnellering



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Effektforbruk

Effektforbruk:

$$P(t) = i_{DD}(t) \cdot V_{DD}$$

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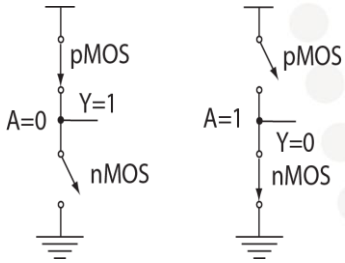
Dynamisk effektforbruk:

1. Opp- og utladning av kapasitanser.
2. Kortslutningsstrøm.

Statisk effektforbruk



AV strøm:

$$I_{statisk} = I_{ds0} e^{\frac{-V_t}{nU_t}} \left(1 - e^{-\frac{V_{DD}}{U_t}}\right)$$

Statisk effektforbruk:

$$P_{statisk} = I_{statisk} V_{DD}$$

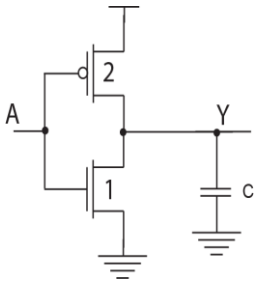
Dynamisk effektforbruk

Gjennomsnittelig dynamisk effektforbruk:

$$P_{dynamisk} = \frac{1}{T}\int_0^T i_{DD}(t)\cdot V_{DD}\,dt$$

$$= \frac{V_{DD}}{T}\int_0^T i_{DD}(t)\,dt$$

Inverter med last:



Over tidsperioden T:

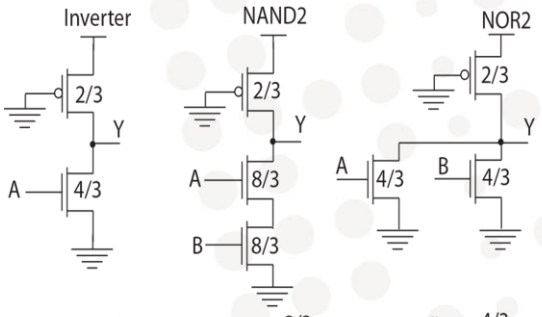
$$P_{dynamisk} = \frac{V_{DD}}{T}\left[Tf_{SW}\,CV_{DD}\right]$$

$$= CV_{DD}^2 f_{SW}$$

Tar hensyn til aktivitet:

$$P_{dynamisk} = \alpha CV_{DD}^2 f_{SW}$$

Pseudo nMOS

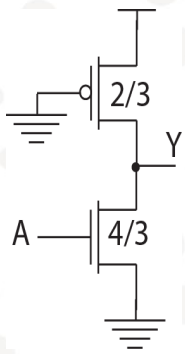


Inverter	NAND2	NOR2
$g_u = 4/3$	$g_u = 8/3$	$g_u = 4/3$
$g_d = 4/9$	$g_d = 8/9$	$g_d = 4/9$
$g_{avg} = 8/9$	$g_{avg} = 16/9$	$g_{avg} = 8/9$
$P_u = 18/9$	$P_u = 30/9$	$P_u = 30/9$
$P_d = 6/9$	$P_d = 10/9$	$P_d = 10/9$
$P_{avg} = 12/9$	$P_{avg} = 20/9$	$P_{avg} = 20/9$

Pseudo nMOS inverter

Antar μn = 2μp og opptrekk ¼ av nedtrekk:

$$W_n = \frac{4}{3} W_{n_{enhet}} \qquad W_p = 2\frac{1}{4}\frac{4}{3}$$
$$= \frac{4}{3} \qquad = \frac{2}{3}$$

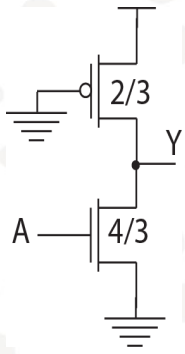


Antar $W_n = C_{inngang}$ og $W_p = C_{gate\_pMOS}$:

$$g_u = \frac{W_n}{W_p + \frac{1}{2}W_p} \qquad g_d = \frac{W_n}{\left(W_n - \frac{1}{2}W_p\right) + 2\left(W_n - \frac{1}{2}W_p\right)}$$
$$= \frac{\frac{4}{3}}{\frac{2}{3}+\frac{1}{3}} \qquad = \frac{\frac{4}{3}}{3\left(\frac{4}{3}-\frac{1}{3}\right)}$$
$$= \frac{4}{3} \qquad = \frac{4}{9}$$

Parasittisk tidsforsinkelse:

$$P_u = R_{opptrekk}\, C_{intern} \qquad P_d = R_{nedtrekk}\, C_{intern}$$
$$= R_p\left(\frac{2}{3}+\frac{4}{3}\right)C \qquad = R\left(\frac{2}{3}+\frac{4}{3}\right)C$$
$$= 3R\,2C \qquad = R\,2C$$
$$= 2\tau \qquad = \frac{2}{3}\tau$$



Pseudo nMOS NAND2

Motstand i opptrekk:

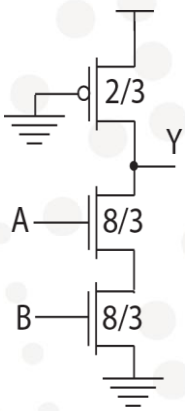
$$R_p = 2\left(\frac{1}{W_p}\right)R$$
$$= 3R$$

Motstand i nedtrekk:

$$R_n = W_n^{-1}$$
$$R_{nMOS\_kjede} = \left(W_n^{-1} + W_n^{-1}\right)R$$
$$= \frac{2}{W_n}R$$
$$= \frac{3}{4}R$$

Dimensjonering:

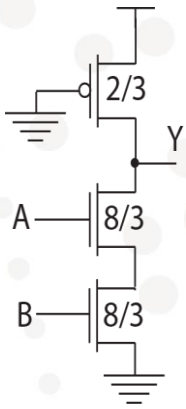
$$\frac{2}{W_n}R = \frac{1}{4}R_p$$
$$\frac{2}{W_n}R = \frac{1}{4}3R$$
$$W_n = \frac{8}{3}$$



Logisk effort:

$$g_u = \frac{W_n}{W_p + \frac{1}{2}W_p}$$
$$= \frac{\frac{8}{3}}{\frac{2}{3}+\frac{1}{3}}$$
$$= \frac{8}{3}$$

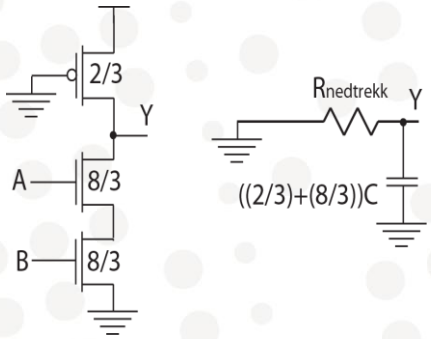
$$g_d = \frac{W_n}{3\left(\left(\frac{1}{W_n}+\frac{1}{W_n}\right)^{-1} - \frac{1}{2}W_p\right)}$$
$$= \frac{W_n}{3\left(\frac{1}{2}W_n - \frac{1}{2}W_p\right)}$$
$$= \frac{\frac{8}{3}}{3\left(\frac{4}{3}-\frac{1}{3}\right)}$$
$$= \frac{8}{9}$$



Parasittisk tidsforsinkelse:

$$P_u = R_{\text{opptrekk}}\, C_{\text{intern}}$$
$$= 3R\left(\frac{2}{3}+\frac{8}{3}\right)C$$
$$= 10\,RC$$
$$= \frac{10}{3}\tau$$

$$P_d = R_{\text{nedtrekk}}\, C_{\text{intern}}$$
$$= R\left(\frac{2}{3}+\frac{8}{3}\right)C$$
$$= \frac{10}{3}RC$$
$$= \frac{10}{9}\tau$$

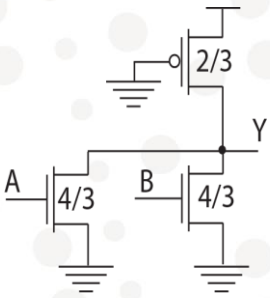


Pseudo nMOS NOR

Logisk effort:

$$g_u = \frac{W_n}{W_p + \frac{1}{2}W_p}$$
$$= \frac{\frac{4}{3}}{\frac{2}{3}+\frac{1}{3}}$$
$$= \frac{4}{3}$$

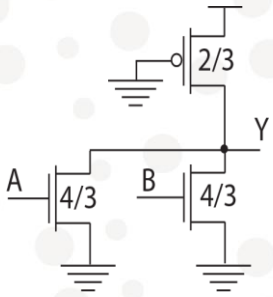
$$g_d = \frac{W_n}{3\left(W_n - \frac{1}{2}W_p\right)}$$
$$= \frac{\frac{4}{3}}{3\left(\frac{4}{3}-\frac{1}{3}\right)}$$
$$= \frac{4}{9}$$



Parasittisk tidsforsinkelse:

$$P_u = R_{opptrekk}\, C_{intern}$$
$$= 3R\left(\frac{2}{3}+\frac{4}{3}+\frac{4}{3}\right)C$$
$$= 10\,RC$$
$$= \frac{10}{3}\tau$$

$$P_d = R_{nedtrekk}\, C_{intern}$$
$$= R\left(\frac{2}{3}+\frac{4}{3}+\frac{4}{3}\right)C$$
$$= \frac{10}{3}RC$$
$$= \frac{10}{9}\tau$$



Eksempel

Gjennomsnittelig logisk effort for NOR port:

$$g_{avg} = \frac{8}{9}$$

Kjedeeffort:

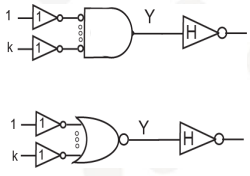
$$F = GBH$$
$$= \frac{8}{9}H$$

Optimal porteffort:

$$f^{\wedge} = \sqrt{\frac{8}{9}H}$$

Optimal inngangskapasitans:

$$C_{inngang} = \frac{C_{ekstern}\cdot g}{f^{\wedge}}$$
$$= \frac{\frac{8}{9}H}{\sqrt{\frac{8}{9}H}}$$
$$= \frac{2\sqrt{2H}}{3}$$



Dette gir for NOR port:

$$W_p = \frac{W_n}{2} = \frac{\sqrt{2H}}{3}$$

Effektiv motstand:

$$R_{opptrekk} = 2W_p^{-1} \quad R_{nedtrekk} = \left(W_n - \frac{1}{2}W_p\right)^{-1} R$$
$$= \frac{6}{\sqrt{2H}} = \left(\frac{2\sqrt{2H}}{3} - \frac{1}{2}\frac{\sqrt{2H}}{3}\right)^{-1} R$$
$$= \frac{2}{\sqrt{2H}}R$$

Parasittisk tidsforsinkelse:

$$P_u = \frac{6}{\sqrt{2H}}R\left(\frac{\sqrt{2H}}{3} + k\frac{2\sqrt{2H}}{3}\right)C$$
$$= \frac{6\sqrt{2H}(1+2k)}{3\sqrt{2H}}RC$$
$$= \frac{2(1+2k)}{3}\tau$$

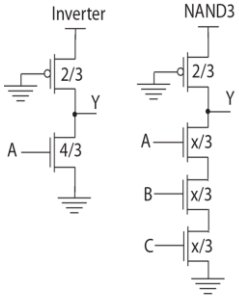
$$P_d = \frac{2}{\sqrt{2H}}R\left(\frac{\sqrt{2H}(1+2k)}{3}\right)C$$
$$= \frac{2(1+2k)}{3}RC$$
$$= \frac{2(1+2k)}{9}\tau$$

Total tidsforsinkelse:

$$D = Nf^{\wedge} + P$$
$$= 2\sqrt{\frac{8}{9}H} + 1 + \frac{4(1+2k)}{9}$$
$$= \frac{4\sqrt{2H}}{3} + \frac{(13+8k)}{9}$$

Oppgave 6.18

Tegn transistorskjema for pseudo-nMOS 3inngangs NAND port. Angi transistorstørrelser og finn logisk effort for nedtrekk og opptrekk og gjennomsnitt for portene.



Inverter	NAND3
$g_u = 4/3$	$g_u = x/3$
$g_d = 4/9$	$g_d = x/9$
$g_{avg} = 8/9$	$g_{avg} = 4x/9$
$P_u = 18/9$	$P_u = (2+x)/3$
$P_d = 6/9$	$P_d = (2+x)/9$
$P_{avg} = 12/9$	$P_{avg} = 2(2+x)/9$

Vi antar at motstanden i opptrekket skal være 4 ganger så stor som motstanden i nedtrekket:

$$R_p = 2\frac{3}{2}R = 3R$$

$$R_{NmosKJEDE} = \left(W_n^{-1} + W_n^{-1} + W_n^{-1}\right)R = \frac{3}{W_n}R$$

Som gir:

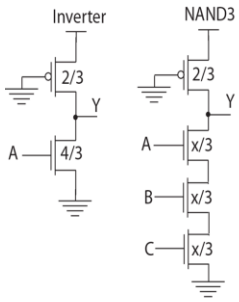
$$\frac{3}{W_n}R = \frac{1}{4}R_p$$

$$\frac{1}{W_n} = \frac{1}{4}$$

$$W_n = 4$$

Effektiv motstand i nedtrekk:

$$R_{nedtrekk} = \left(R_{nMOS\_kjede}^{-1} - R_p^{-1}\right)^{-1} = \left(\frac{W_n}{3} - \frac{1}{2}\frac{2}{3}\right)^{-1}R = R$$

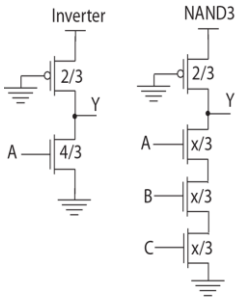


Inverter	NAND3
$g_u = 4/3$	$g_u = x/3$
$g_d = 4/9$	$g_d = x/9$
$g_{avg} = 8/9$	$g_{avg} = 4x/9$
$P_u = 18/9$	$P_u = (2+x)/3$
$P_d = 6/9$	$P_d = (2+x)/9$
$P_{avg} = 12/9$	$P_{avg} = 2(2+x)/9$

Logisk effort:

$$g_u = \frac{W_n}{W_p + \frac{1}{2}W_p} = \frac{4}{\frac{2}{3}+\frac{1}{3}} = 4$$

$$g_d = \frac{W_n}{3\left(\left(\frac{1}{W_n}+\frac{1}{W_n}+\frac{1}{W_n}\right)^{-1} - \frac{1}{2}W_p\right)} = \frac{W_n}{3\left(\frac{1}{3}W_n - \frac{1}{2}W_p\right)} = \frac{4}{3\left(\frac{4}{3}-\frac{1}{3}\right)} = \frac{4}{3}$$



$g_u = 4/3$ $g_d = 4/9$ $g_{avg} = 8/9$ $P_u = 18/9$ $P_d = 6/9$ $P_{avg} = 12/9$

$g_u = x/3$ $g_d = x/9$ $g_{avg} = 4x/9$ $P_u = (2+x)/3$ $P_d = (2+x)/9$ $P_{avg} = 2(2+x)/9$

Parasittisk tidsforsinkelse:

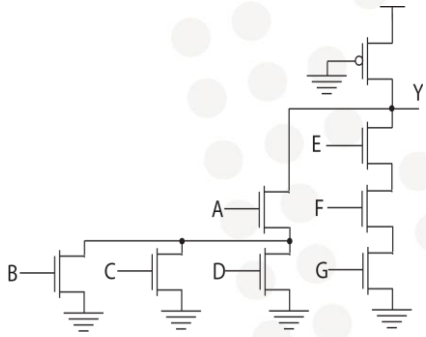
$$P_u = R_{\text{opptrekk}}\, C_{\text{intern}}$$
$$= 3R\left(\frac{2}{3} + 4\right)C$$
$$= 14\,RC$$
$$= \frac{14}{3}\tau$$

$$P_d = R_{\text{nedtrekk}}\, C_{\text{intern}}$$
$$= R\,\frac{14}{3}C$$
$$= \frac{14}{9}\tau$$

Oppgave 6.19

Tegn transistorskjema for en pseudo-nMOS port som implementerer funksjonen

$F = \overline{A(B + C + D) + E \cdot F \cdot G}$.



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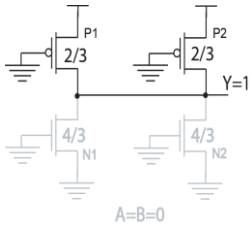
Ganged CMOS



$$g_u = \frac{W_p + W_n}{2W_p + W_p}$$

$$= \frac{\frac{2}{3} + \frac{4}{3}}{2\frac{2}{3} + \frac{2}{3}}$$

$$= 1$$

$$P_u = R_{\text{opptrekk}}\, C_{\text{intern}}$$

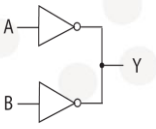
$$= \left(\frac{R_p \cdot R_p}{R_p + R_p} \right) \left(\frac{2}{3} + \frac{2}{3} + \frac{4}{3} + \frac{4}{3} \right) C$$

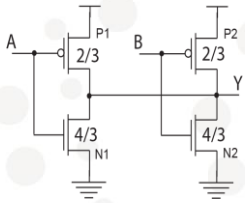
$$= 2R_p C$$

$$= 2 \cdot 2 \cdot \frac{3}{2} RC$$

$$= 6RC$$

$$= 2\tau$$





$$g_d = \frac{W_p + W_n}{\left(W_n - \frac{1}{2}W_p\right) + 2\left(W_n - \frac{1}{2}W_p\right)}$$

$$= \frac{\frac{2}{3} + \frac{4}{3}}{3\left(\frac{4}{3} - \frac{1}{2}\frac{2}{3}\right)}$$

$$= \frac{2}{3}$$

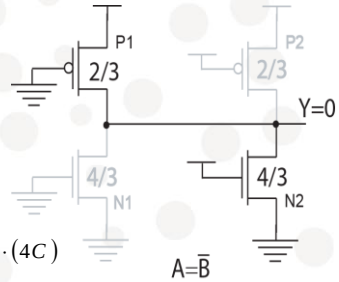
$$P_d = R_{\text{nedtrekk}}\, C_{\text{intern}}$$

$$= \left(W_n - \frac{1}{2}W_p\right)^{-1} R \cdot (4C)$$

$$= \left(\frac{4}{3} - \frac{1}{2}\frac{2}{3}\right) 4RC$$

$$= 4RC$$

$$= \frac{4}{3}\tau$$



$$g_d = \frac{W_p + W_n}{2W_n + 4W_n}$$

$$= \frac{\frac{2}{3} + \frac{4}{3}}{2\frac{4}{3} + 4\frac{4}{3}}$$

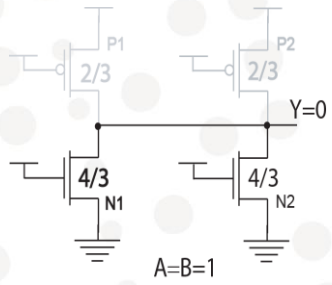
$$= \frac{1}{4}$$

$$P_d = R_{\text{nedtrekk}}\ C_{\text{intern}}$$

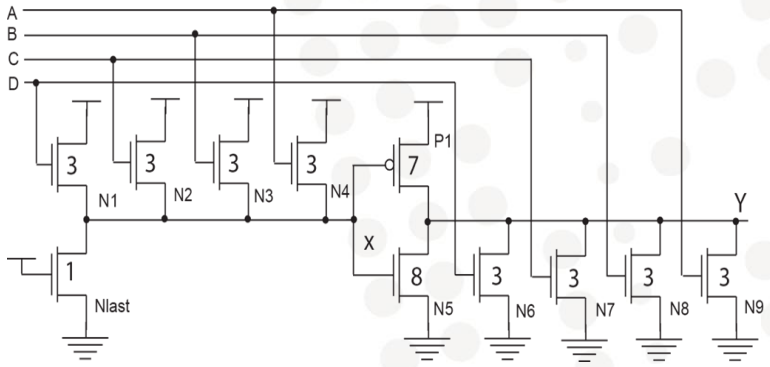
$$= \left(\frac{R_n \cdot R_n}{R_n + R_n}\right) \cdot (4C)$$

$$= 2R_nC$$

$$= \frac{3}{2}RC$$



Source følger opptrekkslogikk



Oppgave 6.25

Sammenlign gjennomsnittelig tidsforsinkelse i 2, 4, 8 og 16 inngangs pseudo nMOS og SFPL NOR porter når vi antar at portene skal drive fire identiske porter.

Vi ser på hvordan parasittisk tidsforsinkelse varierer med antall innganger *n* for en pseudo NMOS NOR port:

$$P_u = R_{opptrekk} C_{intern}$$
$$= 3R\left(\frac{2}{3} + n\frac{4}{3}\right)C$$
$$= (4n+2)RC$$
$$= \frac{(4n+2)}{3}\tau$$

$$P_d = R_{nedtrekk} C_{intern}$$
$$= R\left(\frac{2}{3} + n\frac{4}{3}\right)C$$
$$= \frac{(4n+2)}{3}RC$$
$$= \frac{(4n+2)}{9}\tau$$

Tidsforsinkelse:

$$d = f + P_{avg}$$
$$= g_{avg} \cdot h + \frac{4(2n+1)}{9}$$
$$= \frac{8}{9} \cdot 4 + \frac{4(2n+1)}{9}$$
$$= \frac{4}{9}(8 + (2n+1))$$

Vi ser på hvordan parasittisk tidsforsinkelse varierer med antall innganger *n* for en SFPL NOR port:

$$P_d = R_{nedtrekk} C_{intern}$$
$$= \frac{1}{2}\frac{R}{3} \cdot (7 + 8 + n \cdot 6)C$$
$$= \left(\frac{15+2n}{6}\right)\tau$$

$$P_u = R_{opptrekk} C_{intern}$$
$$= \frac{2R}{7}(15 + n \cdot 6)RC$$
$$= 2\left(\frac{15+6 \cdot n}{7}\right)RC$$
$$= 2\left(\frac{5+2 \cdot n}{7}\right)\tau$$

Ekstern last:

$$C_{ekstern} = 4 \cdot (3+3)C$$
$$= 24C$$

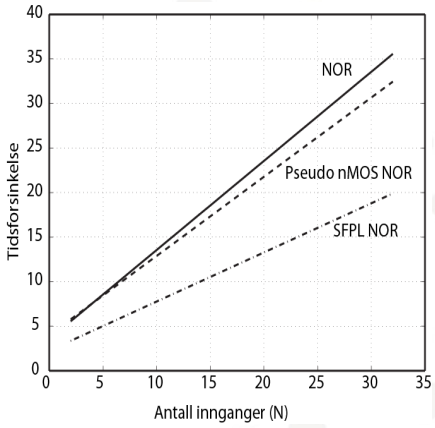
Logisk effort:

$$g_u = \frac{3+3}{W_p + \frac{1}{2}W_p}$$
$$= \frac{6}{7 + \frac{1}{2}7}$$
$$= \frac{4}{9}$$

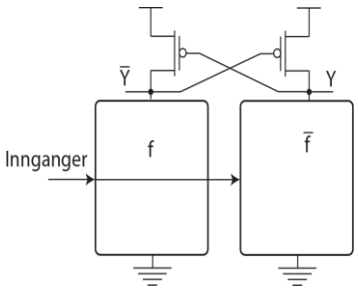
$$g_d = \frac{6}{3\left(6 - \frac{1}{4}6\right)}$$
$$= \frac{4}{9}$$

Tidsforsinkelse:

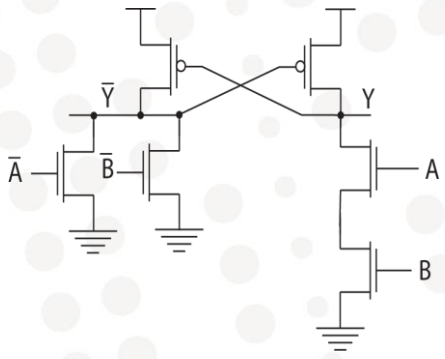
$$d = f + P_{avg}$$
$$= g_{avg} \cdot h + \frac{19}{84}(5+2n)$$
$$= \frac{4}{9} \cdot 4 + \frac{19}{84}(5+2n)$$
$$= \frac{16}{9} + \frac{19}{84}(5+2n)$$



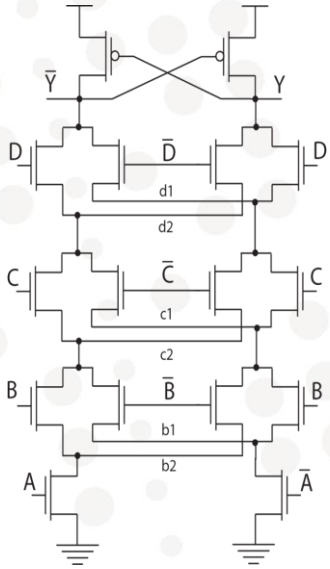
Kaskode spenning svitsj logikk



NAND port

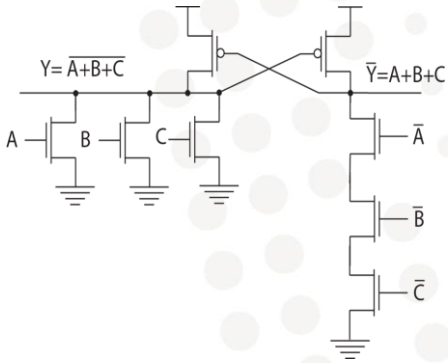


4 inngangs
XNOR port



Oppgave 6.26

Tegn transistorskjema for en 3inngangs CVSL OR /NOR port.



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