INF3410/4411, Fall 2018

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Excerpt of Sedra/Smith Chapter 15: Inverter Delay

Content

Digital/Binary and Analog Linear/Small-Signal Abstraction

Logic gates (book 15.1)

Inverter Gate Delay (book 15.4)

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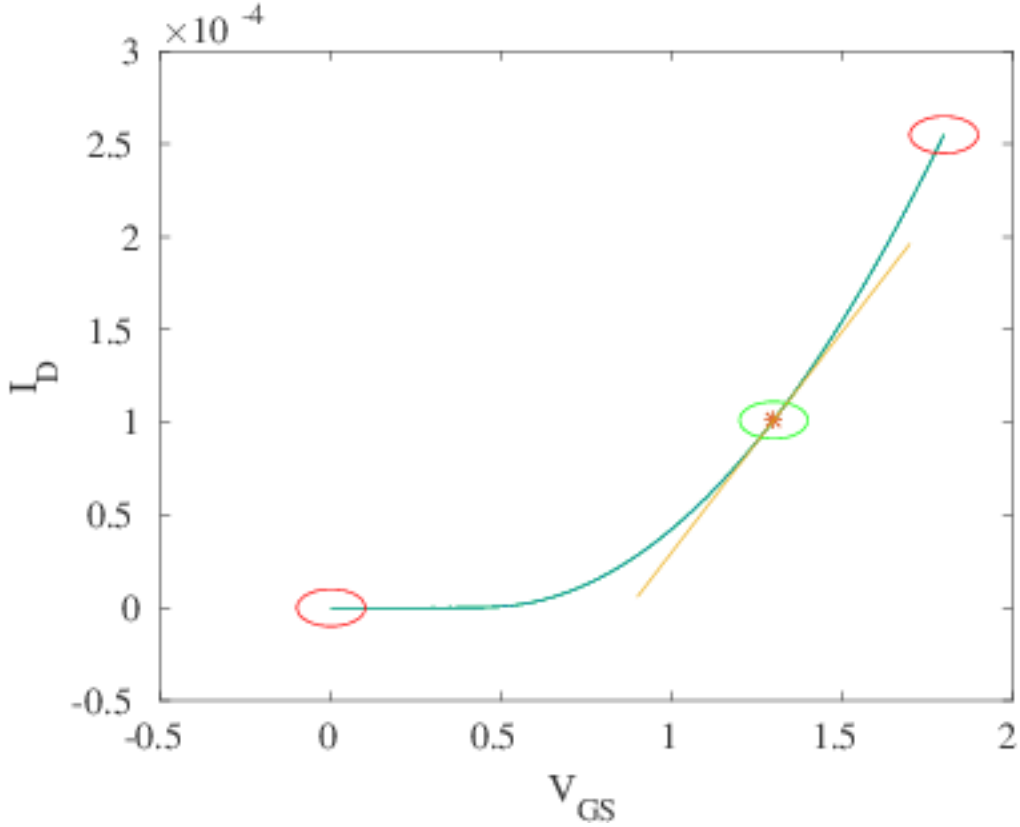
Digital/Binary and Analog Linear/Small-Signal Abstraction
A digital MOSFET model

Logic gates (book 15.1)

Inverter Gate Delay (book 15.4)

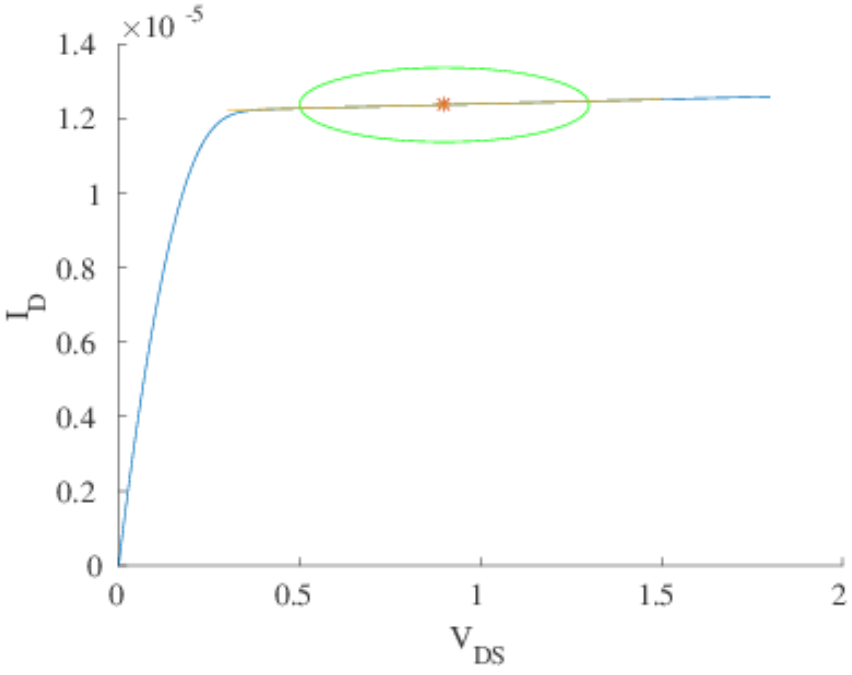
Digital and Analog Simplifications i_D vs. v_{GS}



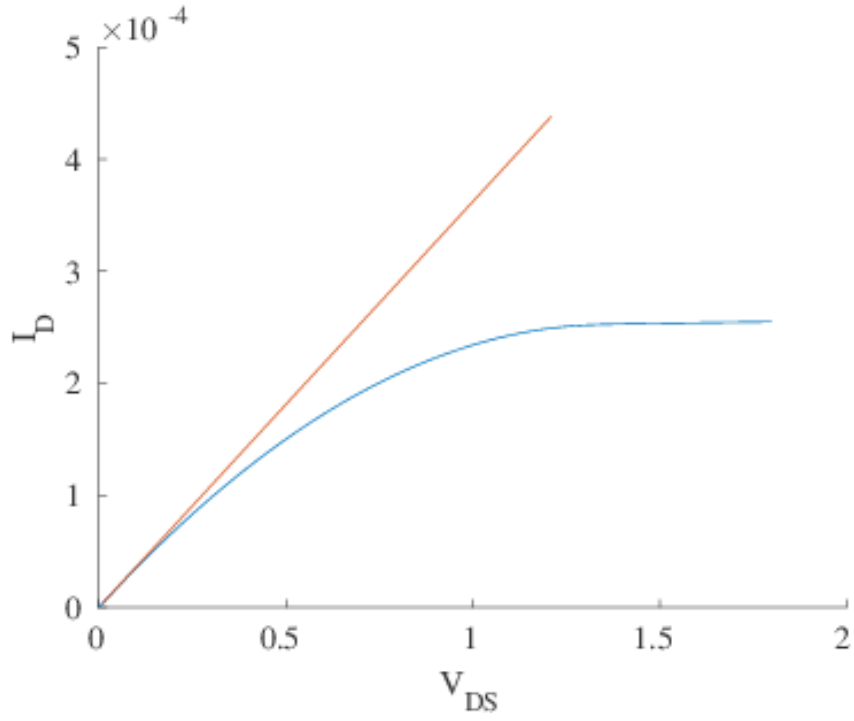
The transistor level digital abstraction only considers the binary input range $v_{GS} \in \{0, Vdd\}$

The transistor level analog abstraction (small signal model) only considers a small input range around a bias point/point of operation and linear output approximation.

Digital and Analog Simplifications i_D vs. v_{DS}

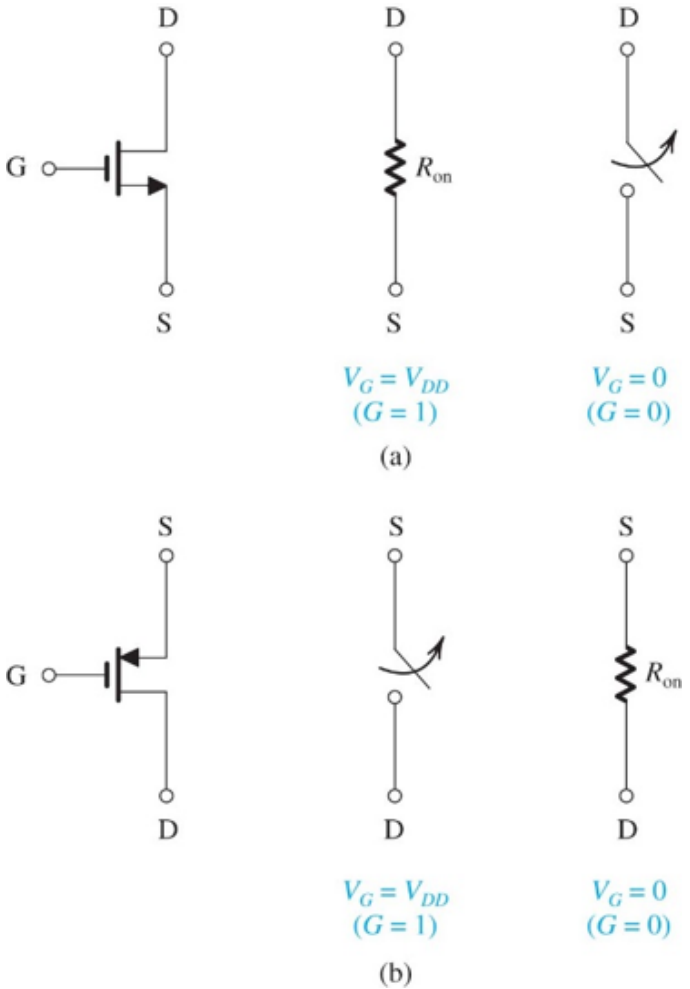


Again the transistor level analog abstraction only considers a small input range around a bias point/point of operation and linear output approximation. In the active region the linear approximation holds for quite a large range for v_{DS}.



The transistor level digital abstraction also uses a linear approximation here for the two different v_{GS}: an open circuit and a resitive behaviour $R_{on} = r_{ds}$.

Digital MOSFET Model Variant



Thus in the digital transistor abstraction both pFET and nFET have two conductive states controlled by the input voltage at the gate.

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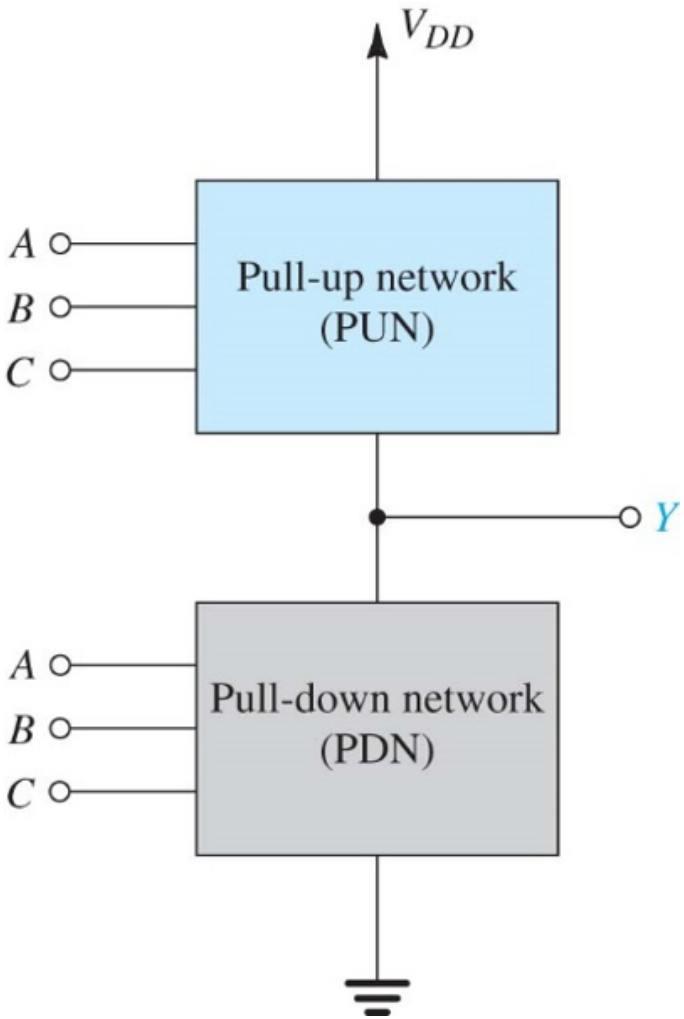
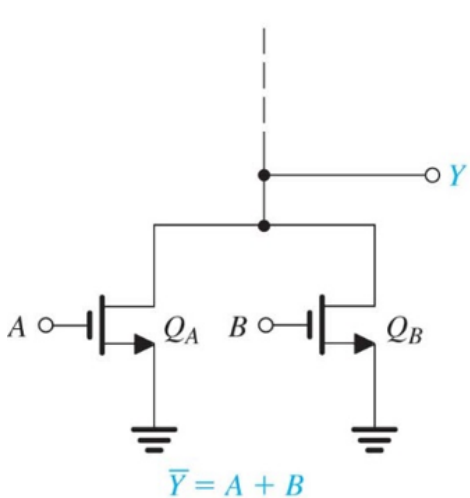
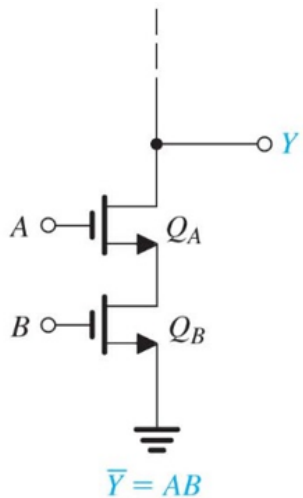
Pull-Up and Pull-Down

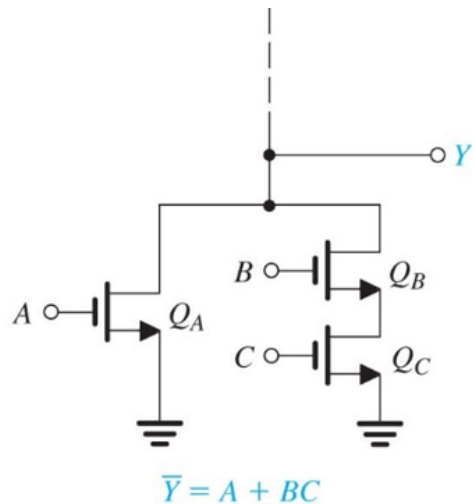


Logic functions can be implemented by complementary pull-up and pull down networks ... or you can just add a resistor tot PUN or PDN... Would that be smart?

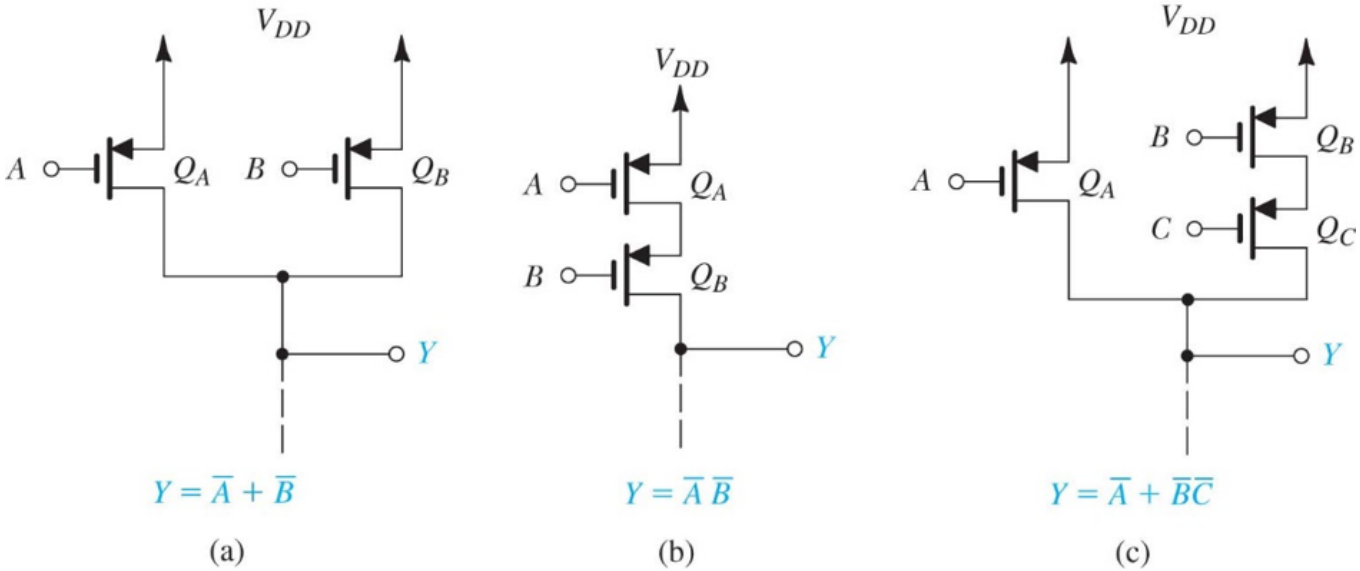
PDN examples







PUN examples



Complementary PUN and PDN

Usually, logic gates are composed of a PUN and PDN that implement eachothers *inverse* function. Such that always either the PUN or the PDN are active. E.g. the PDN:

$$\bar{Y} = (A + B) * C$$

And the PUN

$$Y = \overline{(A + B) * C} = ...$$

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$$\bar{Y} = (A + B) * C$$

And the PUN

$$Y = \overline{(A + B) * C} = \overline{(A + B)} + \bar{C} = (\bar{A} * \bar{B}) + \bar{C}$$

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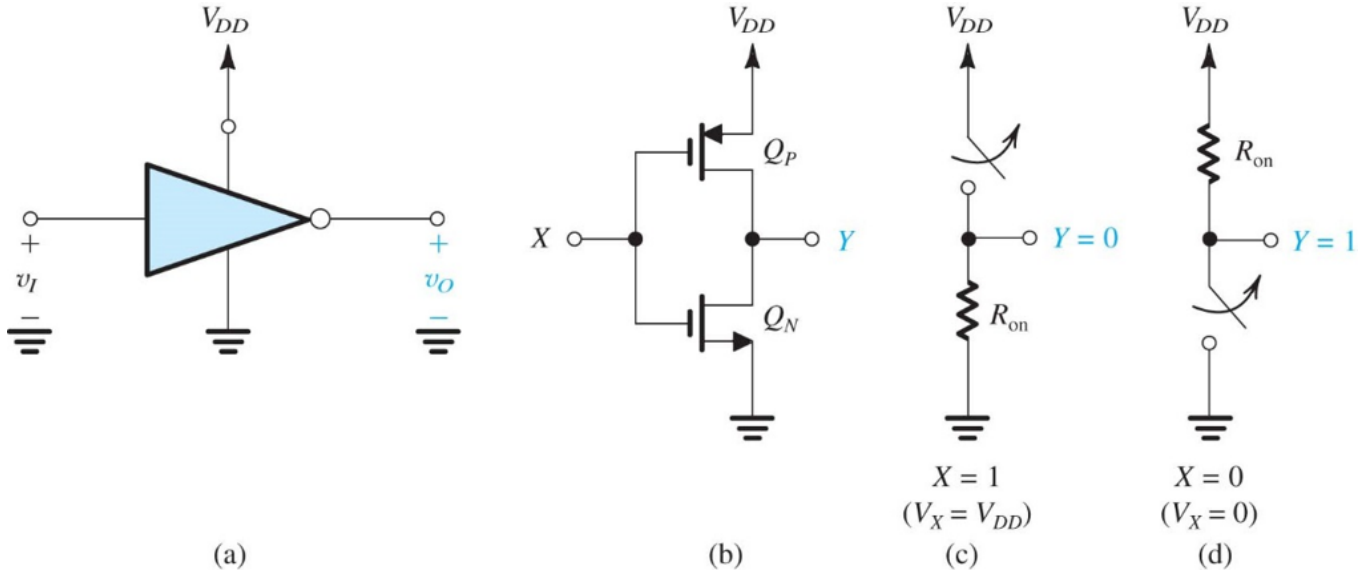
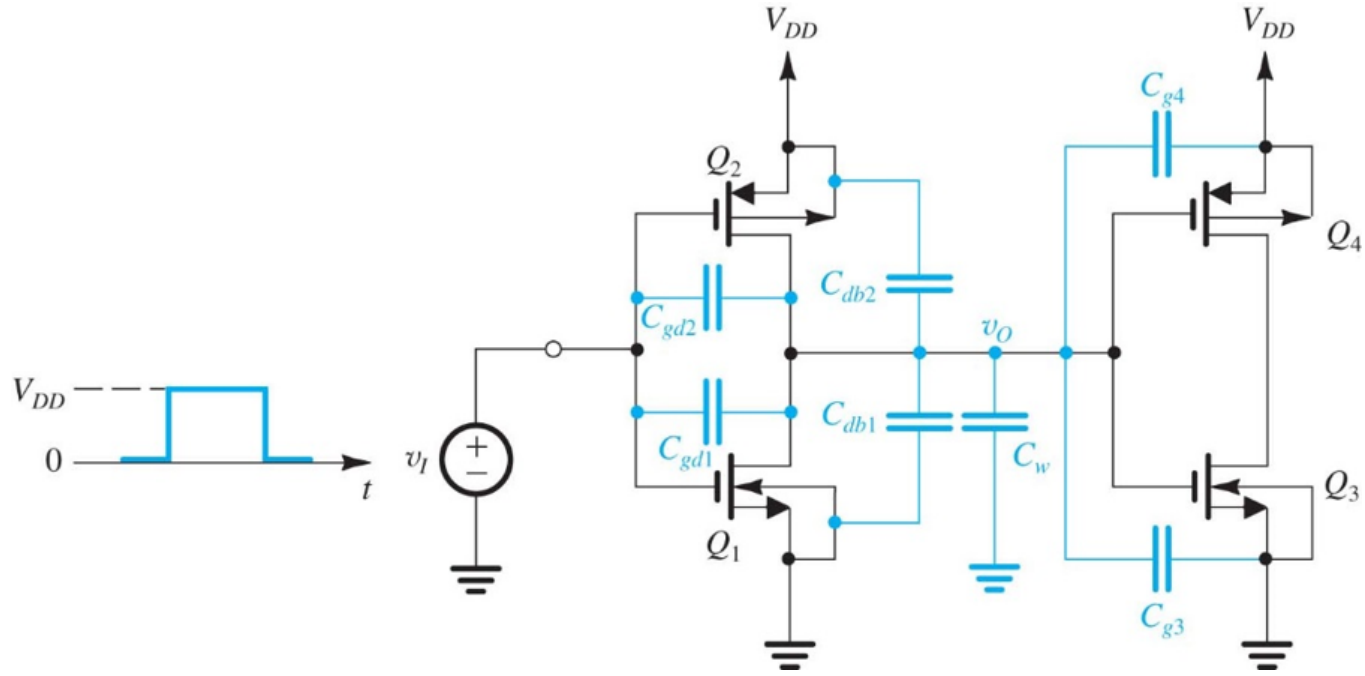
CMOS Inverter Model

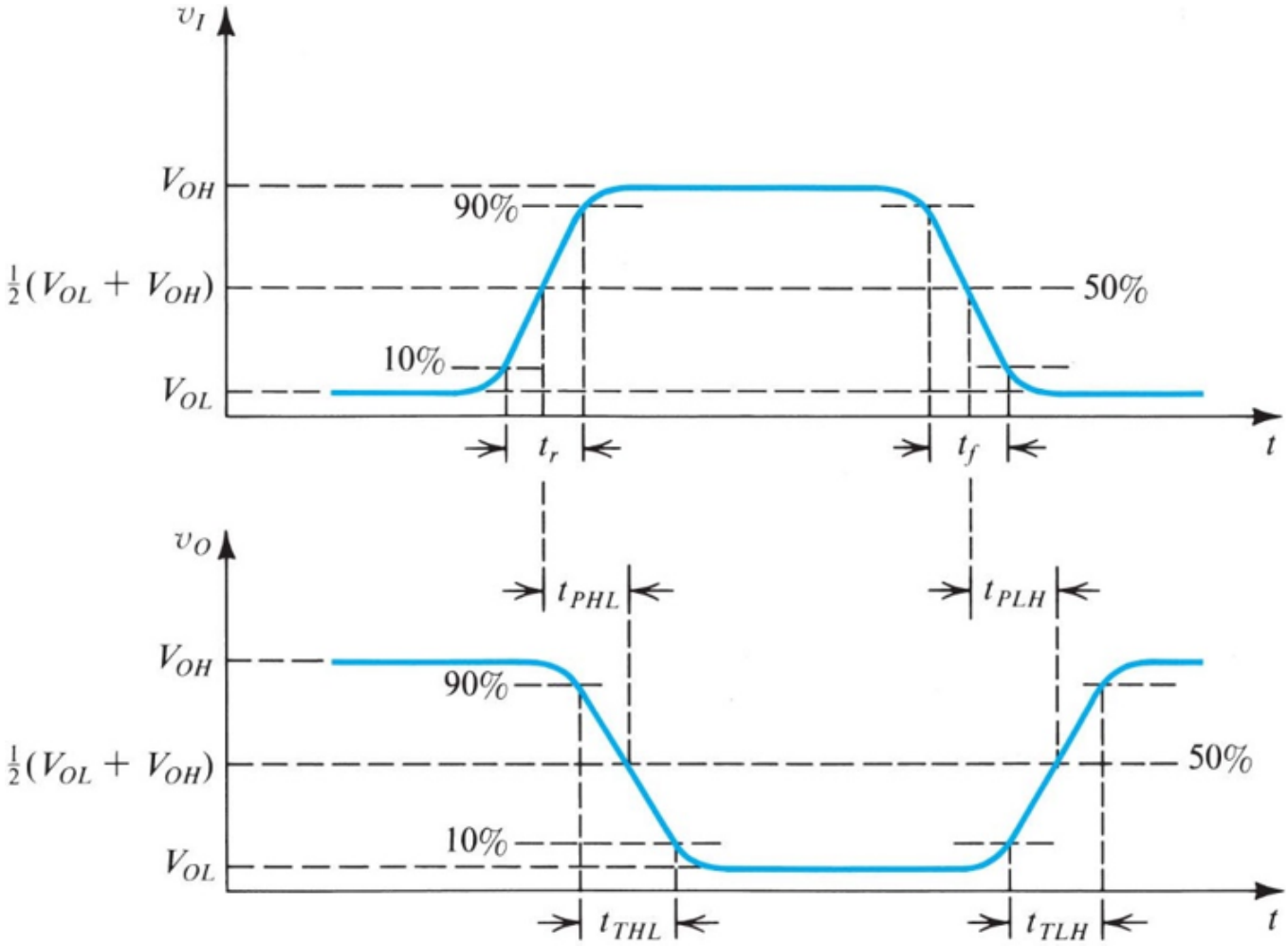


CMOS Inverter HF Model

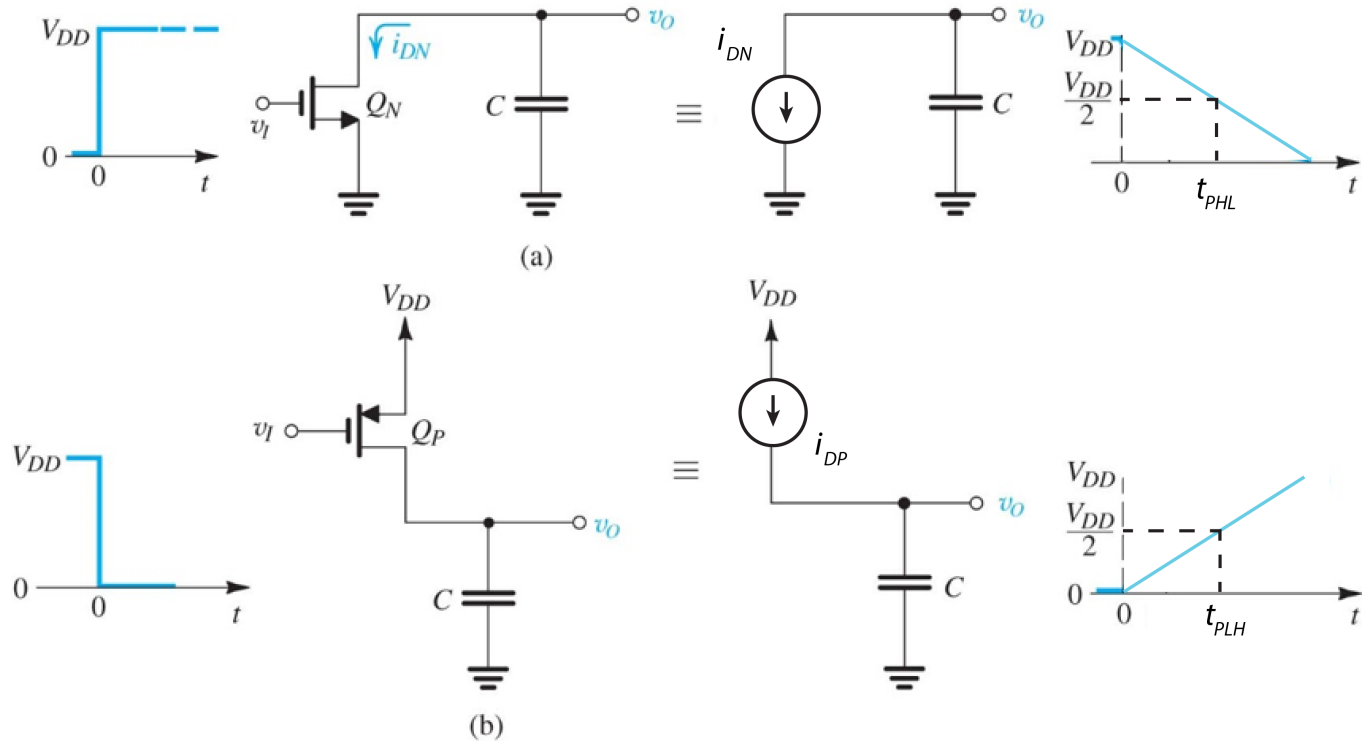


$$C = 2 * (C_{gd1} + C_{gd2}) + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_W \quad (15.59)$$

Propagation delay and transition time



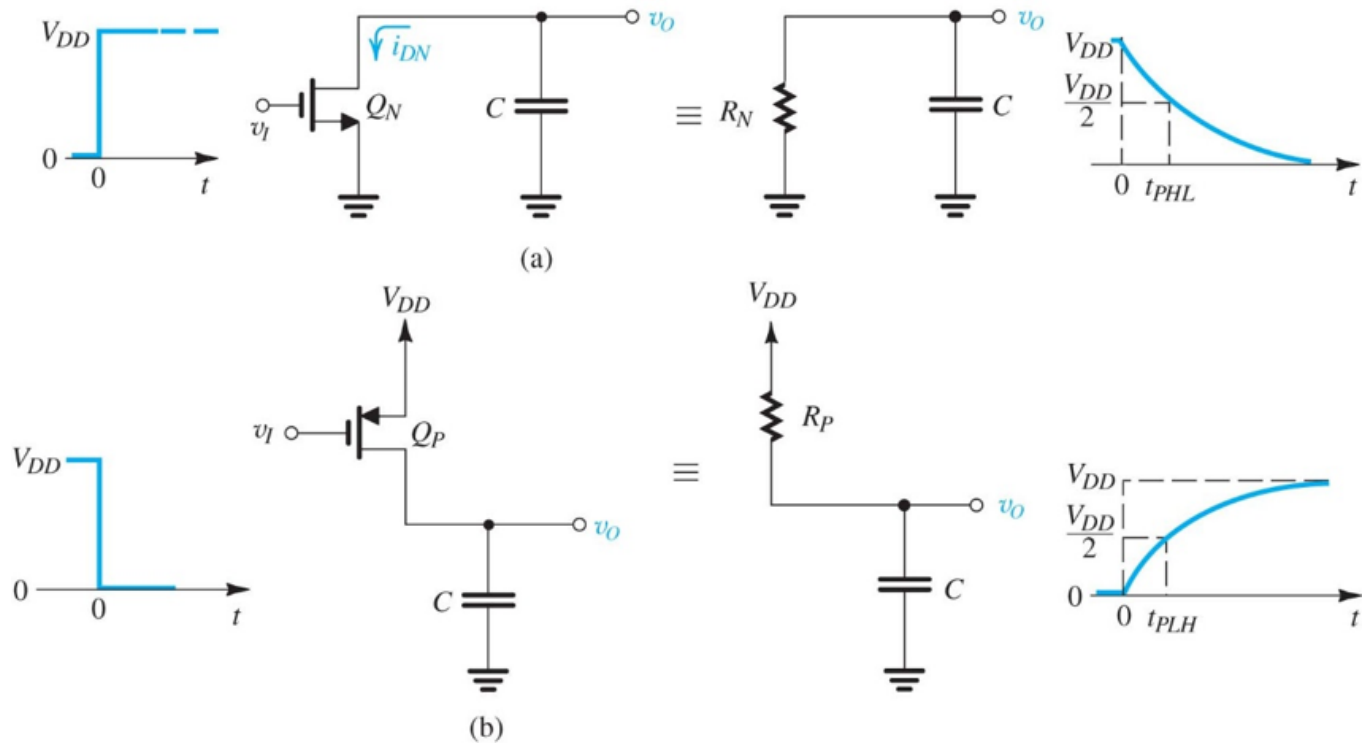
IC model for delay



$$\hat{i}_{DN} = \frac{i_{DN}(\mathrm{Vdd}) + i_{DN}(\frac{\mathrm{Vdd}}{2})}{2} \quad (15.47)$$

$$t_{PHL(LH)} = \frac{C\mathrm{Vdd}}{2\hat{i}_{DN(DP)}} = \frac{\alpha_{n(p)}C}{k_{n(p)}\mathrm{Vdd}} \quad (15.46, 15.50)$$

RC model for delay



$$R_{N(P)} = \frac{12.5(30)}{(W/L)_{n(p)}}\text{k}\Omega \quad (15.56)$$

$$t_{PHL(LH)} = 0.69 R_{n(p)} C \quad (15.54)$$

Observations

- To balance t_{PHL} and t_{PLH} often pFETs in digital circuits are chosen to be wider than nFETs
- In contrast to analog circuits, here maximizing speet (f_T) is prefered before maximizing gain (A_0), i.e. digital transistors are most often minimum length. However, small gain still has a negative impact on noise margin.
- These models are really crude and only give an idea of which parameters to tweak in which direction for an expected result. For reasonable absolute estimates one needs to consult transistor level simulation at least, or even post-layout simulation.